

Complementary High Density Trench MOSFET

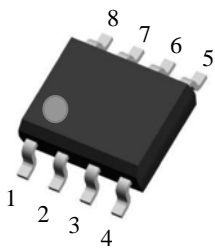
PRODUCT SUMMARY (N-Channel)		
V_{DSS}	I_D	$R_{DS(on)}$ (m Ω) Max
30V	6.5A	28 @ $V_{GS} = 10V, I_D = 6.5A$
		42 @ $V_{GS} = 4.5V, I_D = 5.0A$

PRODUCT SUMMARY (P-Channel)		
V_{DSS}	I_D	$R_{DS(on)}$ (m Ω) Max
-30V	-6.0A	42 @ $V_{GS} = -10V, I_D = -6A$
		70 @ $V_{GS} = -4.5V, I_D = -5A$

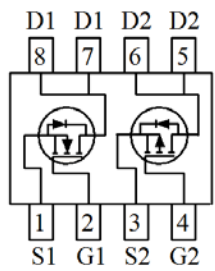
Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Surface mount Package
- Ordering information:GS4606 (Lead(Pb)-free and halogen-free)





Pin 1: Source N
Pin 2: Gate N
Pin 3: Source P
Pin 4: Gate P
Pin 5 / 6: Drain P
Pin 7 / 8: Drain N



SOP-8

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current ^a	6.5	-6.0	A
I_{DM}	Drain Current (Pulsed) ^b	28	-26	A
I_S	Drain-Source Diode Forward Current ^a	2.5	-2.3	A
P_D	Total Power Dissipation @ $T_A=25^\circ\text{C}$ ^a	2	2	W
T_{stg}	Storage Temperature Range ^a	-55 to +150	-55 to +150	$^\circ\text{C}$
T_j	Junction Temperature	150	150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^a	62.5	62.5	$^\circ\text{C/W}$

Note: a: Surface Mounted on FR4 Board, $t \leq 5\text{sec}$.

b: Pulse width limited by maximum junction temperature.

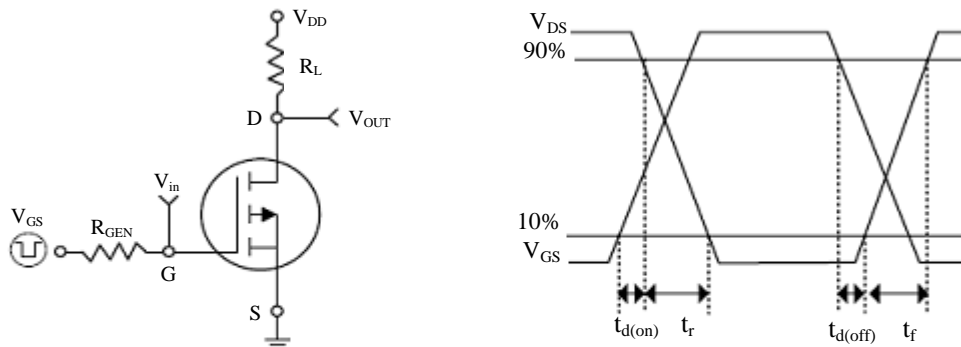
c: UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_j=25^\circ\text{C}$).

N-Channel Electrical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$	-	-	-1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
• On Characteristics^d						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	-	3.0	V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=6.5A$	-	22	28	m Ω
		$V_{GS}=4.5V, I_D=5.0A$	-	34	42	
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=5.0A$	-	6.0	-	S
• Dynamic Characteristics^e						
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	-	398	-	pF
C_{oss}	Output Capacitance		-	67	-	
C_{rss}	Reverse Transfer Capacitance		-	61	-	
• Switching Characteristics^e						
Q_g	Total Gate Charge	$V_{DS}=10V, I_D=1A, V_{GS}=10V$	-	7.4	-	nC
Q_{gs}	Gate-Source Charge		-	1.7	-	
Q_{gd}	Gate-Drain Charge		-	1.3	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15V, R_L=15\Omega, I_D=1A, V_{GS}=10V, R_{GEN}=6\Omega$	-	8.0	-	nS
t_r	Turn-on Rise Time		-	11.2	-	
$t_{d(off)}$	Turn-off Delay Time		-	17.2	-	
t_f	Turn-off Fall Time		-	7.54	-	
• Drain-Source Diode Characteristics						
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS}=0V, I_S=2.5A$	-	-	1.3	V

Note: d: Pulse Test : Pulse Width < 300 μ s, Duty Cycle < 2%

e: Guaranteed by design, not subject to production testing.



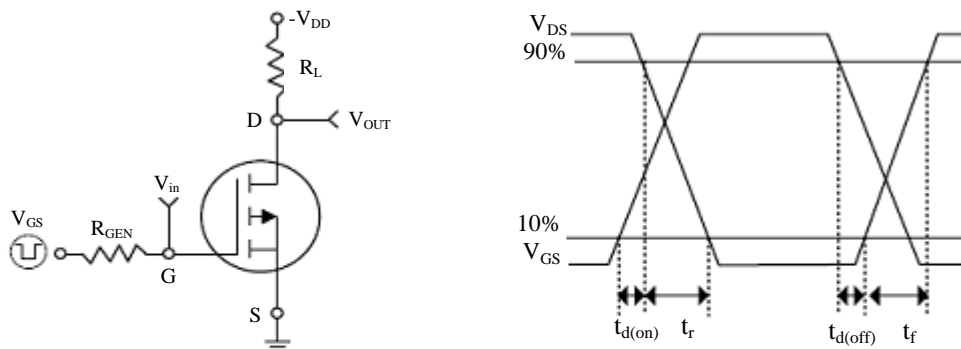
Switching Test Circuit and Switching Waveforms

P-Channel Electrical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
• On Characteristics^d						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-	-3.0	V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=-10V, I_D=-6.0A$	-	33	42	m Ω
		$V_{GS}=-4.5V, I_D=-5.0A$	-	56	70	
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-6.0A$	-	12.7	-	S
• Dynamic Characteristics^e						
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	-	930	-	pF
C_{oss}	Output Capacitance		-	121	-	
C_{rss}	Reverse Transfer Capacitance		-	102	-	
• Switching Characteristics^e						
Q_g	Total Gate Charge	$V_{DS}=-15V, I_D=-3A, V_{GS}=-10V$	-	20	-	nC
Q_{gs}	Gate-Source Charge		-	4.1	-	
Q_{gd}	Gate-Drain Charge		-	2.6	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=-15V, R_L=5\Omega, I_D=-3A, V_{GS}=-10V, R_{GEN}=6\Omega$	-	9.5	-	nS
t_r	Turn-on Rise Time		-	5.4	-	
$t_{d(off)}$	Turn-off Delay Time		-	42.5	-	
t_f	Turn-off Fall Time		-	13.6	-	
• Drain-Source Diode Characteristics						
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS}=0V, I_S=-2.3A$	-	-	-1.2	V

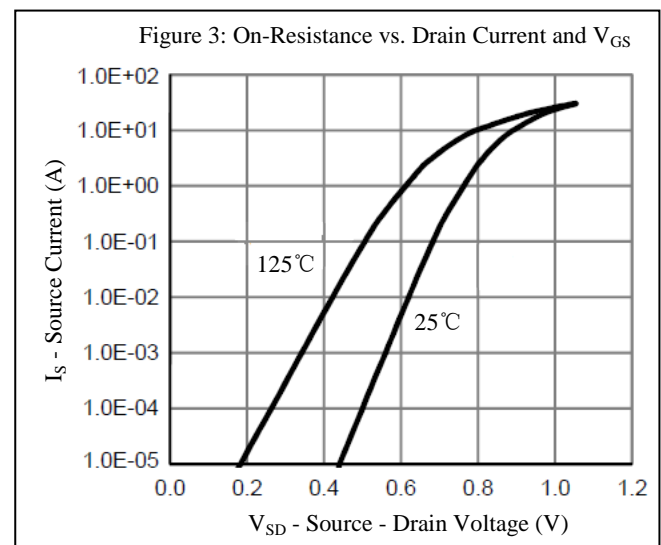
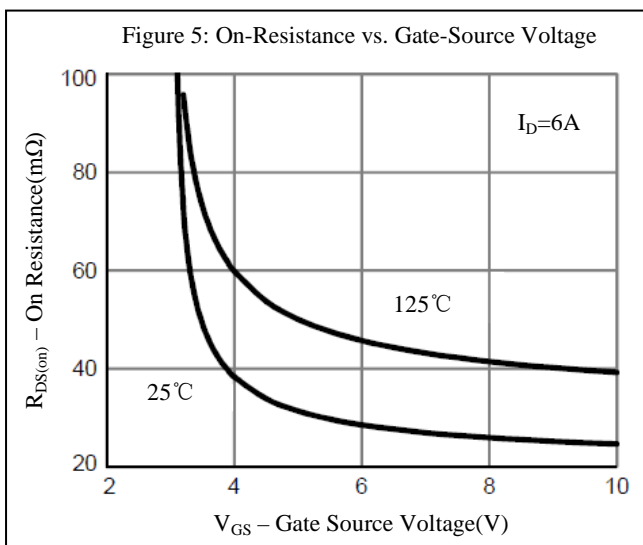
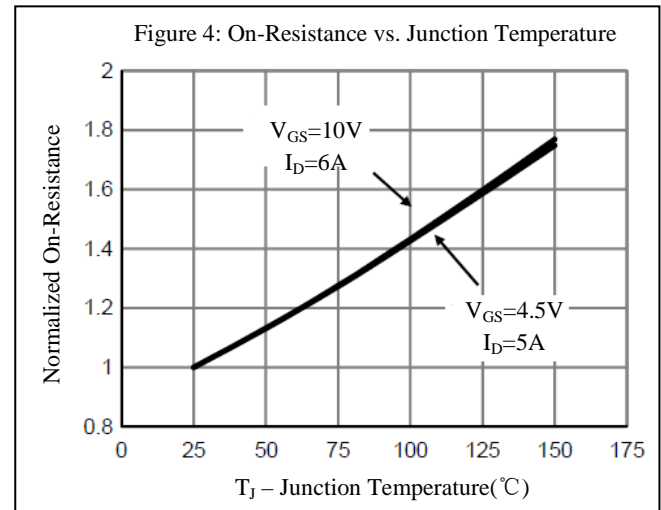
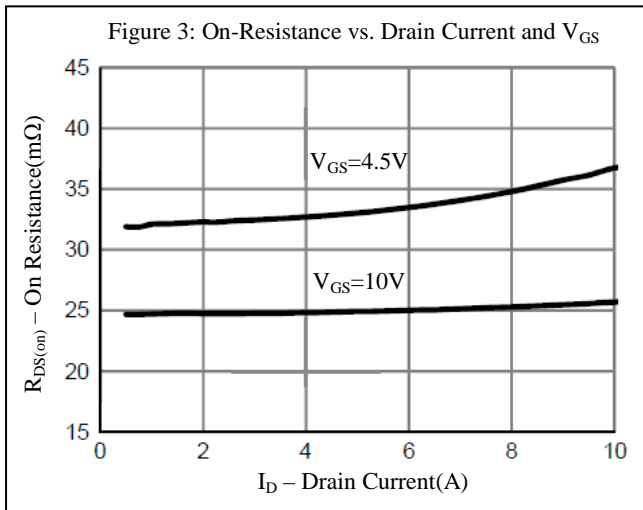
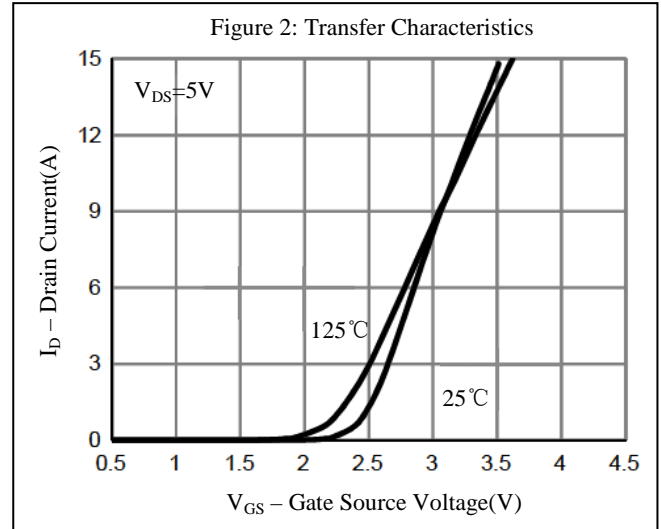
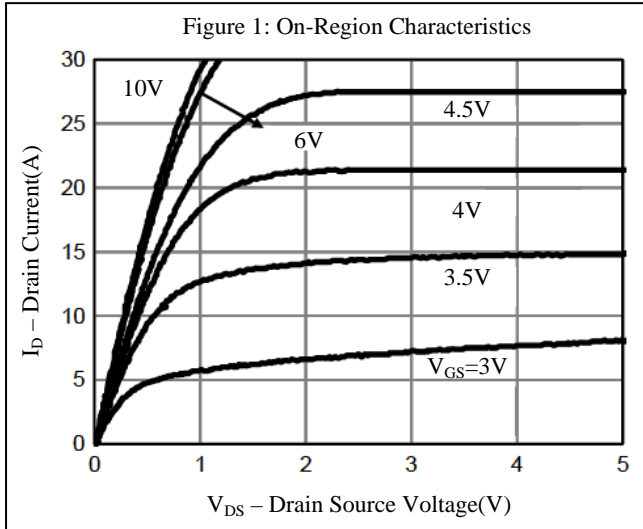
Note: d: Pulse width limited by maximum junction temperature.

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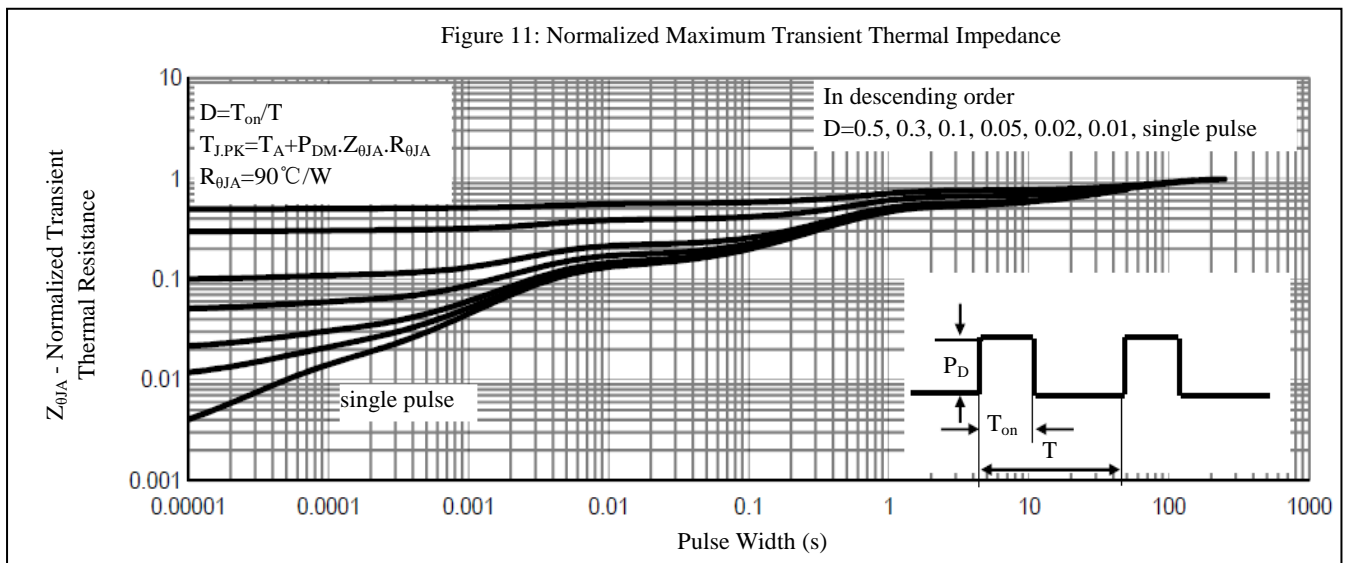
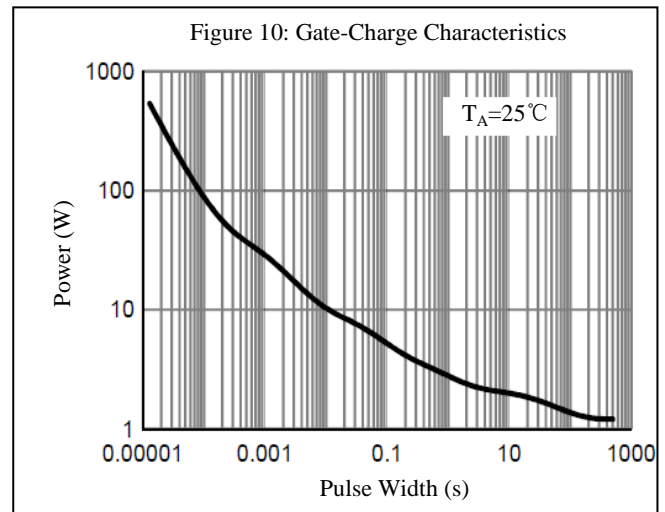
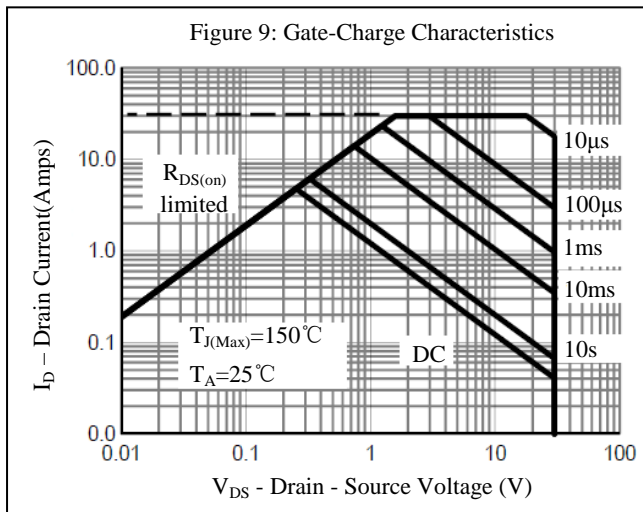
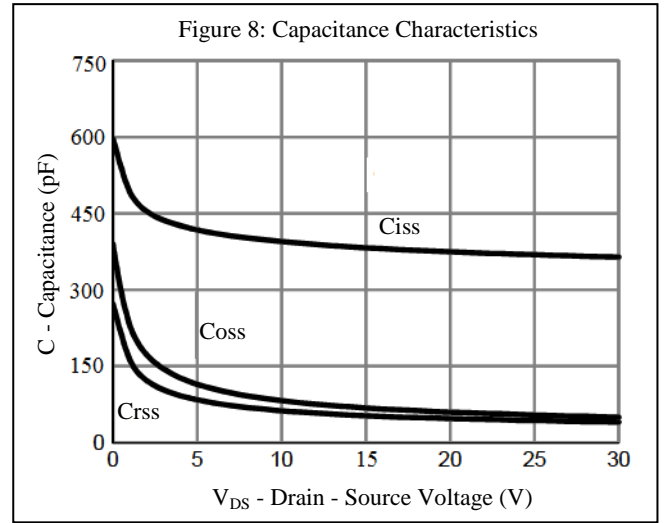
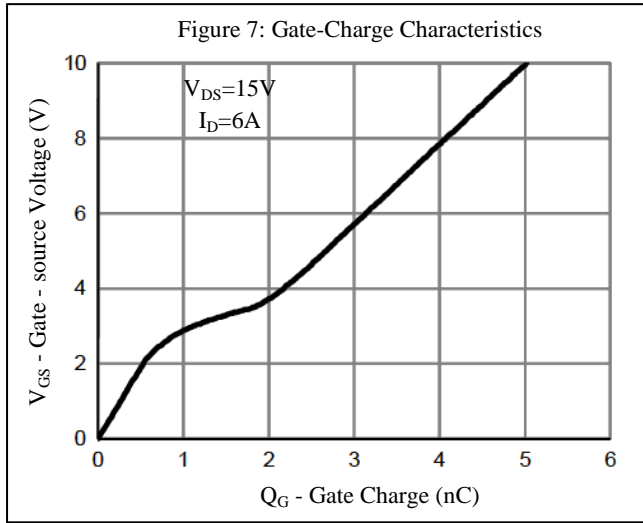


Switching Test Circuit and Switching Waveforms

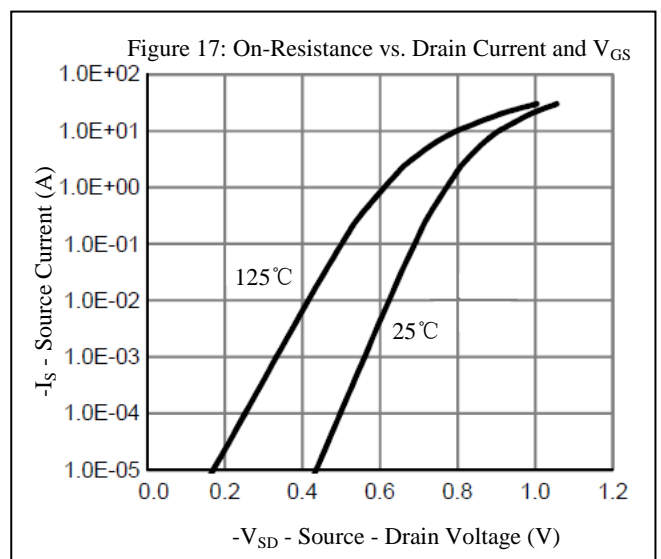
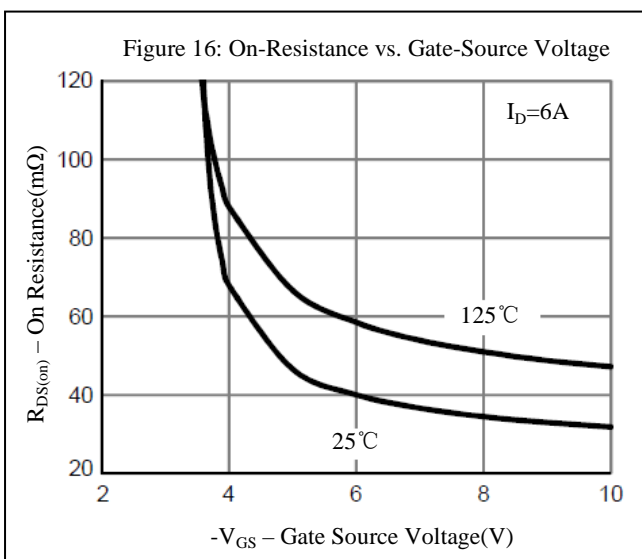
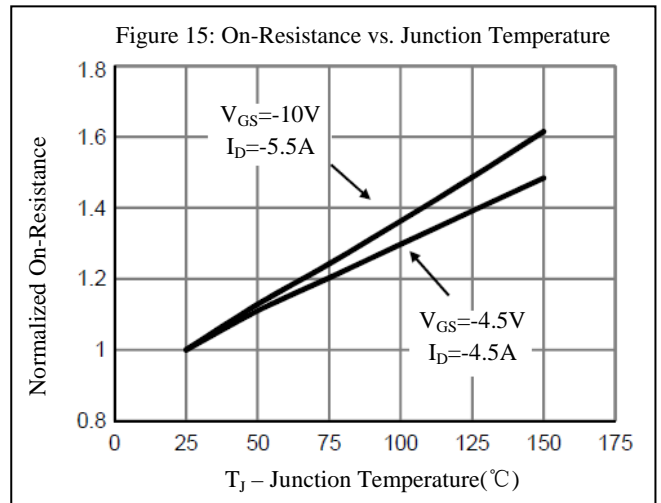
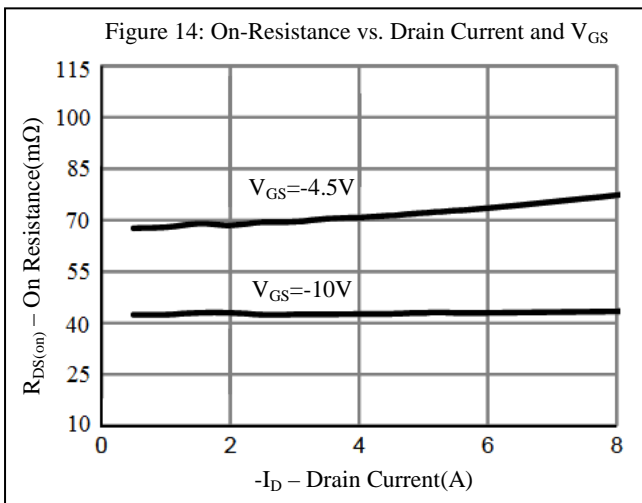
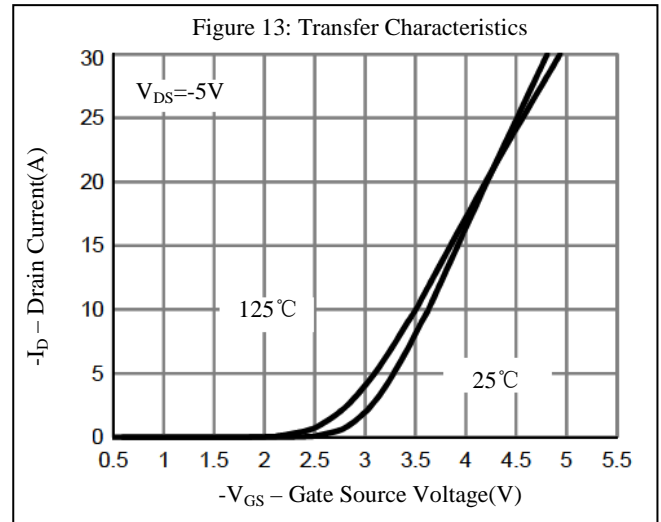
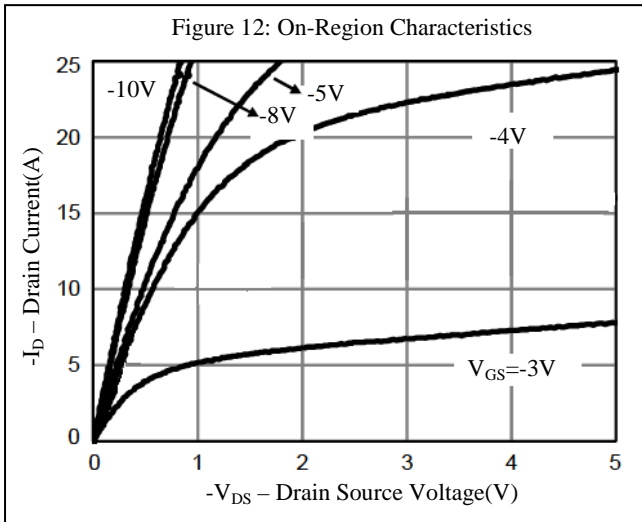
Characteristics Curve(N-Channel)



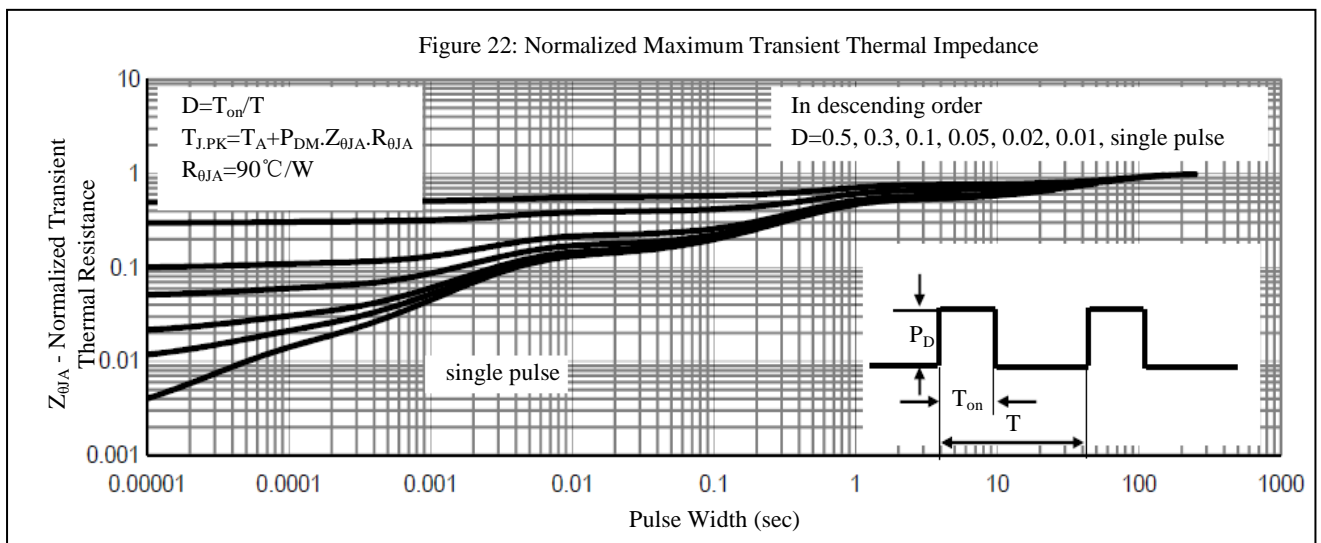
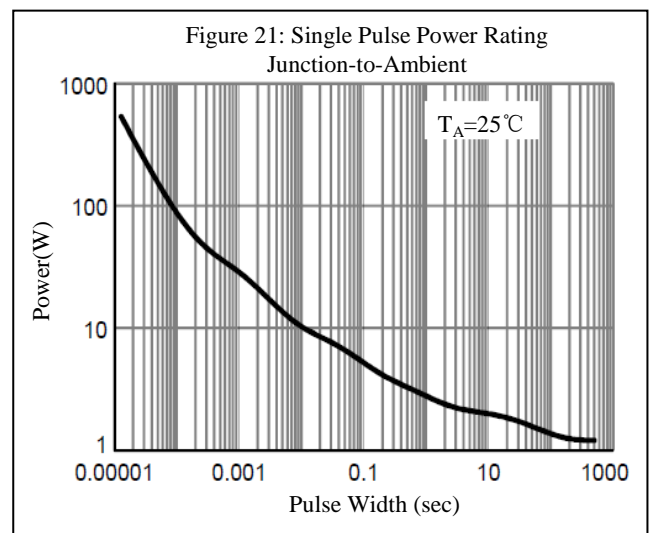
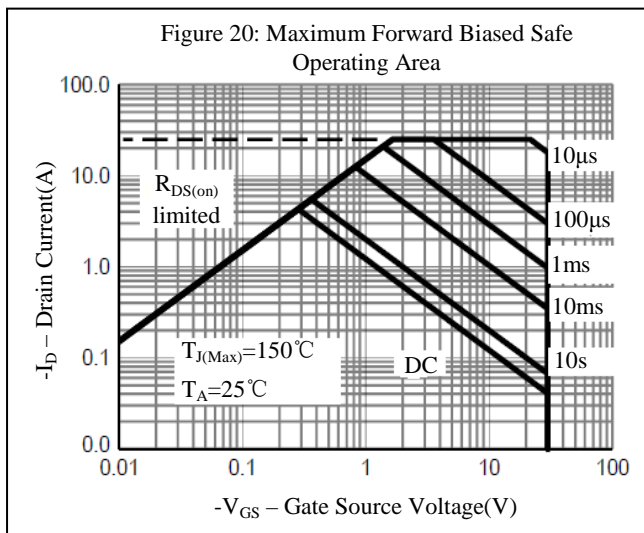
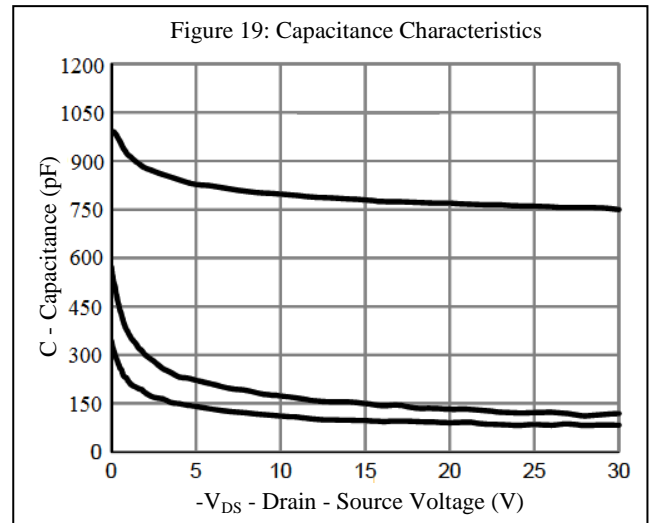
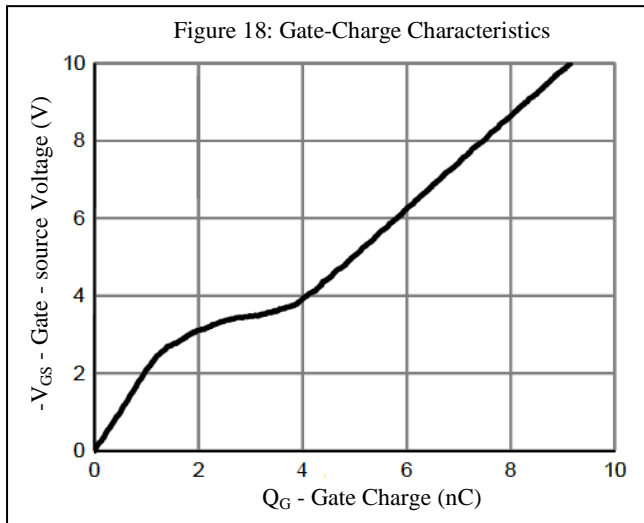
Characteristics Curve(N-Channel)



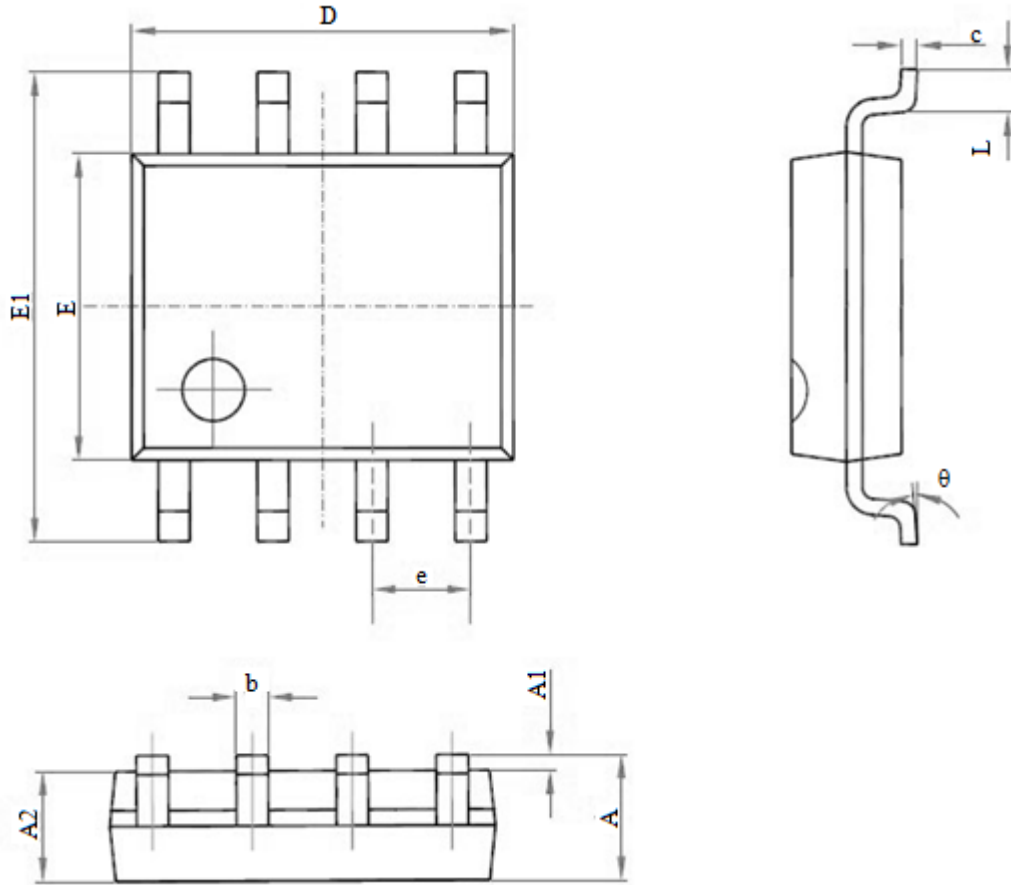
Characteristics Curve(P-Channel)



Characteristics Curve(P-Channel)



SOP-8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters (MM)		Dimensions In Inches (MIL)	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.170	0.250	0.006	0.010
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Notice

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2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.