

GL Silicon N-Channel Power MOSFET

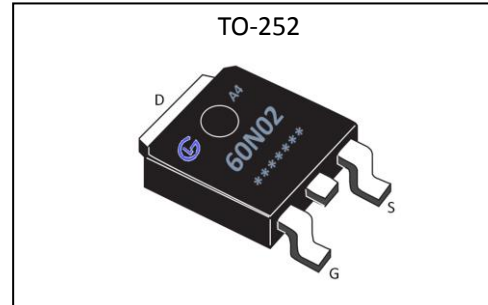
General Description :

The GL60N02A4 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is TO-252, which accords with the RoHS standard.

V_{DSS}	20	V
I_D	60	A
P_D	60	W
$R_{DS(ON)type}$	3.8	m Ω

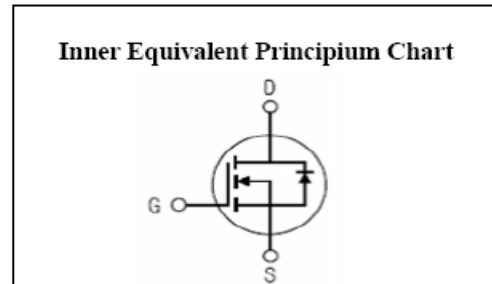
Features :

- $R_{DS(ON)} < 5m\Omega$ @ $V_{GS}=10V$ (Typ3.8m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Applications :

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Absolute ($T_c = 25^\circ C$ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	20	V
I_D	Continuous Drain Current	60	A
I_{DM}	Pulsed Drain Current	200	A
V_{GS}	Gate-to-Source Voltage	± 12	V
P_D	Power Dissipation	60	W
E_{AS}	Single pulse avalanche energy ^{a5}	200	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range	175, -55 to 150	$^\circ C$



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Electrical Characteristics (Tc= 25°C unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	--	--	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} =20V, V _{GS} = 0V, T _a = 25°C	--	--	1.0	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} = +12V	--	--	0.1	μA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} = -12V	--	--	-0.1	μA

ON Characteristics ^{a3}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)1}	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =20A	--	3.8	5.0	mΩ
R _{DS(ON)2}	Drain-to-Source On-Resistance	V _{GS} =4.5V, I _D =20A	--	4.2	5.5	mΩ
R _{DS(ON)2}	Drain-to-Source On-Resistance	V _{GS} =2.5V, I _D =10A	--	4.8	6.3	mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.5	0.8	2.0	V
Pulse width tp≤380μs, δ≤2%						

Dynamic Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =20A	15	--	--	S
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V f=1.0MHz	--	2000	--	pF
C _{oss}	Output Capacitance		--	500	--	
C _{rss}	Reverse Transfer Capacitance		--	210	--	

Resistive Switching Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =10V, I _D =25A V _{GS} =5V, R _G =1.8Ω	--	7	--	ns
t _r	Rise Time		--	18	--	
t _{d(OFF)}	Turn-Off Delay Time		--	30	--	
t _f	Fall Time		--	17	--	
Q _g	Total Gate Charge	V _{DD} =10V, I _D =25A V _{GS} =10V	--	28	--	nC
Q _{gs}	Gate to Source Charge		--	7	--	
Q _{gd}	Gate to Drain ("Miller") Charge		--	6.8	--	



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Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current ^{a2} (Body Diode)		--	--	60	A
V_{SD}	Diode Forward Voltage ^{a3}	$I_S=60A, V_{GS}=0V$	--	--	1.2	V

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case ^{a2}	2.1	°C/W

^{a1} : Repetitive Rating: Pulse width limited by maximum junction temperature.

^{a2} : Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

^{a3} : Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

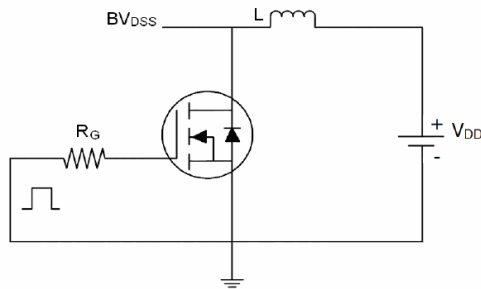
^{a4} : Guaranteed by design, not subject to production

^{a5} : EAS condition : $T_j=25^\circ\text{C}, V_{DD}=15V, V_{GS}=10V, L=1.0\text{mH}, R_g=25\Omega$

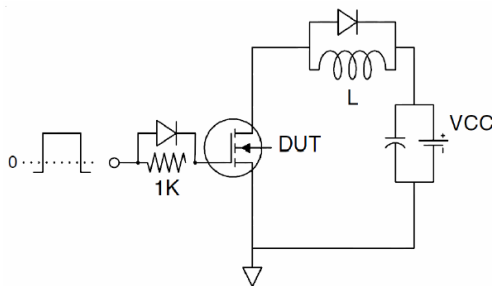
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Test circuit

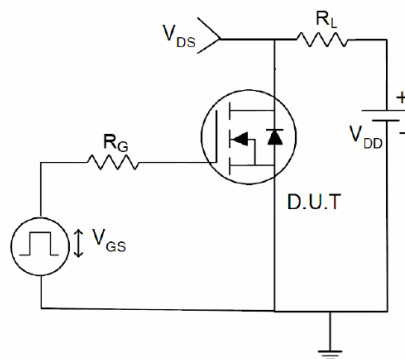
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:





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Characteristics Curve :

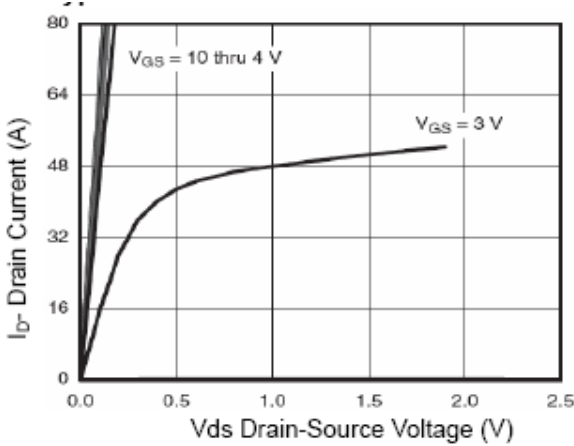


Figure 1 Output Characteristics

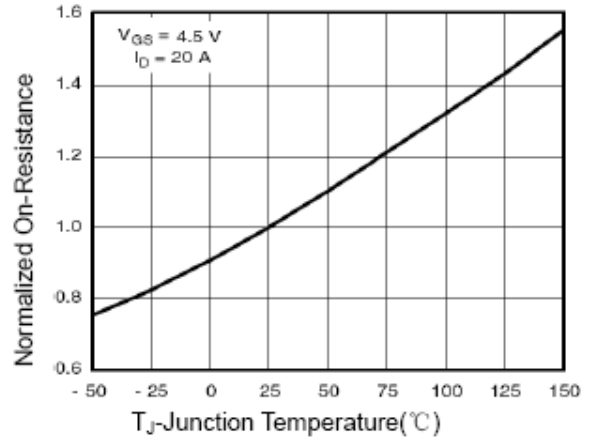


Figure 4 Rdson-Junction Temperature

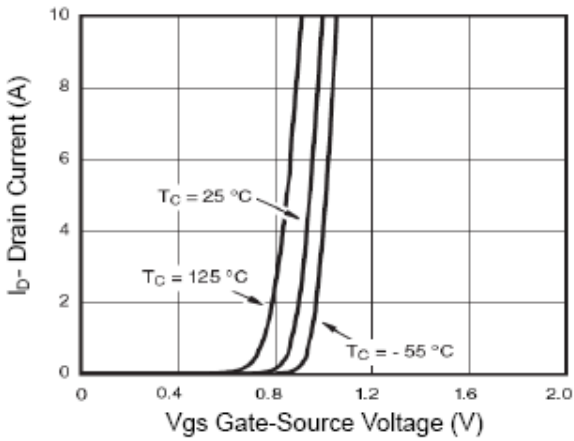


Figure 2 Transfer Characteristics

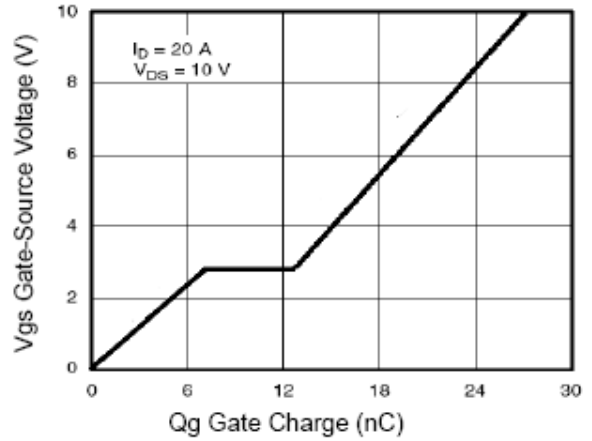


Figure 5 Gate Charge

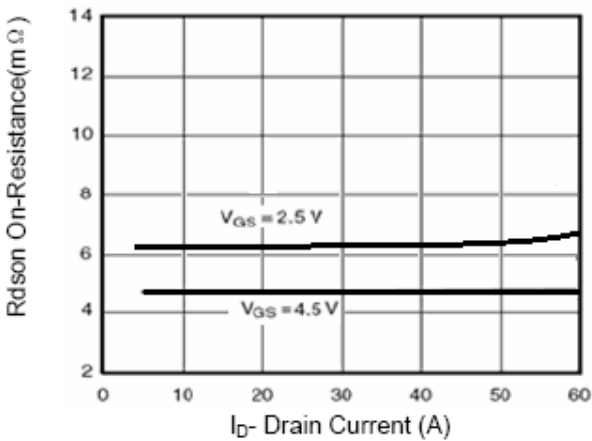


Figure 3 Rdson- Drain Current

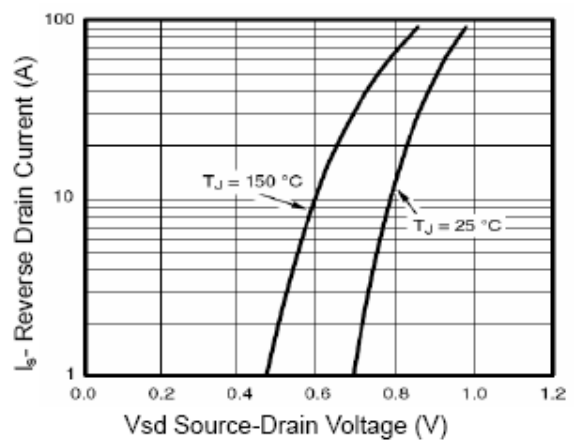


Figure 6 Source- Drain Diode Forward



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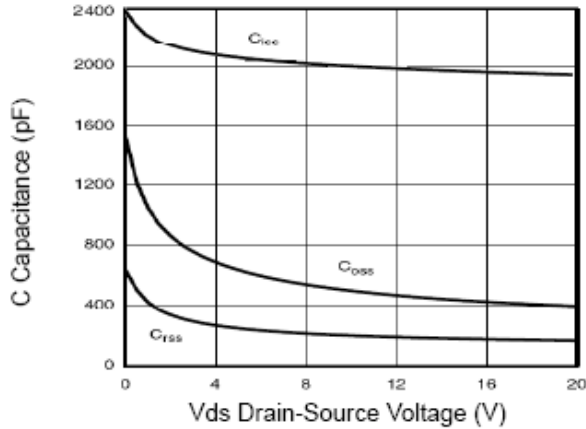


Figure 7 Capacitance vs Vds

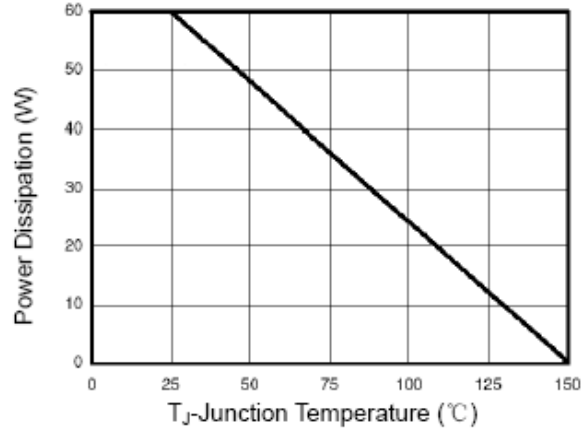


Figure 9 Power De-rating

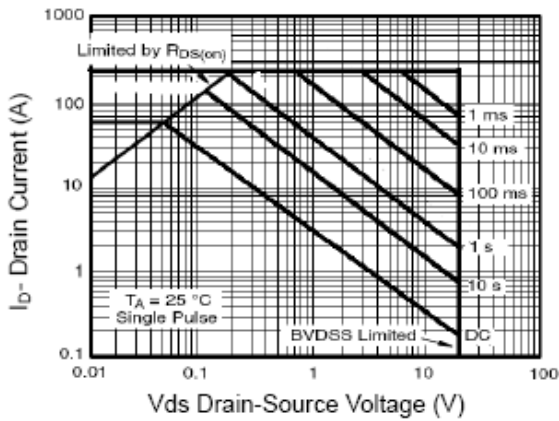


Figure 8 Safe Operation Area

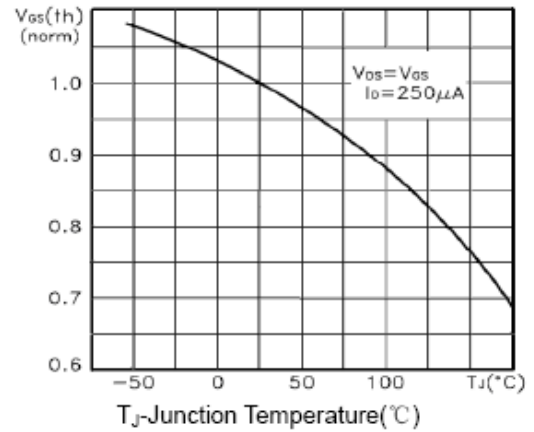


Figure 10 $V_{GS(th)}$ vs Junction Temperature

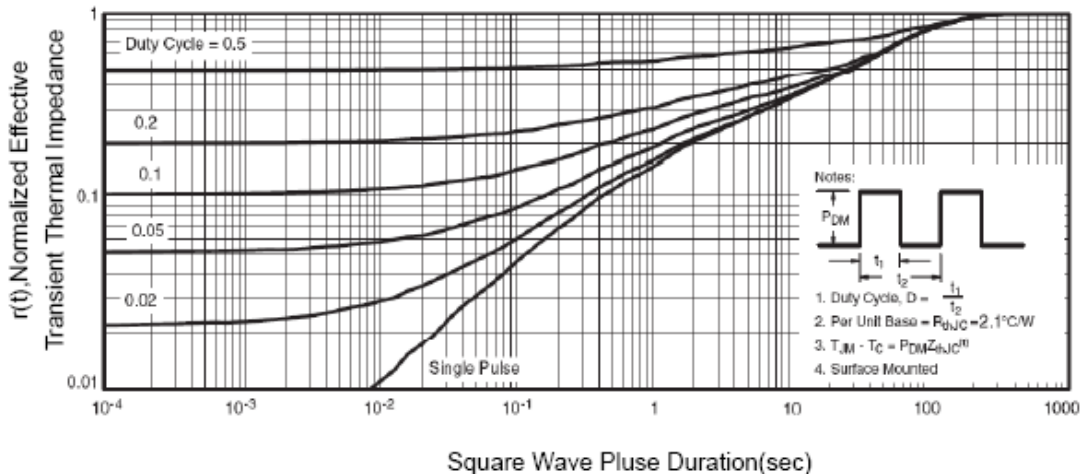


Figure 11 Normalized Maximum Transient Thermal Impedance

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