NCP81258

Product Preview

Synchronous Buck MOSFET Driver

The NCP81258 is a high−performance dual MOSFET gate driver in a small 2 mm x 2 mm package, optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. A zero−current detection feature allows for a high−efficiency solution even at light load conditions. VCC UVLO ensures the MOSFETs are off when supply voltages are low. A bi−directional Enable pin provides a fault signal to the controller when a UVLO fault is detected.

Features

- Space−efficient 2 mm x 2 mm DFN8 Thermally−enhanced Package
- VCC Range of 4.5 V to 13.2 V
- Internal Bootstrap Diode
- 5 V 3−stage PWM Input
- Zero Current Detect Function Provides Power Saving Operation during Light Load Conditions
- Bi−directional Enable Feature pulls Enable Pin Low during a UVLO Fault
- Pre−OVP Function Protects Load during HS FET Short
- Adaptive Anti−cross Conduction Circuit Protects against Cross−conduction during FET Turn−on and Turn−off
- Output Disable Control Turns Off Both MOSFETs via Enable Pin
- VCC Undervoltage Lockout
- These Devices are Pb−free, Halogen−free/BFR−free and are RoHS Compliant

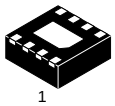
Typical Applications

- Power Solutions for Notebook and Desktop Systems

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

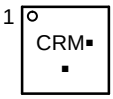
ON Semiconductor®

www.onsemi.com



DFN8
MN SUFFIX
CASE 506AA

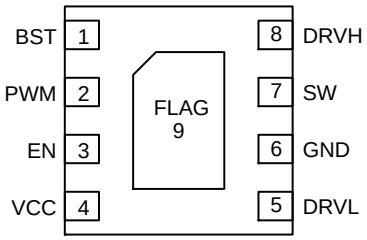
MARKING DIAGRAM



CR = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81258MNTBG	DFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

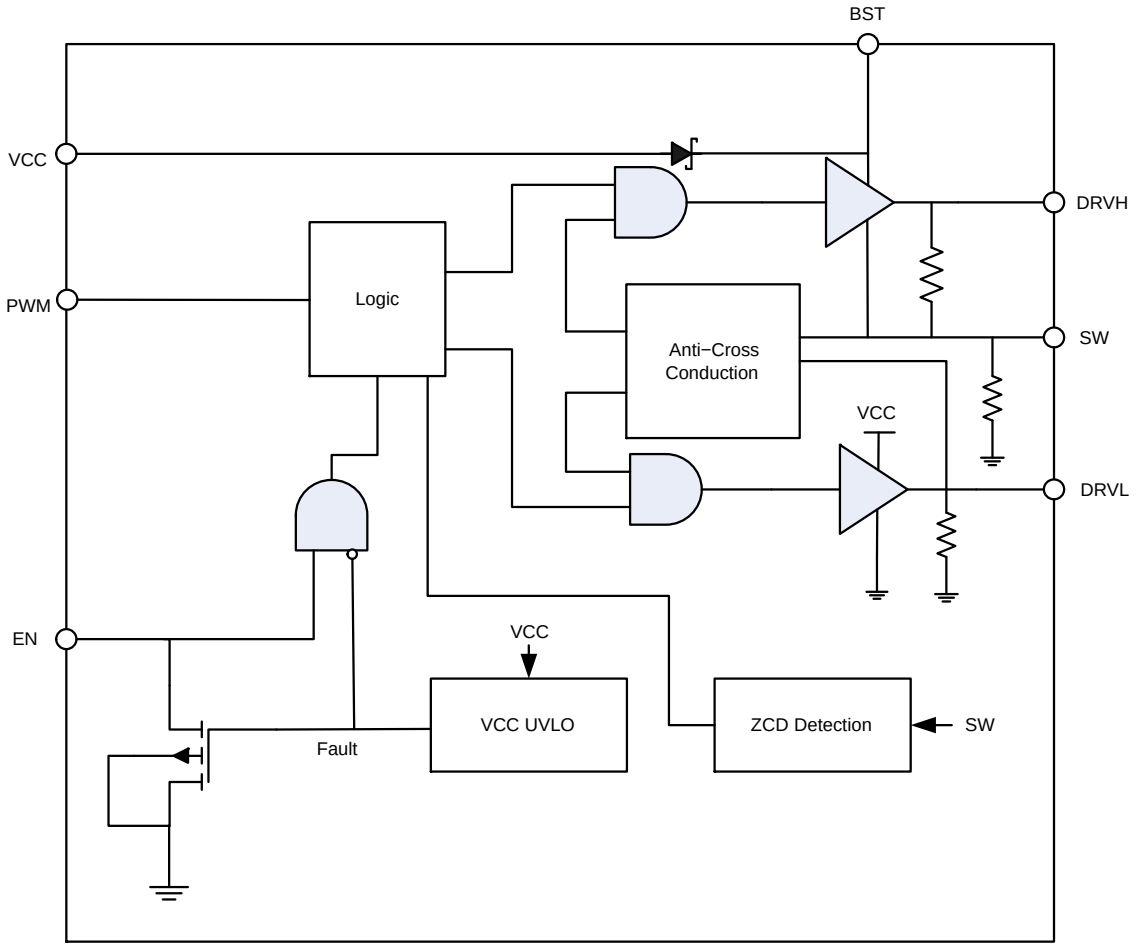


Figure 1. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	BST	Floating bootstrap supply pin for the high−side gate driver. Connect the external bootstrap capacitor between this pin and SW.
2	PWM	Control input: PWM = High → DRVH is high, DRVL is low. PWM = Mid → Zero current detect enabled. Diode emulation mode. PWM = Low → DRVH is low, DRVL is high.
3	EN	Control input: EN = High → Driver is enabled. EN = Low → Driver is disabled.
4	VCC	Power supply input. Connect a bypass capacitor (1 μF) from this pin to ground.
5	DRVL	Low−side gate drive output. Connect to the gate of the low−side MOSFET.
6	GND	Bias and reference ground. All signals are referenced to this node.
7	SW	Switch node. Connect this pin to the source of the high−side MOSFET and drain of the low−side MOSFET.
8	DRVH	High−side gate drive output. Connect to the gate of the high−side MOSFET.
9	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to the ground plane.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max
Main Supply Voltage (Note 1)	VCC	−0.3 V	15 V 16 V (< 50 ns)
Bootstrap Supply Voltage	BST	−0.3 V wrt/SW	35 V wrt/GND 40 V (≤ 50 ns) wrt/GND 15 V wrt/SW
Switch Node Voltage	SW	−5 V −10 V (≤ 200 ns)	35 V 40 V (≤ 50 ns)
High−Side Driver Output	DRVH	−0.3 V wrt/SW −2 V (≤ 200 ns) wrt/SW	BST + 0.3 V SW + 15 V (< 80 ns)
Low−Side Driver Output	DRVL	−0.3 V −5 V (≤ 200 ns)	VCC + 0.3 V 15 V (< 80 ns)
DRVH/DRVL Control Input, Enable Pin	PWM, EN	−0.3 V	6.5 V
Ground	GND	0 V	0 V
Storage Temperature Range	T_{STG}	−55°C	150°C
Operating Junction Temperature Range	T_J	−40°C	150°C
Moisture Sensitivity Level	MSL	1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN8, 2x2 mm (Note 2) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	74	°C/W

2. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 3)

Rating	Symbol	Min	Max	Unit
Input Voltage	VCC	4.5	13.2	V
Ambient Temperature	T_A	−10	125	°C

3. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS VCC = 4.5 V to 13.2 V, BST−SW = 4.5 V to 13.2 V, BST = 4.5 V to 30 V, SW = 0 V to 21 V; for typical values T_A = 25°C, for min/max values T_A = −10°C to 125°C; unless otherwise noted. (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
VCC Operation Voltage			4.5		13.2	V
Pre−OVP VCC Threshold				2.75	3.2	V
UNDERVOLTAGE LOCKOUT						
VCC Start Threshold	V_{CC} rising	V_{UVLO}	3.8	4.35	4.5	V
VCC UVLO Hysteresis		V_{UVLO_HYS}	150	200	250	mV
Output Overvoltage Trip Threshold at Startup	V_{CC} > Pre−OVP VCC Threshold		2.1	2.25	2.4	V
SUPPLY CURRENT						
Normal Mode	I_{CC} + I_{BST}, EN = 5 V, PWM = 100 kHz, C_{LOAD} = 3 nF for DRVH, 3 nF for DRVL	I_{normal}		12.2		mA
Shutdown Mode	I_{CC} + I_{BST}, EN = GND	$I_{shutdown}$		0.5	1.9	mA
Standby Current 1	I_{CC} + I_{BST}, EN = 5 V, PWM = 0 V, No loading on DRVH & DRVL	$I_{standby1}$		2.1		mA
Standby Current 2	I_{CC} + I_{BST}, EN = 5 V, PWM = 5 V, No loading on DRVH & DRVL	$I_{standby2}$		2.2		mA
BOOTSTRAP DIODE						
Forward Voltage	V_{CC} = 12 V, Forward bias current = 2 mA		0.1	0.4	0.6	V
PWM INPUT						
PWM Input High		PWM_{HI}	3.4			V
PWM Mid−State		PWM_{MID}	1.3		2.7	V
PWM Input Low		PWM_{LO}			0.7	V
ZCD Blanking Timer				250		ns
HIGH−SIDE DRIVER (VCC = 12 V)						
Output Impedance, Sourcing Current	(V_{BST} – V_{SW}) = 12 V			2.0	3.5	Ω
Output Impedance, Sinking Current	(V_{BST} – V_{SW}) = 12 V			1.0	2.0	Ω
DRVH Rise Time	V_{CC} = 12 V, 3 nF load, (V_{BST} – V_{SW}) = 12 V	tr_{DRVH}		16	30	ns
DRVH Fall Time	V_{CC} = 12 V, 3 nF load, (V_{BST} – V_{SW}) = 12 V	tf_{DRVH}		11	25	ns
DRVH Turn−Off Propagation Delay	C_{load} = 3 nF, [PWM = PWM_{LO}] to [V_{DRVH} = 90%]	$tpdl_{DRVH}$	8		30	ns
DRVH Turn−On Propagation Delay	C_{load} = 3 nF, [V_{DRVL} = 1 V] to [V_{DRVH}−V_{SW} = 10%]	$tpdh_{DRVH}$			30	ns
SW Pull−down Resistance	SW to PGND			37.5		kΩ
DRVH Pull−down Resistance	DRVH to SW, (V_{BST} – V_{SW}) = 0 V			37.5		kΩ
HIGH−SIDE DRIVER (VCC = 5 V)						
Output Impedance, Sourcing Current	(V_{BST} – V_{SW}) = 5 V			2.5		Ω
Output Impedance, Sinking Current	(V_{BST} – V_{SW}) = 5 V			1.6		Ω
DRVH Rise Time	V_{CC} = 5 V, 3 nF load, (V_{BST} – V_{SW}) = 5 V	tr_{DRVL}		30		ns
DRVH Fall Time	V_{CC} = 5 V, 3 nF load, (V_{BST} – V_{SW}) = 5 V	tf_{DRVL}		27		ns
DRVH Turn−Off Propagation Delay	C_{LOAD} = 3 nF, [PWM = PWM_{LO}] to [V_{DRVH} = 90%]	$tpdl_{DRVL}$		20		ns
DRVH Turn−On Propagation Delay	C_{LOAD} = 3 nF, [V_{DRVL} = 1 V] to [V_{DRVH}−V_{SW} = 10%]	$tpdh_{DRVL}$		27		ns
SW Pull−down Resistance	SW to PGND			37.5		kΩ

Table 5. ELECTRICAL CHARACTERISTICS VCC = 4.5 V to 13.2 V, BST−SW = 4.5 V to 13.2 V, BST = 4.5 V to 30 V, SW = 0 V to 21 V; for typical values T_A = 25°C, for min/max values T_A = −10°C to 125°C; unless otherwise noted. (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
HIGH−SIDE DRIVER (VCC = 5 V)						
DRVH Pull−down Resistance	DRVH to SW, (V_{BST} – V_{SW}) = 0 V			37.5		kΩ
LOW−SIDE DRIVER (VCC = 12 V)						
Output Impedance, Sourcing Current	V_{CC} = 12 V			2.0	3.5	Ω
Output Impedance, Sinking Current	V_{CC} = 12 V			0.7	1.8	Ω
DRVL Rise Time	V_{CC} = 12 V, C_{LOAD} = 3 nF	tr_{DRVL}		16	35	ns
DRVL Fall Time	V_{CC} = 12 V, C_{LOAD} = 3 nF	tf_{DRVL}		11	20	ns
DRVL Turn−Off Propagation Delay	C_{LOAD} = 3 nF, [PWM = PWM_{HI}] to [V_{DRVL} = 90%]	$tpdl_{DRVL}$			35	ns
DRVL Turn−On Propagation Delay	C_{LOAD} = 3 nF, [V_{DRVH}−V_{SW}] = 1 V to [V_{DRVL} = 10%]	$tpdh_{DRVL}$	8		30	ns
DRVL Pull−down Resistance	DRVL to GND, VCC = GND			37.5		kΩ
LOW−SIDE DRIVER (VCC = 5 V)						
Output Impedance, Sourcing Current	V_{CC} = 5 V			2.5		Ω
Output Impedance, Sinking Current	V_{CC} = 5 V			1.0		Ω
DRVL Rise Time	V_{CC} = 5 V, C_{LOAD} = 3 nF	tr_{DRVL}		30		ns
DRVL Fall Time	V_{CC} = 5 V, C_{LOAD} = 3 nF	tf_{DRVL}		22		ns
DRVL Turn−Off Propagation Delay	C_{LOAD} = 3 nF, [PWM = PWM_{HI}] to [V_{DRVL} = 90%]	$tpdl_{DRVL}$		27		ns
DRVL Turn−On Propagation Delay	C_{LOAD} = 3 nF, [V_{DRVH}−V_{SW} = 1 V] to [V_{DRVL} = 10%]	$tpdh_{DRVL}$		12		ns
DRVL Pull−down Resistance	DRVL to GND, VCC = GND			37.5		kΩ
EN INPUT						
Enable Voltage High		EN_{HI}	2.0			V
Enable Voltage Low		EN_{LO}			1.0	V
Hysteresis				500		mV
Normal Bias Current			−1		1	μA
Enable Pin Sink Current			4		30	mA
EN High Propagation Delay Time	PWM = 0 V, EN going from 0 V to EN_{HI} to DRVL rising to 10%	tpd_{EN_HI}			60	μs
SWITCH NODE						
SW Node Leakage Current					20	μA
Zero Cross Detection Threshold Voltage	Ramp slowly until DRVL goes off (start in DCM mode)			−3		mV

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at TJ = TA = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Values based on design and/or characterization.

Table 6. ZCD DECODER TRUTH TABLE

PWM Input	ZCD	DRVL	DRVH
PWM High	ZCD Reset	Low	High
PWM Mid (positive current)	Positive current through the inductor	High	Low
PWM Mid (negative current)	Zero current through the inductor (after ZCD blanking timer)	Low	Low
PWM Low	ZCD Reset	High	Low

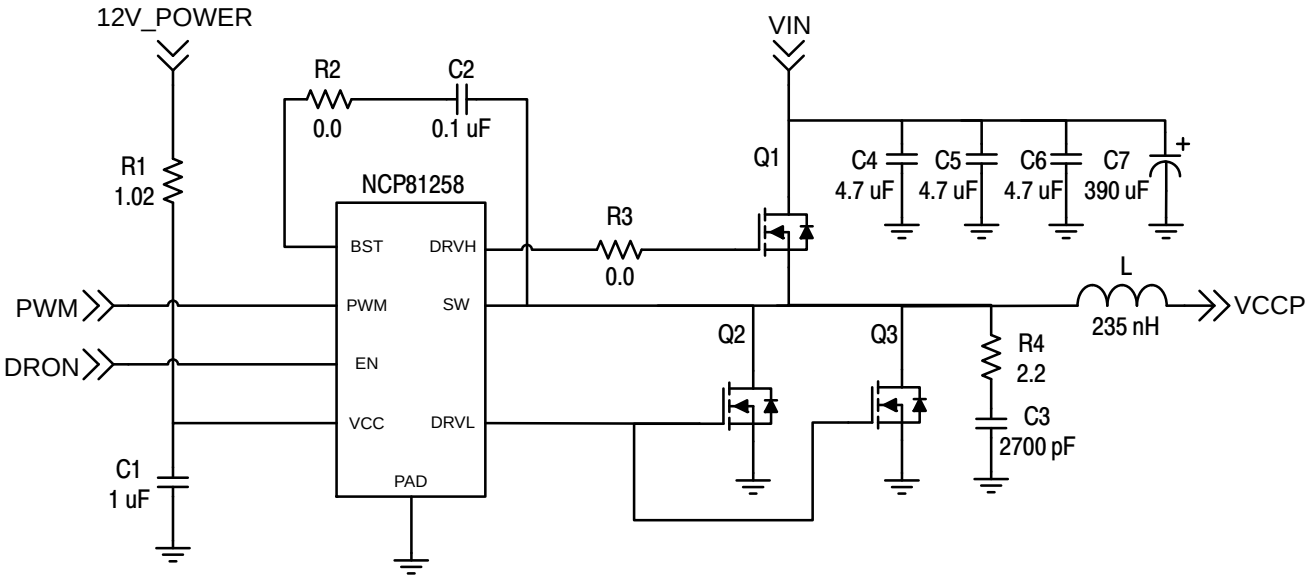


Figure 2. Application Circuit

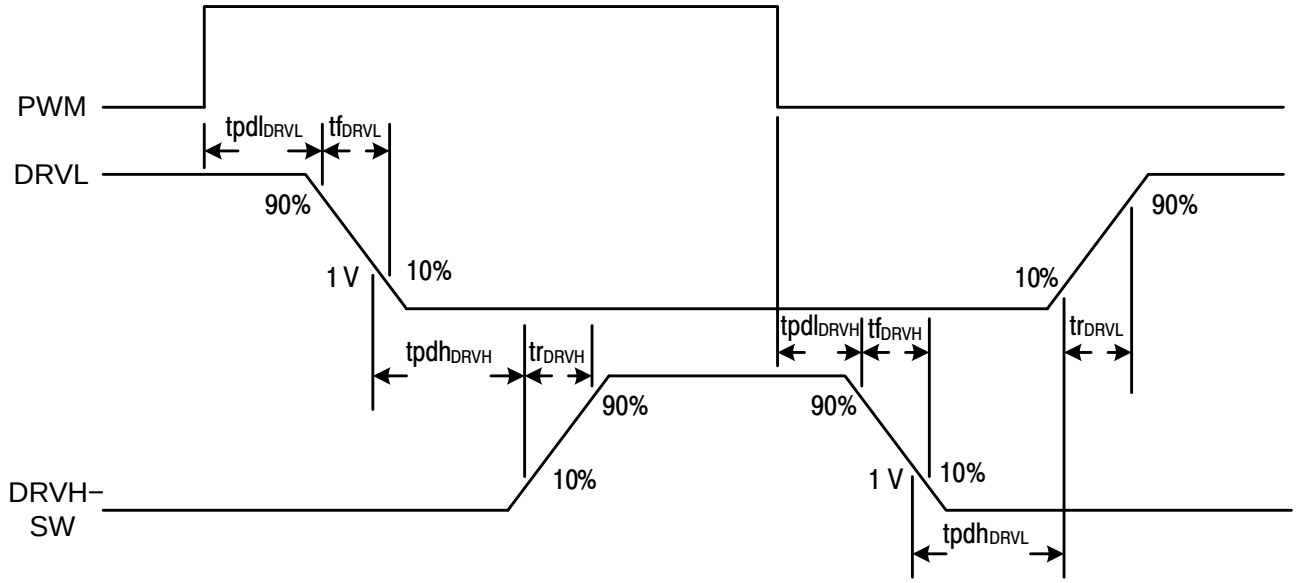


Figure 3. Gate Timing Diagram

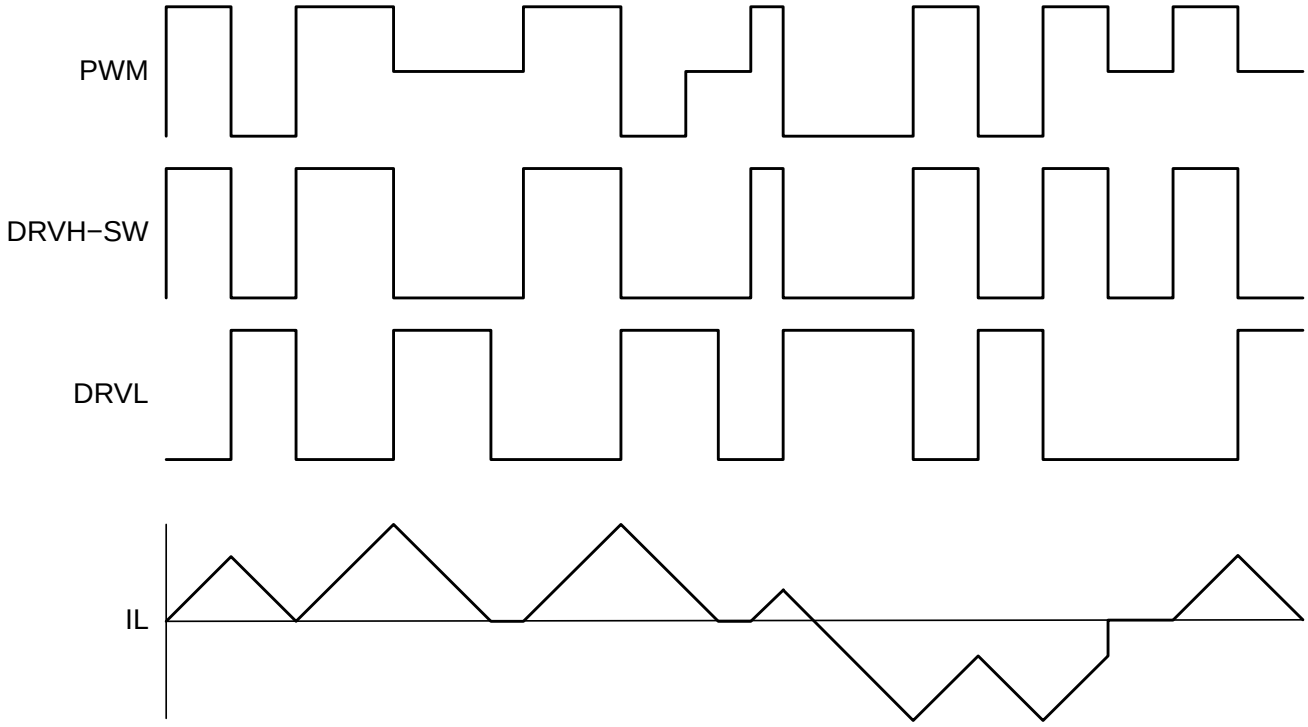


Figure 4. PWM/EN Logic Diagram

APPLICATIONS INFORMATION

The NCP81258 gate driver is a single−phase MOSFET driver designed for driving N−channel MOSFETs in a synchronous buck converter topology.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low−$R_{DS(on)}$ N−channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCC and GND pins.

High−Side Driver

The high−side driver is designed to drive a floating low−$R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor. When the NCP81258 is starting up, the SW pin is held at ground, allowing the bootstrap capacitor to charge up to VCC through the bootstrap diode. When the PWM input is driven high, the high−side driver will turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SW pin rises. When the high−side MOSFET is fully turned on, SW will settle to VIN, and BST will settle to VIN + VCC (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the high−side driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used for C_{BST}.

Power Supply Decoupling

The NCP81258 can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage, a low−ESR capacitor should be placed near the VCC and GND pins. A MLCC between 1 μF and 4.7 μF is typically used.

Undervoltage Lockout

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. Once VCC reaches this threshold, the PWM signal will control DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull−down resistors on DRVH, DRVL and SW to prevent the gates of the MOSFETs from accumulating enough charge to turn on when the driver is powered off.

Pre−Overvoltage Protection

The pre−Overvoltage Protection (pre−OVP) feature is used to protect the load if there is a short across the high−side FET. When VCC is greater than 2.75 V, the voltage on SW is monitored. During startup, if SW is determined to be greater than Output Overvoltage Trip Threshold, DRVL will be latched high to turn on the synchronous FET and provide a path from VIN to ground. This also pulls the EN pin low. To exit this behavior, power to the driver must be turned off (VCC less than V_{UVLO} minus V_{UVLO_HYS}) and then VCC powered back on. When VCC rises above V_{UVLO} and EN is

above EN_{HI}, the gate driver enters normal PWM operation if SW is no longer above the Output Overvoltage Trip Threshold.

Bi−Directional EN Signal

The Enable pin (EN) is used to disable the DRVH and DRVL outputs to prevent power transfer. When EN is above the EN_{HI} threshold, DRVH and DRVL change their states according to the PWM input. A UVLO fault turns on the internal MOSFET that pulls the EN pin towards ground. By connecting EN to the DRON pin of a controller, the controller is alerted when the driver encounters a fault condition.

Every time EN is brought from a low to a high state, the NCP81258 conducts an auto−calibration cycle on the ZCD SW threshold. During the auto−calibration cycle, the driver outputs are prevented from responding to the PWM input, and both outputs are in the low state. This auto−calibration cycle is guaranteed to complete by 60 μs.

Three−State PWM Input

Switching PWM between logic−high and logic−low states will allow the driver to operate in continuous conduction mode as long as VCC is greater than the UVLO threshold and EN is high. The threshold limits are specified in the electrical characteristics table in this datasheet. Refer to Figure 21 for the gate timing diagrams and Table 1 for the EN/PWM logic table.

When PWM is set above PWM_{HI}, DRVL will first turn off after a propagation delay of $tpdl_{DRVL}$. To ensure non−overlap between DRVL and DRVH, there is a delay of $tpdh_{DRVH}$ from the time DRVL falls to 1 V, before DRVH is allowed to turn on.

When PWM falls below PWM_{LO}, DRVH will first turn off after a propagation delay of $tpdl_{DRVH}$. To ensure non−overlap between DRVH and DRVL, there is a delay of $tpdh_{DRVL}$ from the time DRVH – SW falls to 1 V, before DRVL is allowed to turn on.

When PWM enters the mid−state voltage range, PWM_{MID}, DRVL goes high after the non−overlap delay, and stays high for the duration of the ZCD blanking timer and an 80 ns de−bounce timer. Once these timers expire, SW is monitored for zero current detection and pulls DRVL low once zero current is detected.

Thermal Considerations

As power in the NCP81258 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP81258 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCP81258 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, the NCP81258, soldered on to a 645 mm^2 copper area, using 1 oz. copper and FR4, can dissipate up to 2.3 W when the ambient temperature (T_A) is 25°C. The power dissipated by the NCP81258 can be calculated from the following equation:

$$P_D \approx VCC \times \left[\left(n_{HS} \times Qg_{HS} + n_{LS} \times Qg_{LS}\right) \times f + I_{standby}\right] \qquad \text{(eq. 2)}$$

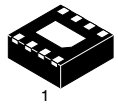
Where n_{HS} and n_{LS} are the number of high−side and low−side FETs, respectively, Qg_{HS} and Qg_{LS} are the gate charges of the high−side and low−side FETs, respectively and *f* is the switching frequency of the converter.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

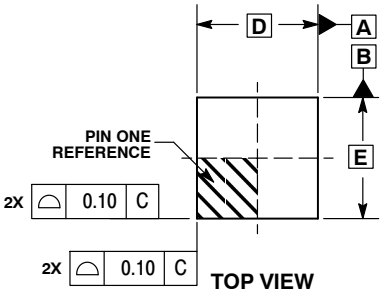
ON Semiconductor®

DFN8 2x2, 0.5P
CASE 506AA−01
ISSUE E

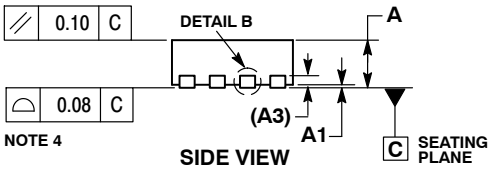
DATE 22 JAN 2010



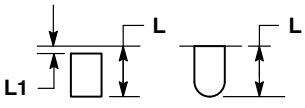
SCALE 4:1



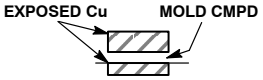
TOP VIEW



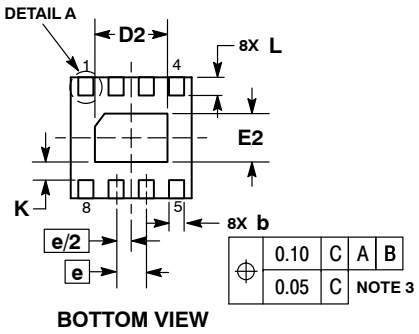
SIDE VIEW



DETAIL A
OPTIONAL CONSTRUCTIONS



DETAIL B
OPTIONAL CONSTRUCTION

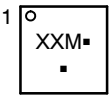


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	−−−	0.10

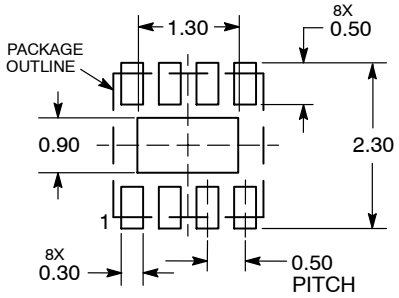
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON18658D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN8, 2.0X2.0, 0.5MM PITCH**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊