NCP81168

VR12.5 Compatible Synchronous Buck MOSFET Driver

The NCP81168 is a high performance MOSFET Driver for a Synchronous Buck converter with integrated bootstrap diode, zero current detect (ZCD), and UVLO into a compact 2x2 DFN8.

Adaptive anti−cross−conduction and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook systems. Additionally, the NCP81168 integrated solution greatly reduces package parasitic and board space compared to a discrete solution.

Features

- Switching frequency of up to 500 kHz
- Adaptive Anti−Cross−Conduction Circuit
- Output Disable Control Turn−Off Both MOSFETs
- Compatible with 3.3 V or 5 V PWM input, with Tri−State
- ZCD for improving Light Load Efficiency
- Internal Bootstrap Diode
- VCC Under Voltage Lockout
- Thermal Enhanced Package
- This is a Pb−Free Device

Typical Applications

- Notebook

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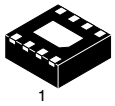
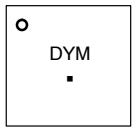


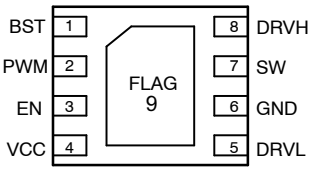
DFN8
CASE 506AA

MARKING DIAGRAM



DY = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81168MNTBG	DFN8 (Pb−Free)	3000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

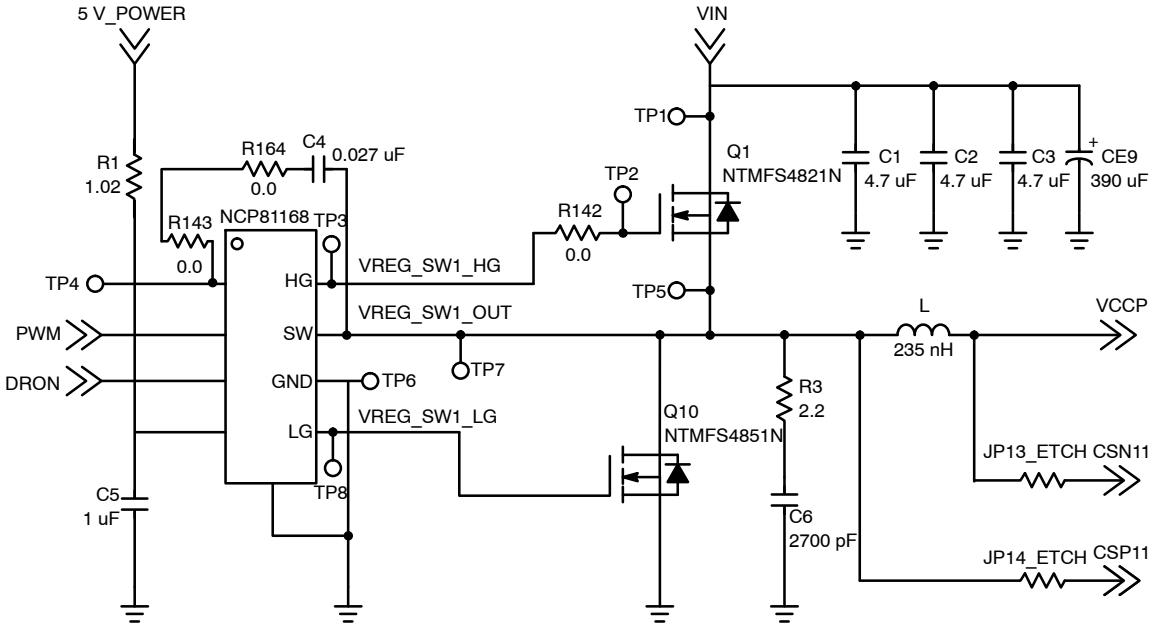


Figure 1. Typical Application Schematic

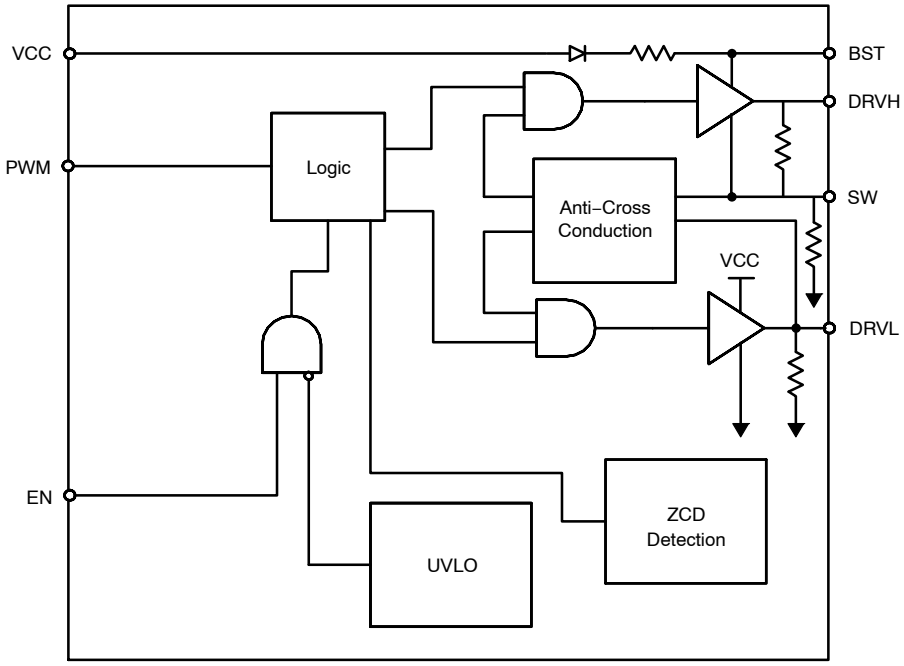


Figure 2. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BST	Bootstrap supply voltage. Connect a MLCC capacitor of at least 0.1 mF from this pin to SW.
2	PWM	Tristate Input.
3	EN	Enable. There is an internal pull−down resistor.
4	VCC	5.0 V power supply for the control logic circuit.
5	DRVL	Low−side gate drive output. Connect to the gate of low−side MOSFET.
6	GND	Analog Ground.
7	SW	Switch−node Output.
8	DRVH	High−side gate drive output. Connect to the gate of high−side MOSFET.
9	FLAG	Thermal Flag. Connect to ground plane.

Table 2. ABSOLUTE MAXIMUM RATINGS (Electrical Information - all signals referenced to GND unless noted otherwise.)

Pin Name	Min	Max	Unit
VCC	−0.3	7	V
BST (DC)	−0.3	35	V
BST (< 50 ns)	−0.3	40	V
SW (DC)	−5	35	V
SW (< 50 ns)	−10	40	V
DRVH	−0.3 wrt/SW −2 (< 200 ns) wrt/SW	BST+0.3	V
DRVL	−0.3	V_{VCC} + 0.3	V
All other pins	−0.3	V_{VCC} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance (Note 1)	$R_{\theta JA}$	119	°C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level − QFN Package	MSL	1	

NOTE: These devices have limited built-in ESD protection. The devices should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the device.

1. Test board conditions: 1 inches × 1 inches Cu, 1 oz. thickness

Table 4. ELECTRICAL CHARACTERISTICS

(V_{VCC} = 4.5 - 5.5 V, V_{BST} - V_{SW} = 4.5 - 5.5 V, V_{EN} = 5.0 V, C_{VCC} = 0.1 μF unless specified otherwise). Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC						
Operating Voltage	V_{VCC}	EN = 5 V, PWM = 500 kHz	4.5	–	5.5	V
Operating Current		I_{CC} + I_{BST}, EN = 5 V, PWM = 100 kHz, 3 nF load for DRVH and DRVL	–	2	4	mA
Enabled Current, No Switching		I_{CC} + I_{BST}, EN = 5 V, PWM = 0 V, no load for DRVH and DRVL	–	0.9	–	mA
		I_{CC} + I_{BST}, EN = 5 V, PWM = 5 V, no load for DRVH and DRVL	–	1.1	–	mA
Disabled Current		I_{CC} + I_{BST}, EN = 0 V	–	0.3	1.4	μA
UVLO Threshold	V_{UVLO}	VCC rising	3.8	4.35	4.5	V
UVLO Hysteresis			150	200	250	mV
EN INPUT						
Input Voltage High			3.3	–	–	V
Input Voltage Mid			1.35	–	1.8	V
Input Voltage Low			–	–	0.6	V
Input Bias Current			−1	–	1.0	μA
Propagation Delay Time		EN and DRVH Falling	–	14	40	ns
ZCD_EN						
ZCD Blanking + De−Bounce Timer	t_{blank}		–	350	–	ns
PWM INPUT						
Input High Voltage	V_{PWM_HI}		3.4	–	–	V
Input Mid Voltage	V_{PWM_MID}		1.3	–	2.7	V
Input Low Voltage	V_{PWM_LO}		–	–	0.7	V
DRVH						
Output Impedance, Sourcing Current		V_{BST}−V_{WS} = 5 V	–	0.7	1.2	Ω
Output Impedance, Sinking Current		V_{BST}−V_{WS} = 5 V	–	0.5	1.2	Ω
Rise Time	t_{rDRVH}	3 nF Load	–	15	25	ns
Fall Time	t_{fDRVH}	3 nF Load	–	10	25	ns
Turn-Off Propagation Delay	$tpdl_{DRVH}$	3 nF Load	10	–	30	ns
Turn-On Propagation Delay	$tpdh_{DRVH}$	3 nF Load	10	–	40	ns
DRVH Pulldown Resistance		From DRVH to SW	–	45	–	kΩ
DRVL						
Output Impedance, Sourcing Current			–	0.8	1.3	Ω
Output Impedance, Sinking Current			–	0.3	1.0	Ω
Rise Time	t_{rDRVL}	3 nF Load	–	18	25	ns
Fall Time	t_{fDRVL}	3 nF Load	–	9	15	ns
Turn-Off Propagation Delay	$tpdl_{DRVL}$	3 nF Load	10	–	30	ns
Turn-On Propagation Delay	$tpdh_{DRVL}$	3 nF Load	5	–	25	ns
DRVH Pulldown Resistance		From DRVH to SW	–	45	–	kΩ

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = 4.5 - 5.5 V, V_{BST} - V_{SW} = 4.5 - 5.5 V, V_{EN} = 5.0 V, C_{VCC} = 0.1 μF unless specified otherwise). Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SW						
SW Node Leakage Current			–	–	20	μA
SW Pulldown Resistance		SW to GND	–	45	–	kΩ
BOOTSTRAP DIODE						
Forward Voltage	V_F	V_{VCC} = 5 V, Forward Bias Current = 2.0 mA	0.1	0.4	0.6	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. TRUTH TABLE

State	EN	PWM	ZCD_EN	DRVH	DRVL
Chip Enabled	H	H	Reset	H	L
Chip Enabled	H	M	Positive Current through the Inductor	L	H
Chip Enabled	H	M	Zero Current through the Inductor	L	L
Chip Enabled	H	L	Reset	L	H
Chip Disabled	M	X	X	L	L

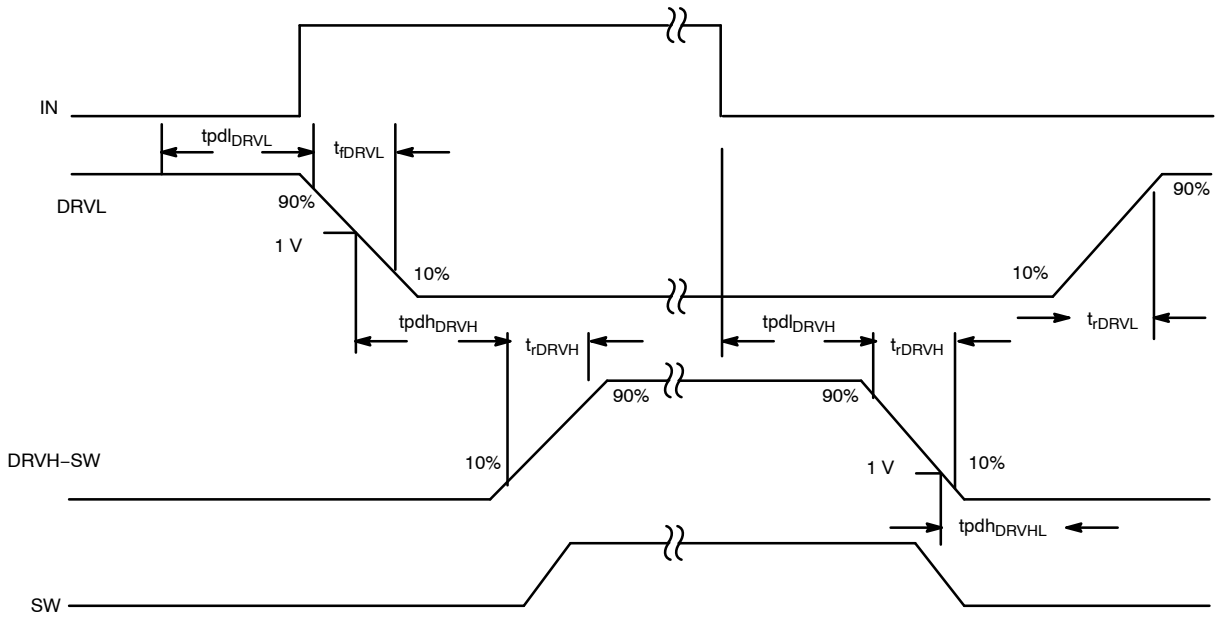


Figure 3. Timing Diagram

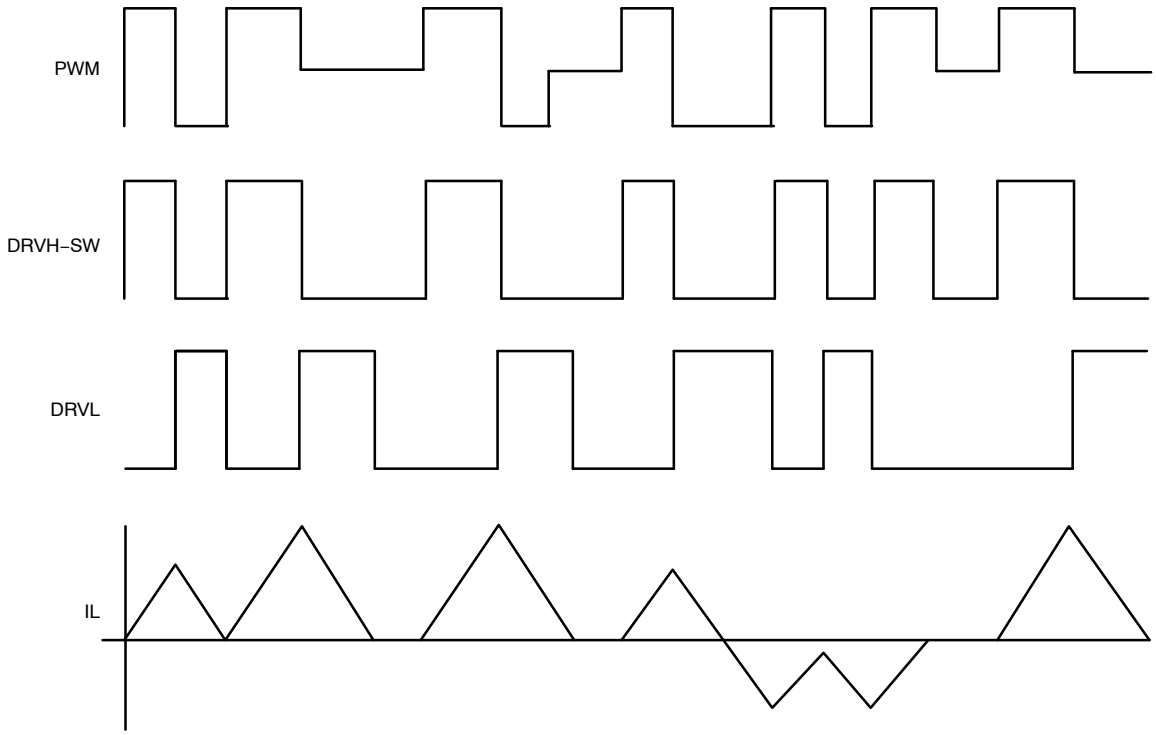


Figure 4. ZCD Behavior

APPLICATION INFORMATION

NCP81168 is a high performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a Synchronous Buck Converter. The NCP81168 supports numerous other functions such as ZCD, under−voltage lock−out (UVLO), and adaptive anti−cross−conduction circuit into a 2x2 DFN8 package.

High−Side Driver

The high−side driver drives an external N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of an internal diode and an external bootstrap capacitor. When the NCP81168 is starting up, the SW pin is at ground, so the bootstrap capacitor charges up to VCC through the bootstrap diode (see Figure 1). When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the voltage at the SW pin rises. When the high−side MOSFET is fully on, the SW voltage equals the VIN voltage, with the BST voltage higher than VCC by the amount of voltage on the bootstrap capacitor. The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Parasitic inductances and capacitances within the packaging and MOSFETs can cause significant ringing of the SW signal during turn−on and turn−off of the high−side MOSFET. When operating at high input voltages and high output currents, the peak ringing voltages on SW could cause the drain−to−source voltage across the MOSFETs to exceed its maximum rating. Including a resistor in series with the bootstrap capacitor can reduce the peak SWN ringing voltages. A resistor value of 4 Ω is recommended when operating at VIN voltages greater than 16 V.

Low−Side Driver

The low−side driver drives an external ground−referenced N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCC and GND.

Power Supply Decoupling

The NCP81168 SW pin sources relatively large currents across the drain−source of the MOSFETs. In order to maintain a constant and stable supply voltage (VCC) – a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi−layer ceramic capacitor (MLCC) should be placed between VCC pins and GND.

Overlap Protection Circuit

As PWM transitions between the logic high and logic low states, the driver circuitry prevents both MOSFETs from being on at the same time which could result in a damage to the device. The NCP81168 prevents cross−conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non−overlap (NOL) time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). The control circuitry monitors the gate−source voltage of both MOSFETs and the SW pin voltage in order to determine the conduction status of the MOSFETs. For example, when the PWM input is driven high, the gate−source voltage of the low−side MOSFET will

go low after a propagation delay. Then, the internal timer will turn−on and delay the turn−on of the high−side MOSFET. An important point to note is that the time it takes for both the MOSFETs to turn−off is dependent on the capacitance on the gate.

Three−State PWM Input

Switching PWM between logic−high and logic−low states allows the driver to operate in continuous conduction mode, as long as VCC is greater than the UVLO threshold and EN is high.

The PWM mid−state allows the NCP81168 to enter a high−impedance mode, where both MOSFETs are off.

Enable Input (EN)

The EN pin disables the high−side MOSFET – if the pin is pulled low. The pin has a pull−down resistance of 300 kΩ to force a disabled state when it is left unconnected. EN can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

EN is also used to alert the NCP81168 whether it exceeded its UVLO threshold or not. The EN pin has an open drain output that will pull down whenever NCP81168 is below its UVLO level (rising or falling). It will release once the UVLO has been exceeded and the part is done initializing.

VCC Under−Voltage Lockout (UVLO)

The VCC pin is monitored by an UVLO Circuit. When VCC voltage rises above the rising threshold − the NCP81168 is enabled.

Table 6. TRUTH TABLE

VCC	EN	Driver State
< UVLO	X	Disabled
> UVLO	L	Disabled
> UVLO	H	Enabled
> UVLO	Open	Disabled

Zero Current Detection

At light load conditions, the inductor current can be negative due to the inductor current ripple. The zero current detection (ZCD) function in the NCP81168 can prevent negative current during these light load conditions and thus leads to higher efficiency. When ZCD is active, the NCP81168 will monitor the voltage at the SW pins when the low−side MOSFET is turn−on. There is a blanking/ de−bounce timer that delays when this monitoring starts, from the time when gate−source voltage of low−side MOSFET goes high. As the inductor current falls towards zero, the voltage on SWN pins will become less negative. When the voltage on the SW pin reaches the ZCD threshold, the LS FET is turned off. Positive current can still flow through the body diode of the LS FET, but the body diode will block any current in the negative direction.

ZCD is activated by placing PWM in the mid−state. The ZCD behavior is explained as follows:

- PWM = High → HS FET is ON, LS FET is OFF
- PWM = Mid → HS FET is OFF, LS FET is OFF when zero current is detected
- PWM = Low → HS FET is OFF, LS FET is ON

PCB Layout Guidelines

PCB layout plays an important role to achieve optimal performance. For stable operation, follow these guidelines.

1. Place VCC decoupling capacitor close to the device. Connect GND at the point of VCC capacitor's ground connection.
2. Place as many GND vias as possible close to the GND pin to minimize thermal resistance.
3. Place BST resistor and capacitor as close to the BST and SW pins as possible in order to reduce ringing. Use trace width of 20 mils or higher to route the path.
4. Shorten the trace between MOSFET gate and driver output. This decreases inductance and should be as wide as possible to reduce resistance.

Typical Performance

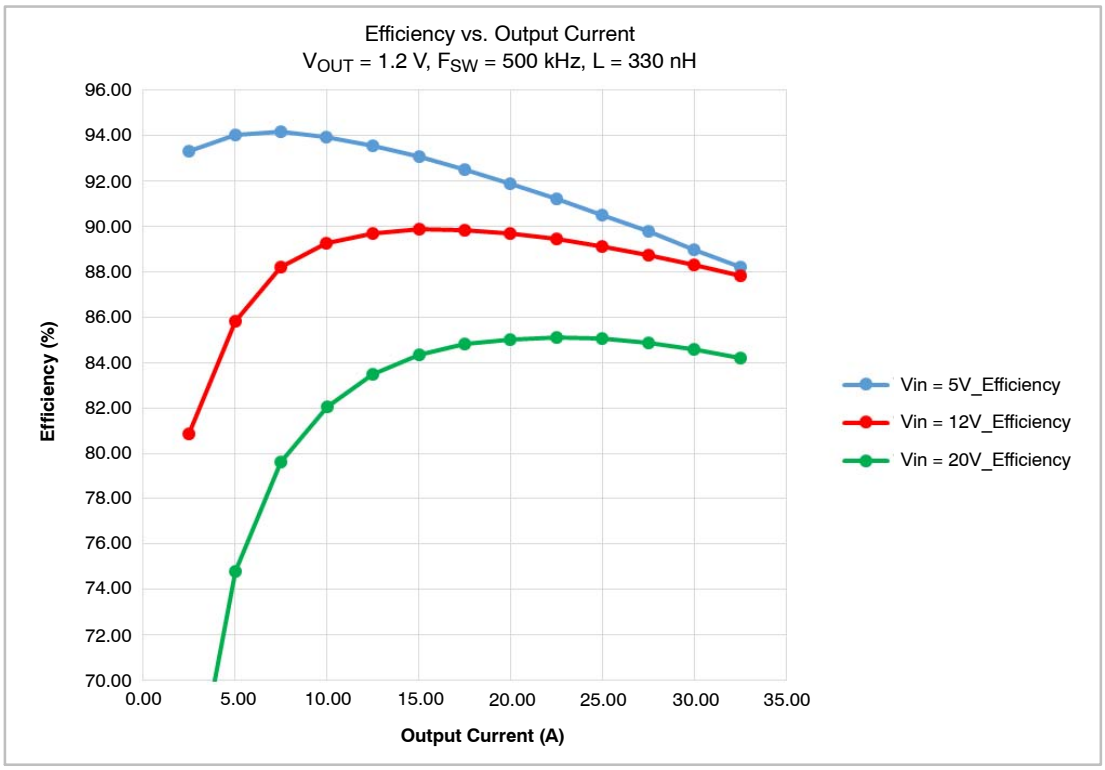


Figure 5. Efficiency vs. Output Current for different input voltages using dual NTMFD4C85N MOSFETs.

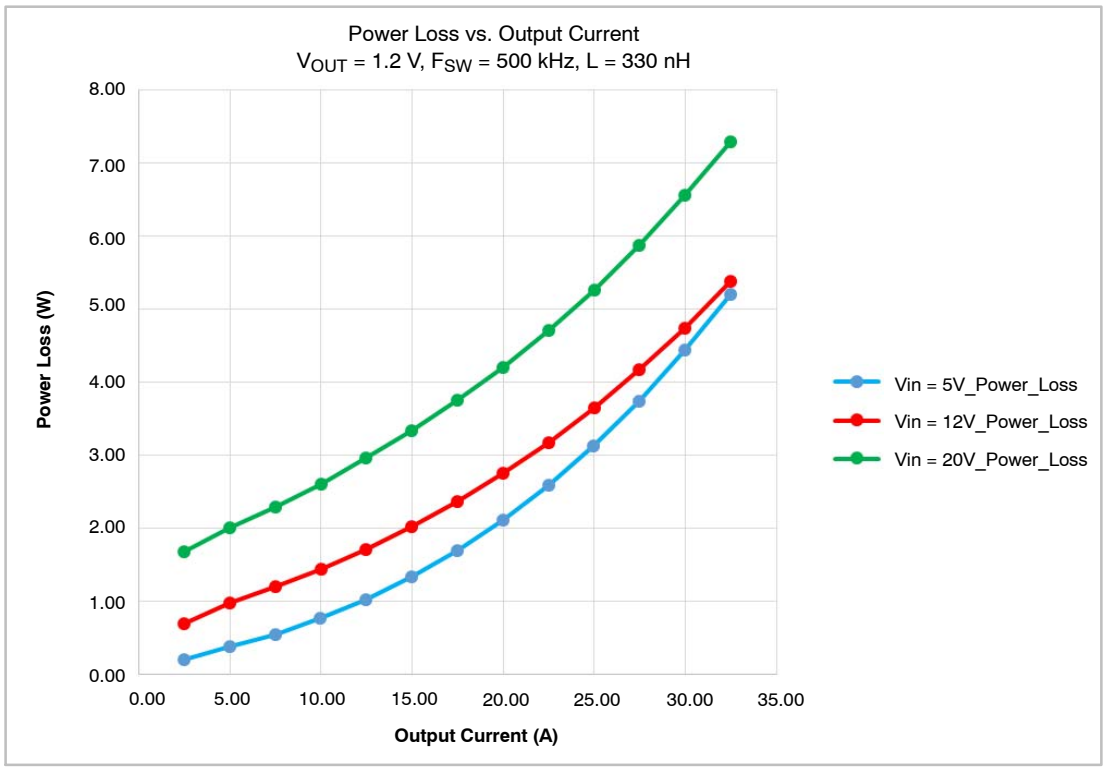
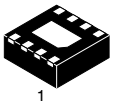


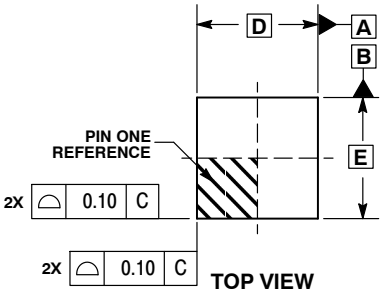
Figure 6. Power Loss vs. Output Current for different input voltages using dual NTMFD4C85N MOSFETs

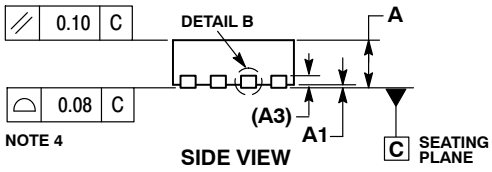
PACKAGE DIMENSIONS

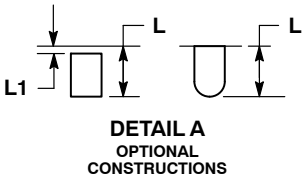
DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

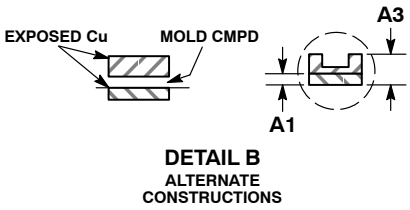


SCALE 4:1



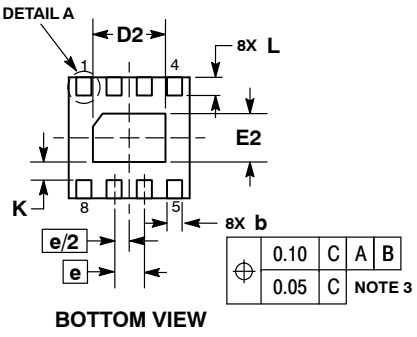




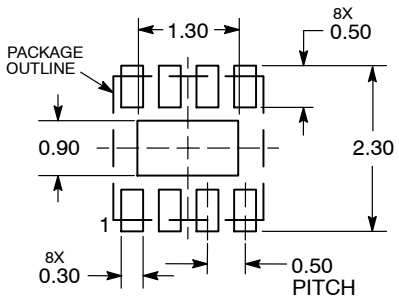


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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