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November 2013

# **FDP19N40**

# N-Channel UniFET<sup>TM</sup> MOSFET 400 V, 19 A, 240 m $\Omega$

#### **Features**

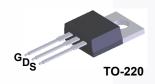
- $R_{DS(on)}$  = 200  $m\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 9.5 A
- Low Gate Charge (Typ. 32 nC)
- Low C<sub>rss</sub> (Typ. 20 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · RoHS Compliant

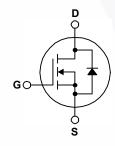
## **Applications**

- Lighting
- · Uninterruptible Power Supply
- · AC-DC Power Supply

# **Description**

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





# **MOSFET Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter		FDP19N40	Unit
$V_{DSS}$	Drain to Source Voltage			400	V
$V_{GSS}$	Gate to Source Voltage			±30	V
	Drain Current	- Continuous (T <sub>C</sub> = 25°C)		19	А
ID	Drain Current	- Continuous (T <sub>C</sub> = 100°C)		11.4	A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	76	Α
E <sub>AS</sub>	Single Pulsed Avalanche	Energy	(Note 2)	542	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	19	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (N		(Note 1)	21.5	mJ
dv/dt	Peak Diode Recovery dv	/dt	(Note 3)	15	V/ns
П	Dower Dissinction	(T <sub>C</sub> = 25°C)		215	W
$P_{D}$	Power Dissipation	- Derate Above 25°C		1.65	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Te	emperature Range		-55 to +150	°C
$T_L$	Maximum Lead Tempera	ture for Soldering, 1/8" from Case for	5 Seconds	300	°C

### **Thermal Characteristics**

Symbol	Parameter	FDP19N40	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. 62.5		-0/00

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP19N40	FDP19N40	TO-220	Tube	N/A	N/A	50 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	400	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C	-	0.5	-	V/°C
1	Zero Gate Voltage Drain Current	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μА
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 320 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 9.5 \text{ A}$	-	0.2	0.24	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 9.5 A	-	18.3	-	S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 05.V.V 0.V		-	1590	2115	pF
Coss	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz		-	255	340	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 101112	-	-\	20	29	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 320 V, I <sub>D</sub> = 19 A,		- \	32	40	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V	-	- \	10	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(	(Note 4)	-	13	-	nC

# **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	31	72	ns
t <sub>r</sub>		$V_{DD} = 200 \text{ V}, I_D = 19 \text{ A},$	-	70	150	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_G$ = 25 $\Omega$	-	82	174	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	49	108	ns

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	19	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	76	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 19 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 19 A,	-	349	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100 A/μs	-	3.56	-	μС

- 1: Repetitive rating: pulse-width limited by maximum junction temperature.
- 2: L = 3 mH,  $I_{AS}$  = 19 A,  $V_{DD}$  = 50 V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C. 3:  $I_{SD}$   $\leq$  19 A, di/dt  $\leq$  200 A/ $\mu$ s,  $V_{DD}$   $\leq$  BV $_{DSS}$ , starting  $T_{J}$  = 25°C.
- 4: Essentially independent of operating temperature typical characteristics.

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

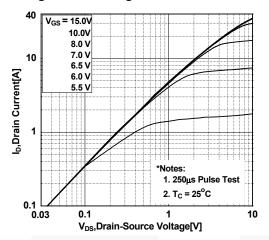


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

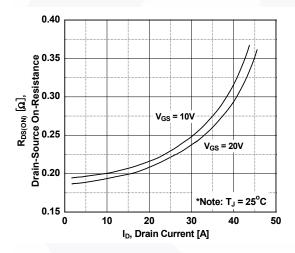


Figure 5. Capacitance Characteristics

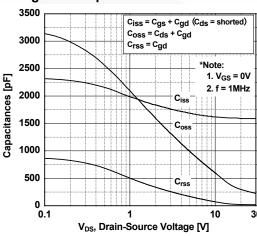


Figure 2. Transfer Characteristics

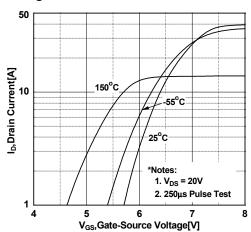


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

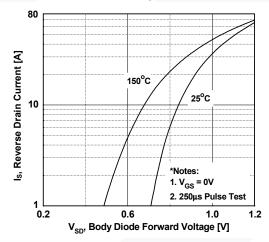
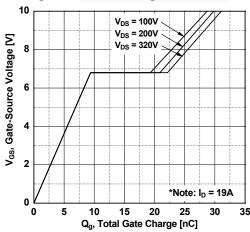


Figure 6. Gate Charge Characteristics



# **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

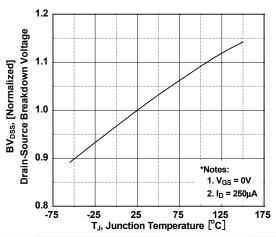


Figure 8. On-Resistance Variation vs. Temperature

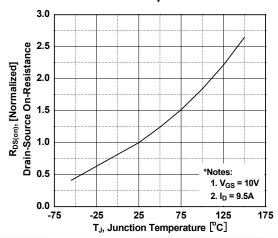


Figure 9. Maximum Safe Operating Area

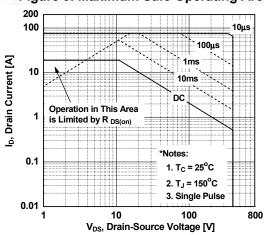


Figure 10. Maximum Safe Operating Area

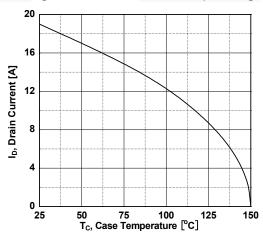
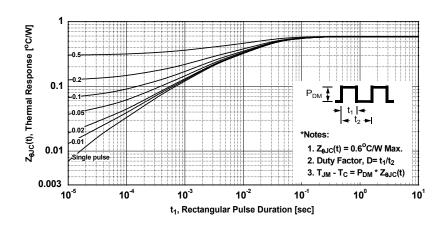


Figure 11. Transient Thermal Response Curve



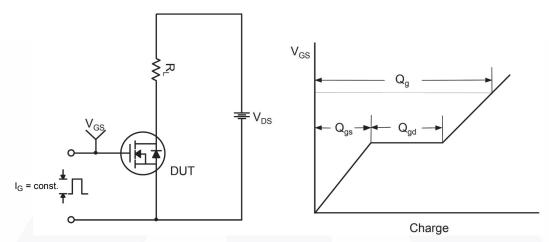


Figure 12. Gate Charge Test Circuit & Waveform

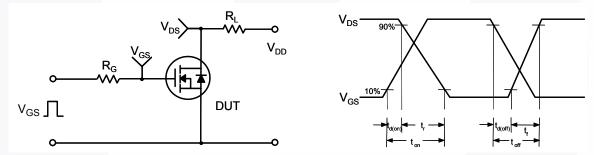


Figure 13. Resistive Switching Test Circuit & Waveforms

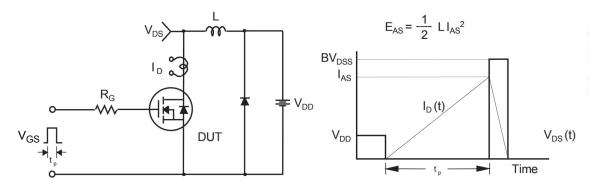


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

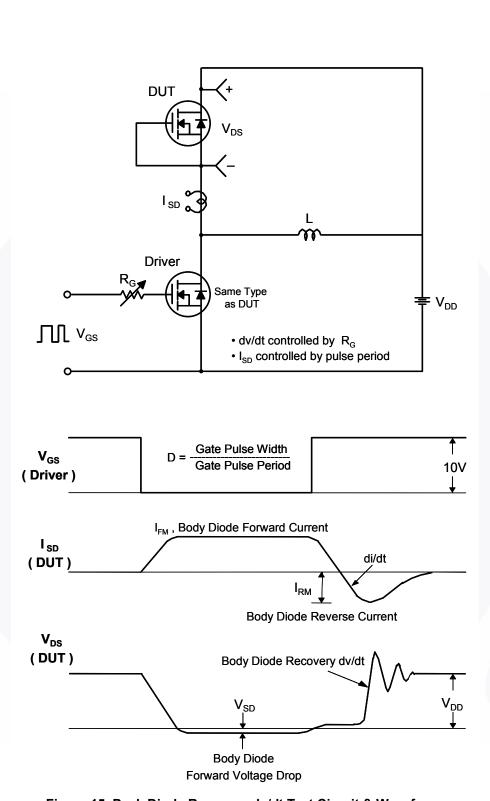


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

### **Mechanical Dimensions**

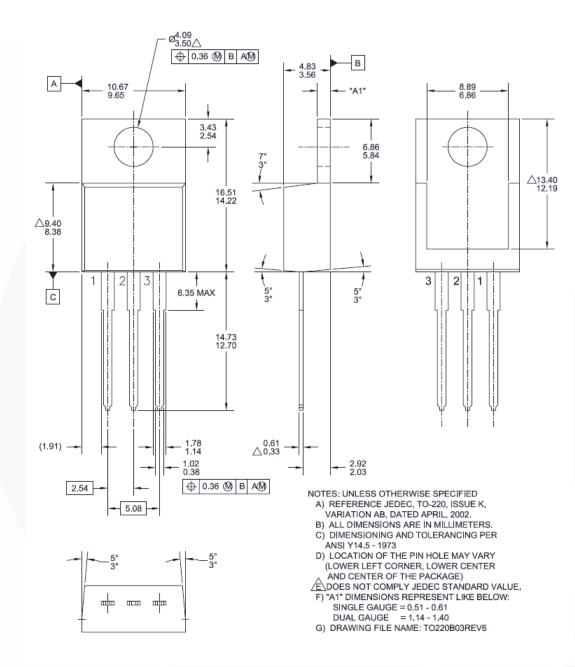


Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB

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