



FQPF5P20

P-Channel QFET[®] MOSFET

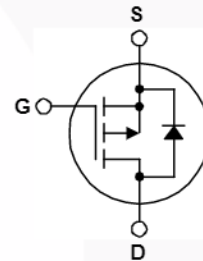
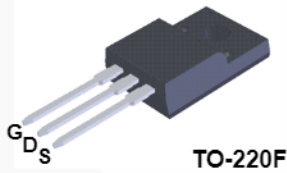
-200 V, -3.4 A, 1.4 Ω

Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -3.4 A, -200 V, $R_{DS(on)} = 1.4 \Omega$ (Max.) @ $V_{GS} = -10 V$, $I_D = -1.7 A$
- Low Gate Charge (Typ. 10 nC)
- Low C_{rss} (Typ. 12 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQPF5P20 FQPF5P20RDTU	Unit
V_{DSS}	Drain-Source Voltage	-200	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ C$)	-3.4
		- Continuous ($T_C = 100^\circ C$)	-2.15
I_{DM}	Drain Current - Pulsed (Note 1)	-13.6	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	330	mJ
I_{AR}	Avalanche Current (Note 1)	-3.4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	3.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-5.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ C$) - Derate Above $25^\circ C$	38	W
		0.3	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	FQPF5P20 FQPF5P20RDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	3.29	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQPF5P20	FQPF5P20	TO-220F	Tube	N/A	N/A	50 units
FQPF5P20RDTU	FQPF5P20	TO-220F (LG-formed)	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	--	-0.17	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	μA
		$V_{DS} = -160\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.7\text{ A}$	--	1.1	1.4	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -1.7\text{ A}$	--	2.15	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	330	430	pF
C_{oss}	Output Capacitance		--	75	98	pF
C_{riss}	Reverse Transfer Capacitance		--	12	15	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -100\text{ V}, I_D = -4.8\text{ A},$ $R_G = 25\ \Omega$	--	9	28	ns	
t_r	Turn-On Rise Time		--	70	150	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	12	35	ns
t_f	Turn-Off Fall Time		(Note 4)	--	25	60	ns
Q_g	Total Gate Charge	$V_{DS} = -160\text{ V}, I_D = -4.8\text{ A},$ $V_{GS} = -10\text{ V}$	--	10	13	nC	
Q_{gs}	Gate-Source Charge		(Note 4)	--	2.8	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	5.2	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	-3.4	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-13.6	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -3.4\text{ A}$	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -4.8\text{ A},$	--	175	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	1.07	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. $L = 42.8\text{ mH}, I_{AS} = -3.4\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq -4.8\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

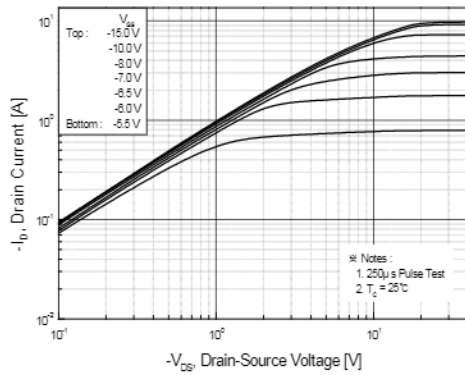


Figure 1. On-Region Characteristics

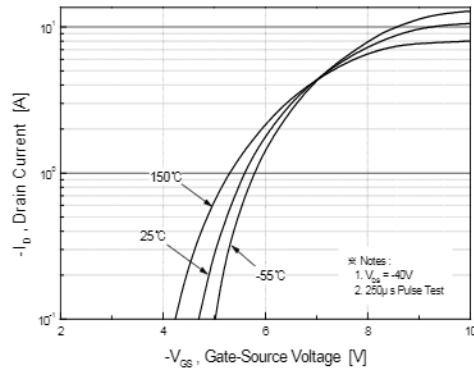


Figure 2. Transfer Characteristics

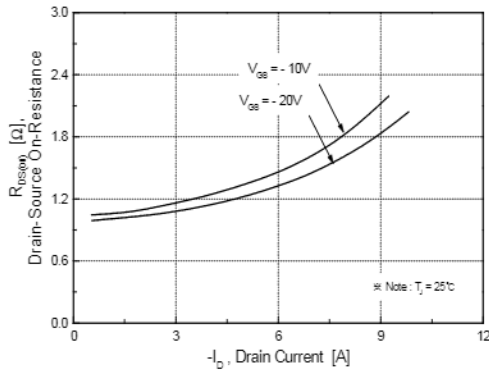


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

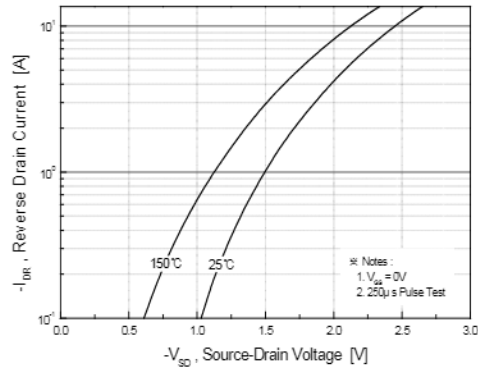


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

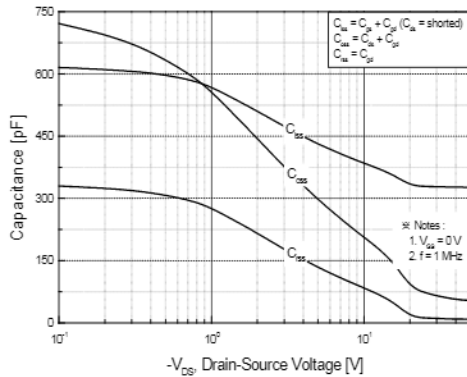


Figure 5. Capacitance Characteristics

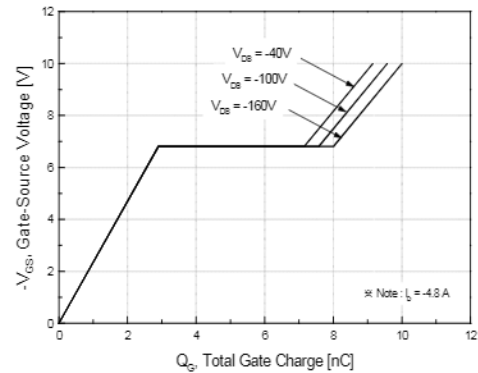


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

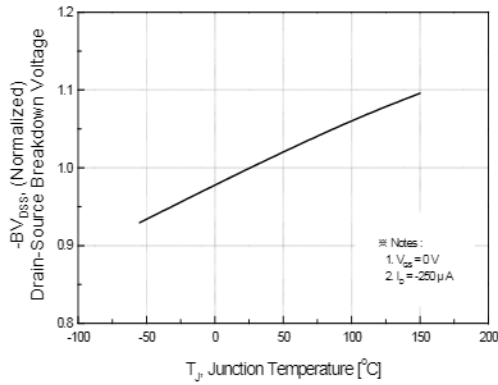


Figure 7. Breakdown Voltage Variation vs. Temperature

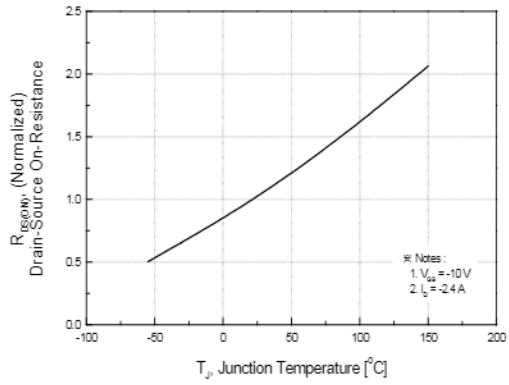


Figure 8. On-Resistance Variation vs. Temperature

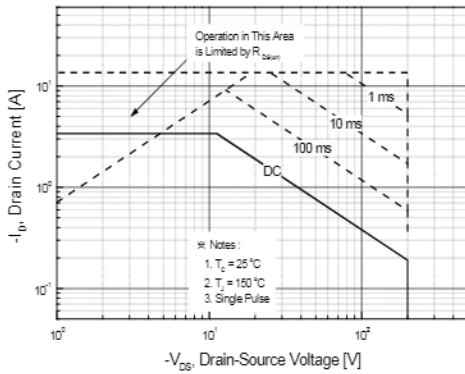


Figure 9. Maximum Safe Operating Area

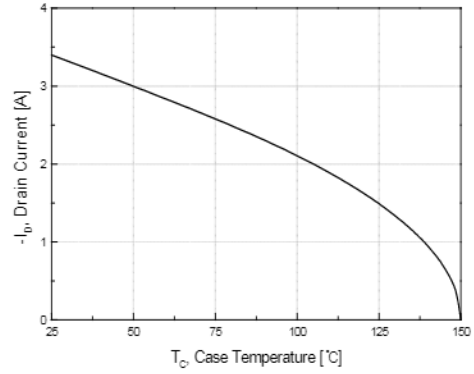


Figure 10. Maximum Drain Current vs. Case Temperature

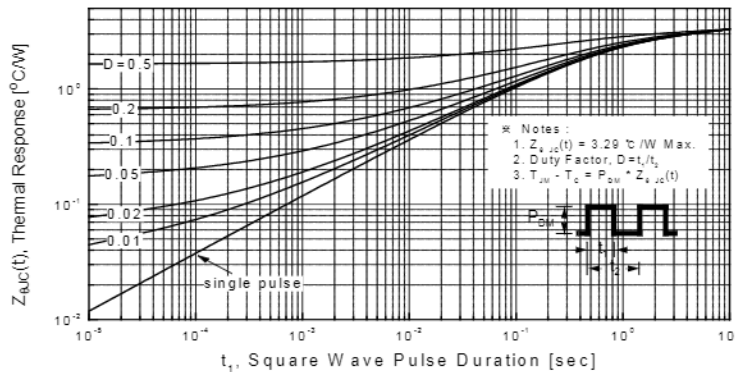


Figure 11. Transient Thermal Response Curve

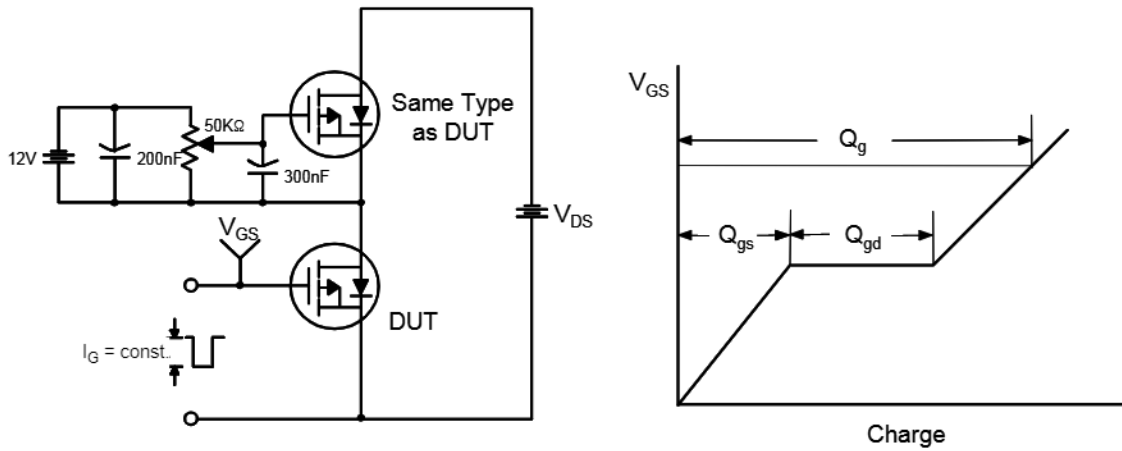


Figure 12. Gate Charge Test Circuit & Waveform

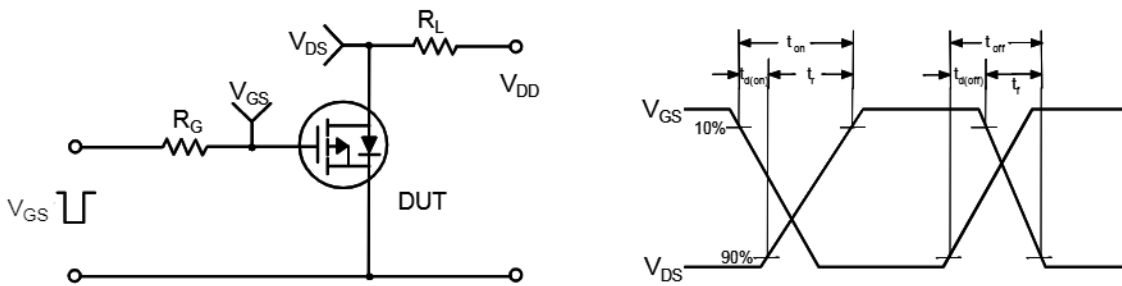


Figure 13. Resistive Switching Test Circuit & Waveforms

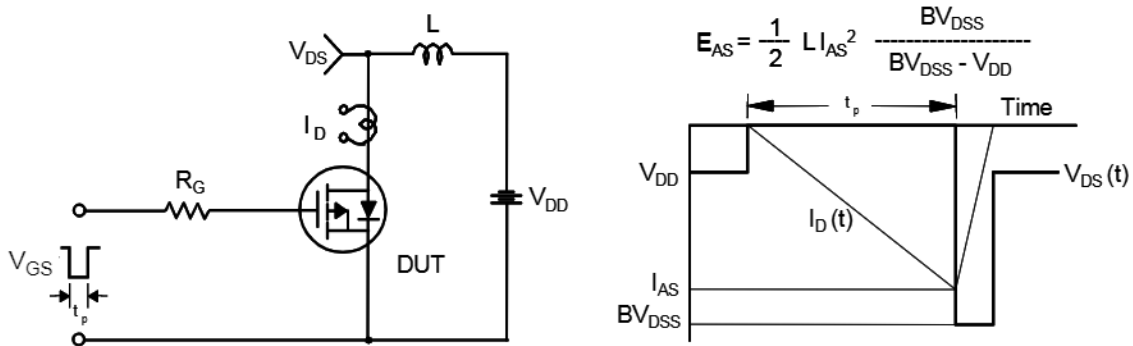
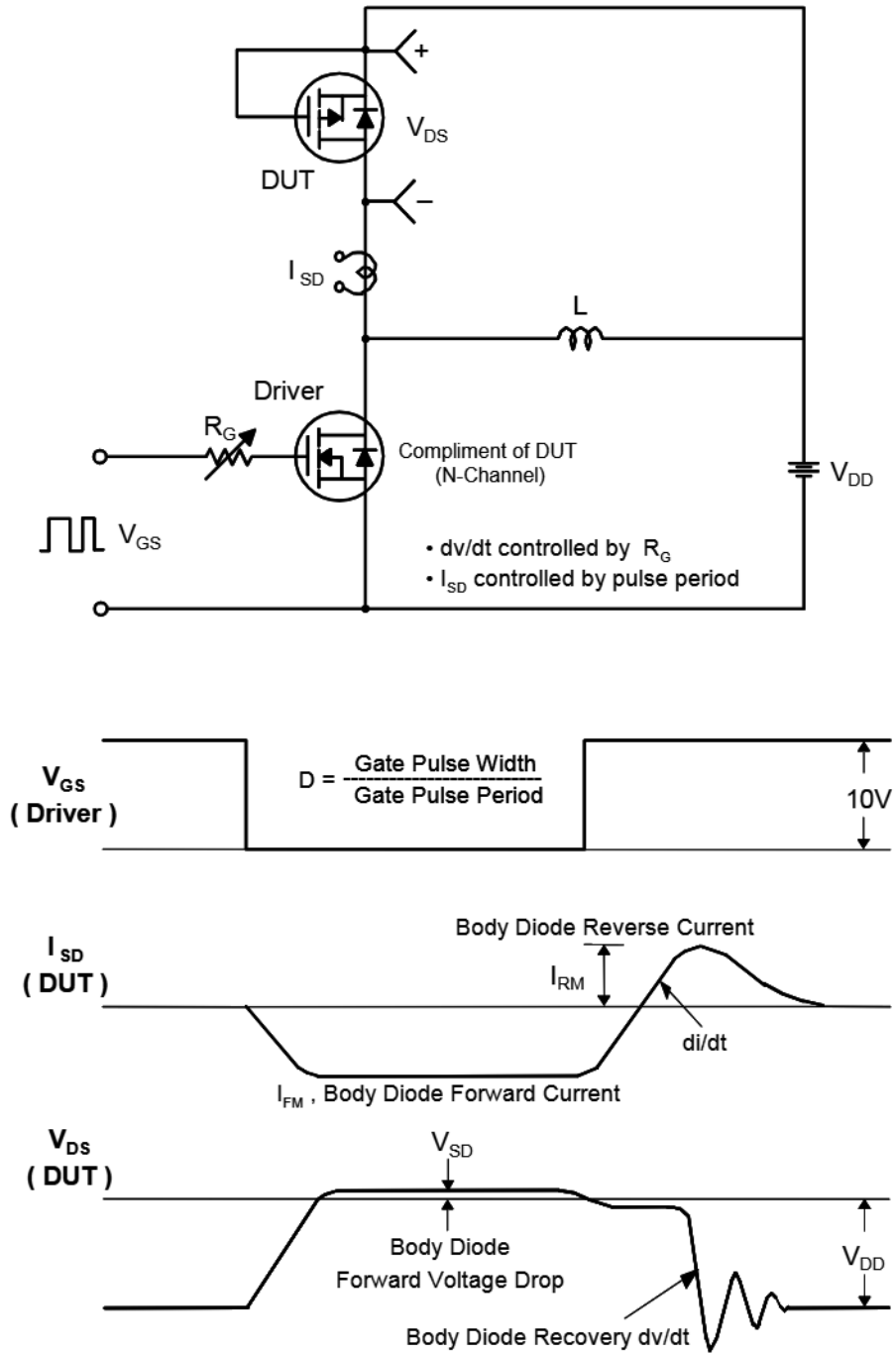


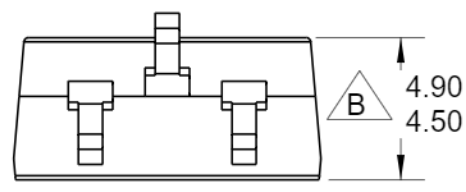
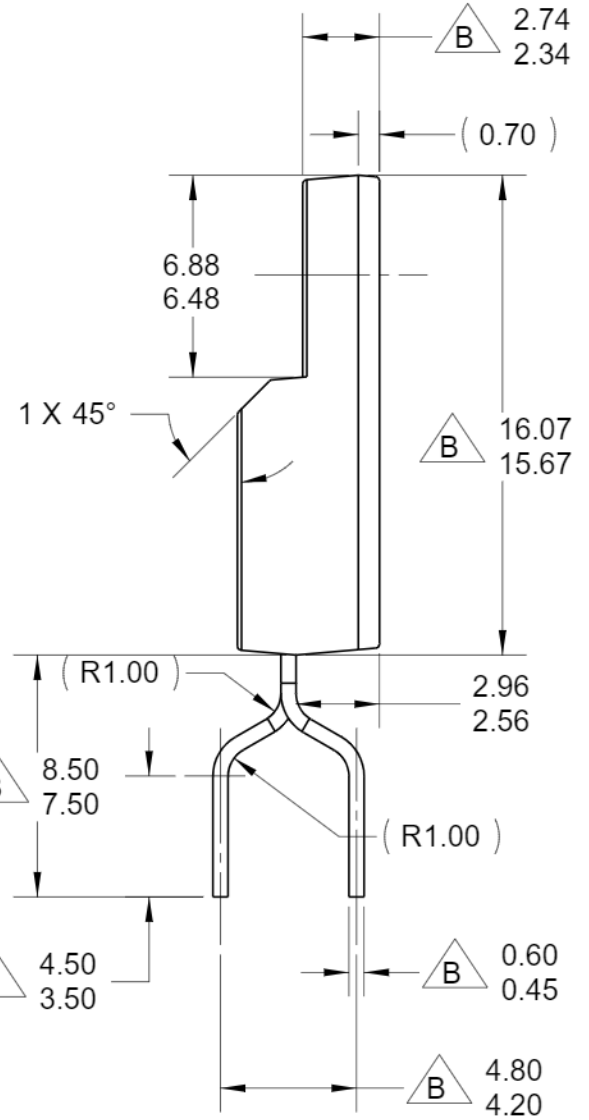
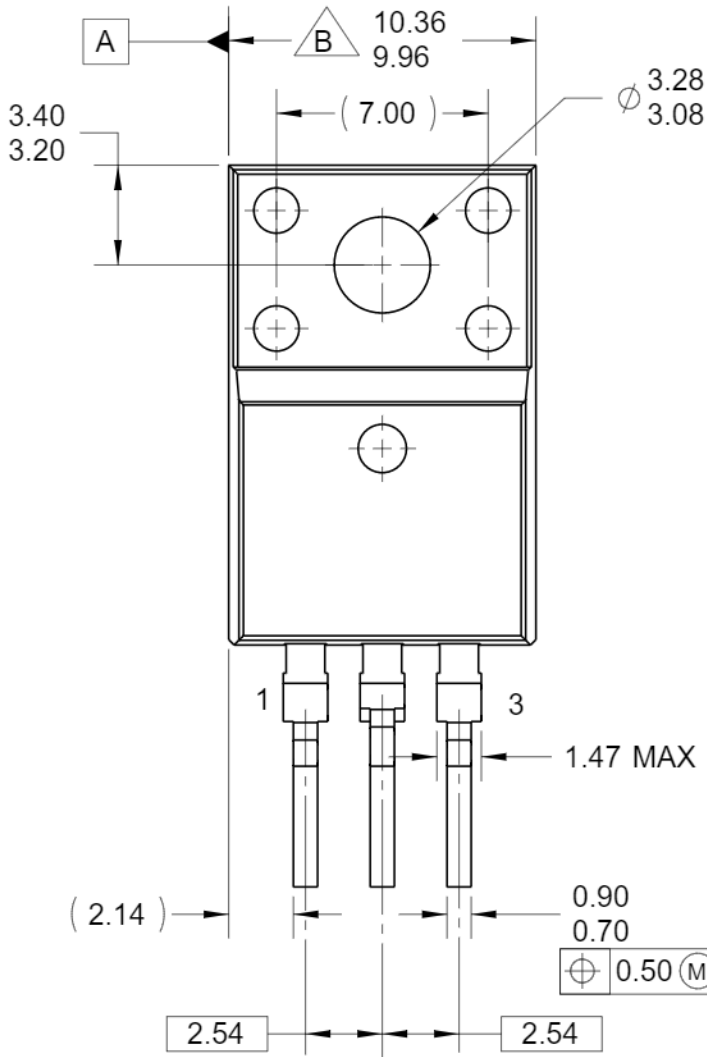
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



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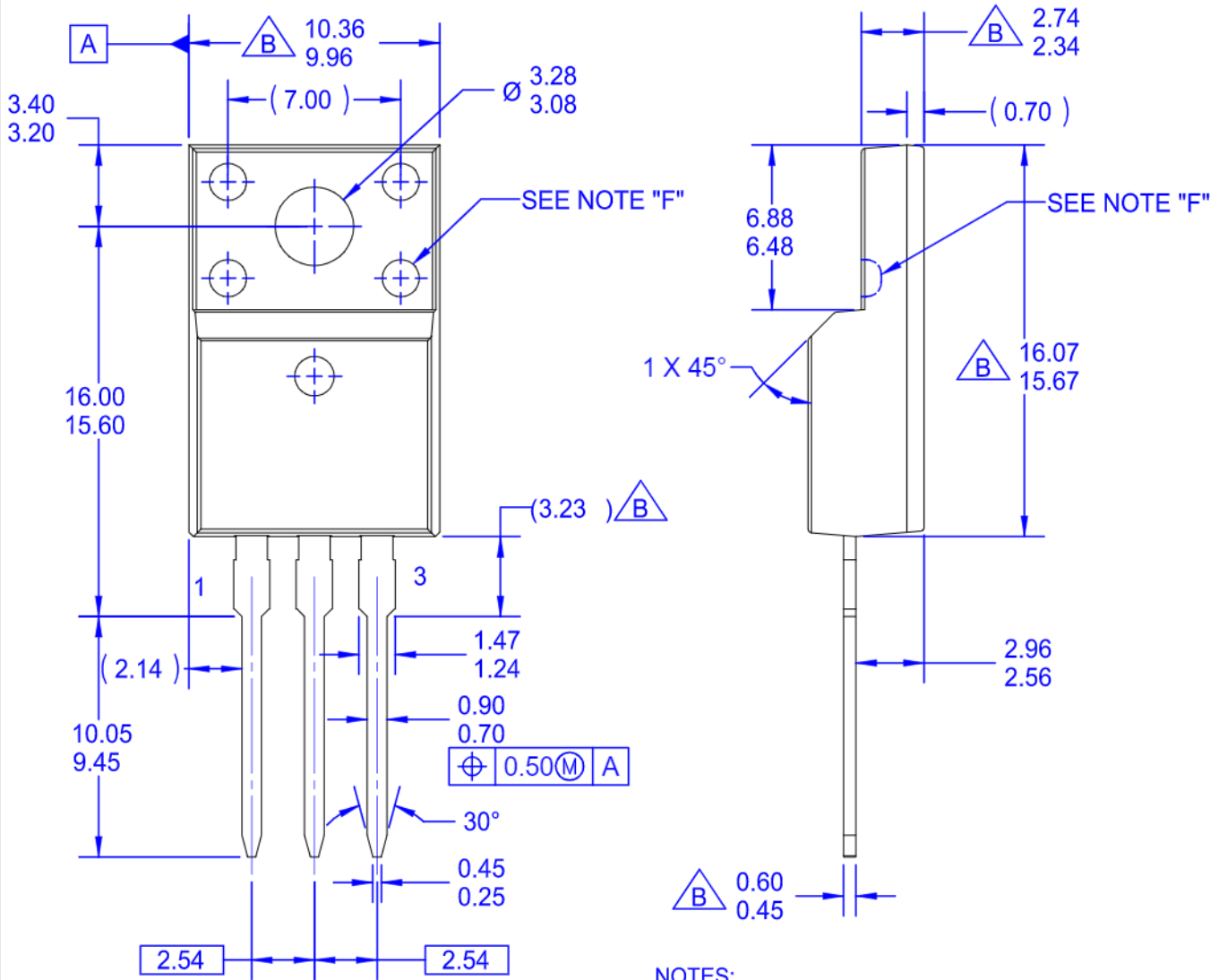
REVISIONS

NBR	DESCRIPTION	DATE	BY/APP'D
1	RELEASED TO DCC	04JUN08	SDLEE/ SUZHOU



NOTES:
 A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
 B. DOES NOT COMPLY EIAJ STD. VALUE.
 C. ALL DIMENSIONS ARE IN MILLIMETERS.
 D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
 E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
 F. DRAWING FILE NAME: TO220N03REV1

APPROVALS		DATE	FAIRCHILD SEMICONDUCTOR™			
DRAWN: BOBOY MALDO		04JUN08	TO220, MOLDED, 3LD, FULL PACK, EIAJ SC91, LG FORM			
CHECKED: SD LEE						
APPROVED: BY HUANG						
APPROVED: HOWARD ALLEN						
PROJECTION			SCALE	SIZE	DRAWING NUMBER	REV
[MM] [INCH]			1:1	N/A	MKT-TO220N03	1
			FORMERLY: N/A	SHEET: 1 OF 1		



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- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV4





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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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