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FQP7P06

P-Channel QFET® MOSFET -60 V, -7 A, 410 $m\Omega$

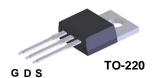
Description

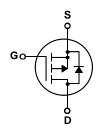
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor® s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.



Features

- -7 A, -60 V, $R_{DS(on)}$ =410 m $\Omega(Max.)$ @ V_{GS} =-10 V, I_D =-3.5 A
- Low Gate Charge (Typ. 6.3 nC)
- Low Crss (Typ. 25 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter		FQP7P06	Unit	
V _{DSS}	Drain-Source Voltage		-60	V	
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		-7.0	А	
			-4.95	А	
I _{DM}	Drain Current - Pulsed	(Note 1)	-28	А	
V _{GSS}	Gate-Source Voltage		± 25	V	
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	90	mJ	
I _{AR}	Avalanche Current	(Note 1)	-7.0	А	
E _{AR}	Repetitive Avalanche Energy	(Note 1)	4.5	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-7.0	V/ns	
P_D	Power Dissipation (T _C = 25°C)		45	W	
	- Derate above 25°C		0.3	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C	
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C	
.r			300		

Thermal Characteristics

Symbol	Parameter	Тур	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		3.35	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		62.5	°C/W

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-60			V
ΔBV_{DSS} / ΔT_{J}	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu A$, Referenced to	25°C	-0.07		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -60 V, V _{GS} = 0 V			-1	μΑ
		V _{DS} = -48 V, T _C = 150°C			-10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -25 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = 25 V, V _{DS} = 0 V			100	nA
On Cha	racteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-2.0		-4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -3.5 A		0.32	0.41	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = -30 \text{ V}, I_{D} = -3.5 \text{ A}$ (Note 4)	4.0		S
C _{oss}	Output Capacitance Reverse Transfer Capacitance	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		110 25	145 32	pF pF
C _{rss}	Reverse Transfer Capacitance			25	32	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -30 \text{ V}, I_{D} = -3.5 \text{ A},$		7	25	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		50	110	ns
t _{d(off)}	Turn-Off Delay Time	1.0 2022		7.5	25	ns
t _f	Turn-Off Fall Time	(No	ete 4, 5)	25	60	ns
Q_g	Total Gate Charge	$V_{DS} = -48 \text{ V}, I_{D} = -7.0 \text{ A},$		6.3	8.2	nC
Q_{gs}	Gate-Source Charge	V _{GS} = -10 V		1.6		nC
Q_{gd}	Gate-Drain Charge	(No	ote 4, 5)	3.1		nC
Drain-S	Source Diode Characteristics ar	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				-7.0	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	m Pulsed Drain-Source Diode Forward Current			-28	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -7.0 \text{ A}$			-4.0	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V, } I_{S} = -7.0 \text{ A,}$		77		ns
	T. Control of the Con	1		1	1	1

- **Notes:**1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 2.1mH, I_{AS} = -7.0A, V_{DD} = -25V, R_G = 25 Ω , Starting T_J = 25°C 3. I_{SD} \leq -7.0A, di/dt \leq 300A/µs, V_{DD} \leq BV_{DSS}, Starting T_J = 25°C 4. Pulse Test : Pulse width \leq 300µs, Duty cycle \leq 2% 5. Essentially independent of operating temperature

Typical Characteristics

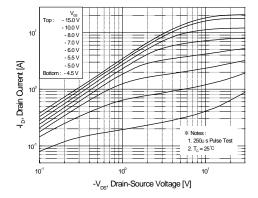


Figure 1. On-Region Characteristics

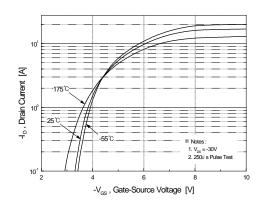


Figure 2. Transfer Characteristics

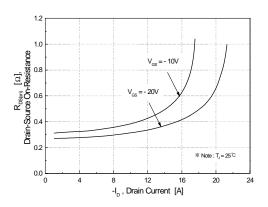


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

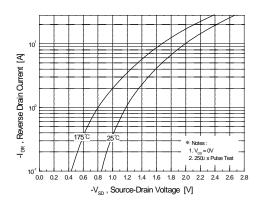


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

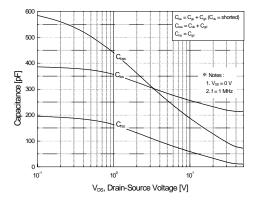


Figure 5. Capacitance Characteristics

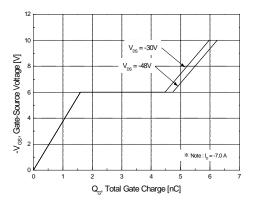
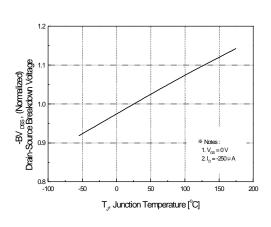


Figure 6. Gate Charge Characteristics

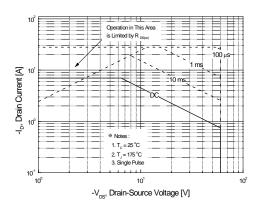


Typical Characteristics (Continued)

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Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



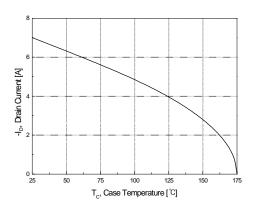


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

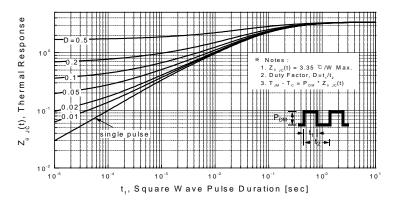
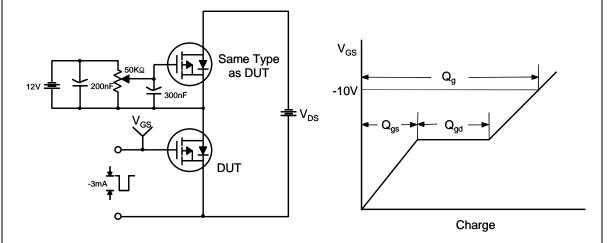
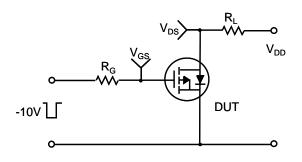


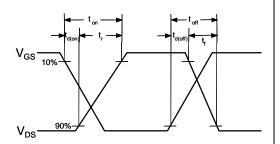
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

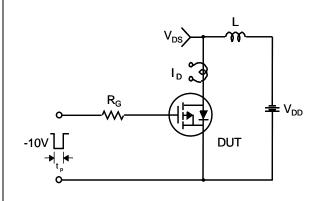


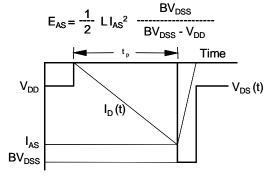
Resistive Switching Test Circuit & Waveforms



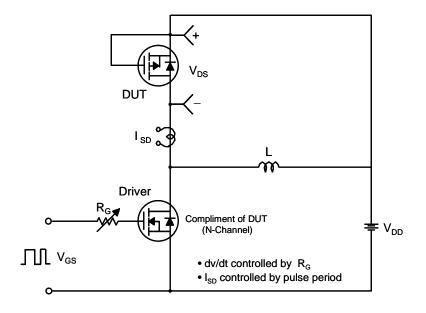


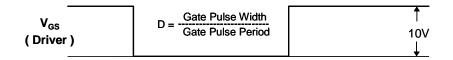
Unclamped Inductive Switching Test Circuit & Waveforms

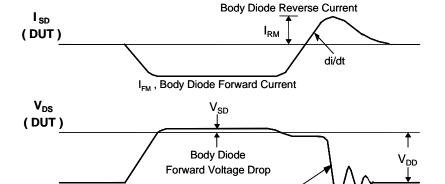




Peak Diode Recovery dv/dt Test Circuit & Waveforms







Body Diode Recovery dv/dt

Mechanical Dimensions TO-220 ø_{3.50}△ ⊕ 0.36 M B AM 10.67 9.65 8.89 6.86 3.43 2.54 6.86 5.84 △13.40 12.19 △9.40 8.38 3 2 1 6.35 MAX 14.73 12.70 0.61 △0.33 (1.91) → 1.78 1.14 2.54 ⊕ 0.36 M B AM NOTES: UNLESS OTHERWISE SPECIFIED A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002. B) ALL DIMENSIONS ARE IN MILLIMETERS. C) DIMENSIONING AND TOLERANCING PER 5.08 ANSI Y14.5 - 1973 D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE) DOES NOT COMPLY JEDEC STANDARD VALUE, F) "A1" DIMENSIONS REPRESENT LIKE BELOW: SINGLE GAUGE = 0.51 - 0.61 DUAL GAUGE = 1,14 - 1,40 ш G) DRAWING FILE NAME: TO220B03REV6 Dimensions in Millimeters





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Datasheet Identification	Product Status	Definition
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