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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

August 2014

FQP15P12 / FQPF15P12

P-Channel QFET® MOSFET

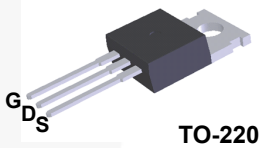
-120 V, -15 A, 0.2 Ω

Description

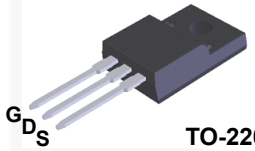
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

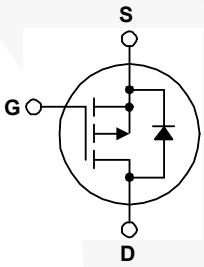
- -15 A, -120 V, $R_{DS(on)}$ = 0.2 Ω (Max.) @ V_{GS}=-10 V, I_D = -7.5 A
- Low Gate Charge (Typ. 29 nC)
- Low Crss (Typ. 110 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



TO-220



TO-220F



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQP15P12	FQPF15P12	Unit
V_{DSS}	Drain-Source Voltage		-120		V
I_D	Drain Current - Continuous (T_C = 25°C)		-15	-15 *	A
	Drain Current - Continuous (T_C = 100°C)		-10.6	-10.6 *	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-60	-60 *	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1157		mJ
I_{AR}	Avalanche Current	(Note 1)	-15		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	10		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-5.0		V/ns
P_D	Power Dissipation (T_C = 25°C)		100	41	W
	- Derate above 25°C		0.67	0.27	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175		°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300		°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FQP15P12	FQPF15P12	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	3.66	°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	40	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	-120	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C	--	-0.13	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -120 V, V_{GS} = 0 V	--	--	-1	μA
		V_{DS} = -96 V, T_C = 150°C	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -7.5 A	--	0.17	0.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = -40 V, I_D = -7.5 A	--	9.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	850	1100	pF
C_{oss}	Output Capacitance		--	310	400	pF
C_{rss}	Reverse Transfer Capacitance		--	110	140	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -60 V, I_D = -15 A, R_G = 25 Ω (Note 4)	--	15	40	ns
t_r	Turn-On Rise Time		--	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		--	80	170	ns
t_f	Turn-Off Fall Time		--	80	170	ns
Q_g	Total Gate Charge	V_{DS} = -96 V, I_D = -15 A, V_{GS} = -10 V (Note 4)	--	29	38	nC
Q_{gs}	Gate-Source Charge		--	5.1	--	nC
Q_{gd}	Gate-Drain Charge		--	15	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-15	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-60	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -15 A	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -15 A, dI_F / dt = 100 A/μs	--	126	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.61	--	μC

Notes:
1. Repetitive rating : pulse width limited by maximum junction temperature.
2. L = 6.0mH, I_{AS} = -15A, V_{DD} = -50V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ -15A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

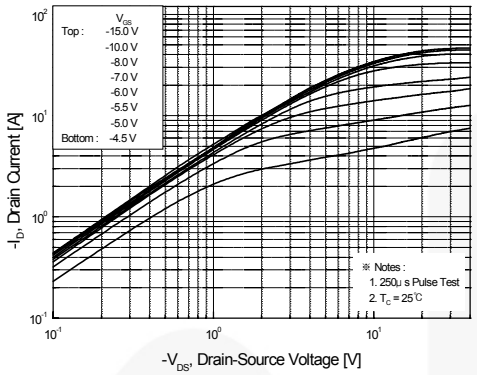


Figure 1. On-Region Characteristics

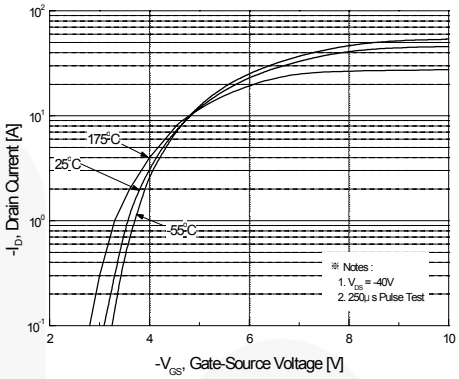


Figure 2. Transfer Characteristics

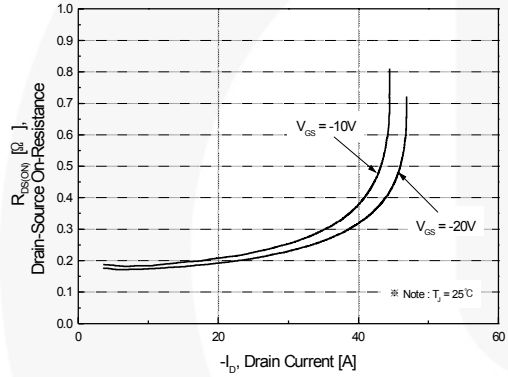


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

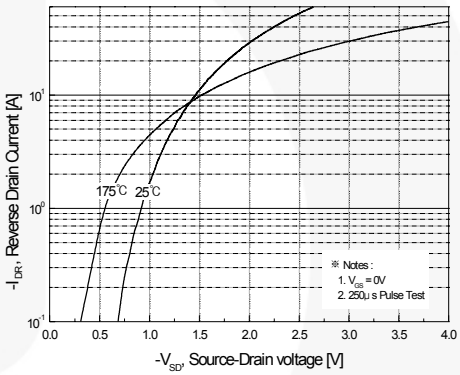


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

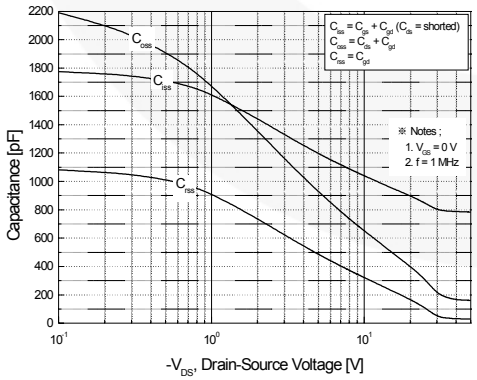


Figure 5. Capacitance Characteristics

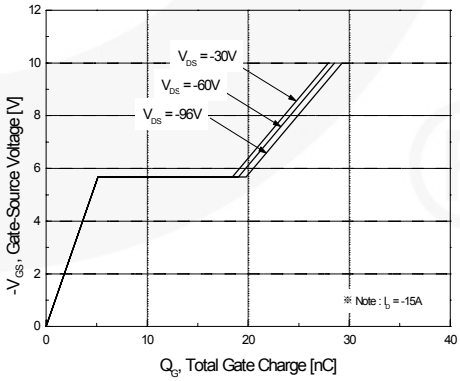


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

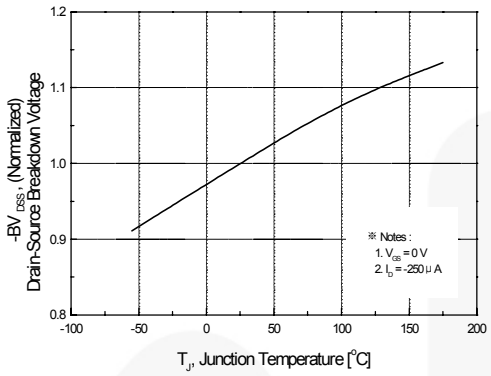


Figure 7. Breakdown Voltage Variation vs Temperature

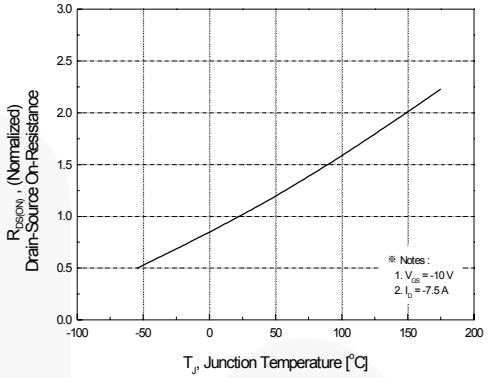


Figure 8. On-Resistance Variation vs Temperature

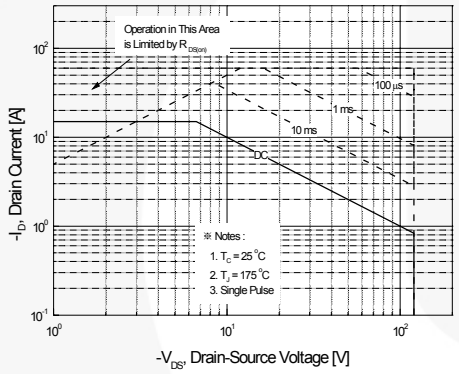


Figure 9-1. Maximum Safe Operating Area for FQP15P12

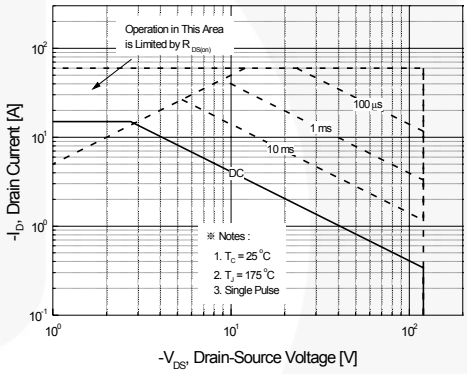


Figure 9-2. Maximum Safe Operating Area for FQPF15P12

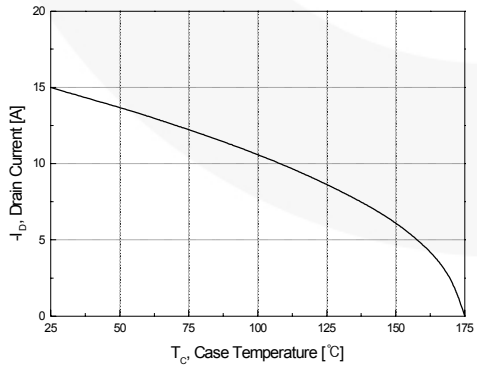


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

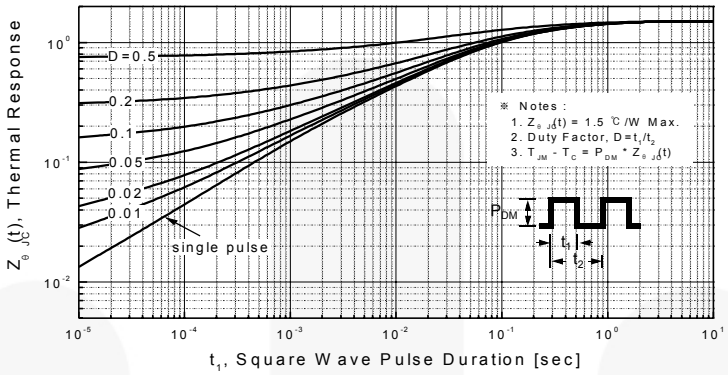


Figure 11-1. Transient Thermal Response Curve for FQP15P12

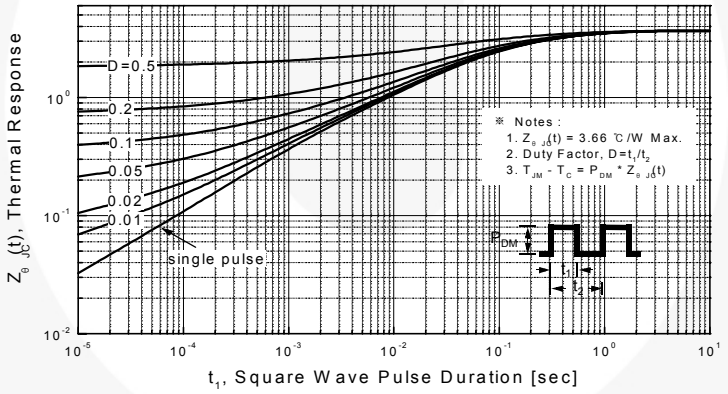


Figure 11-2. Transient Thermal Response Curve for FQPF15P12

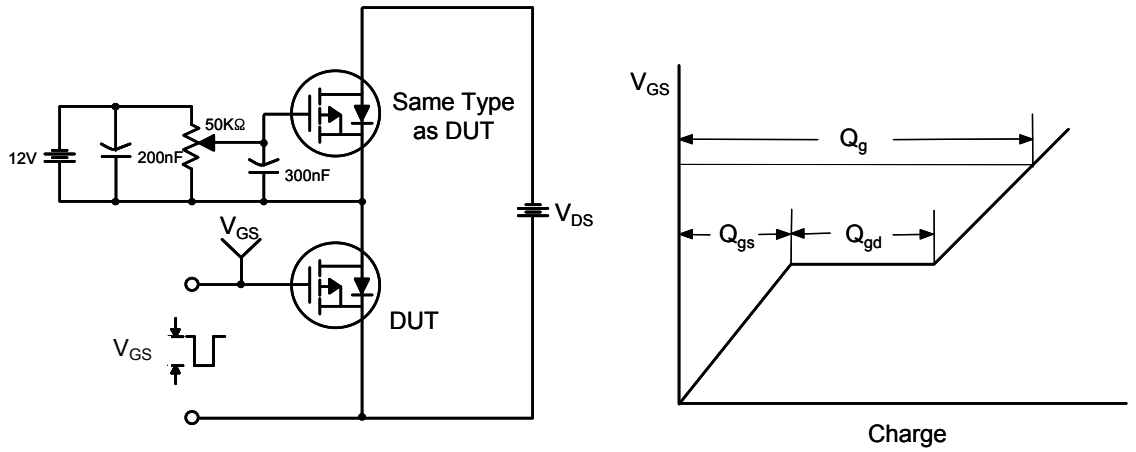


Figure 12. Gate Charge Test Circuit & Waveform

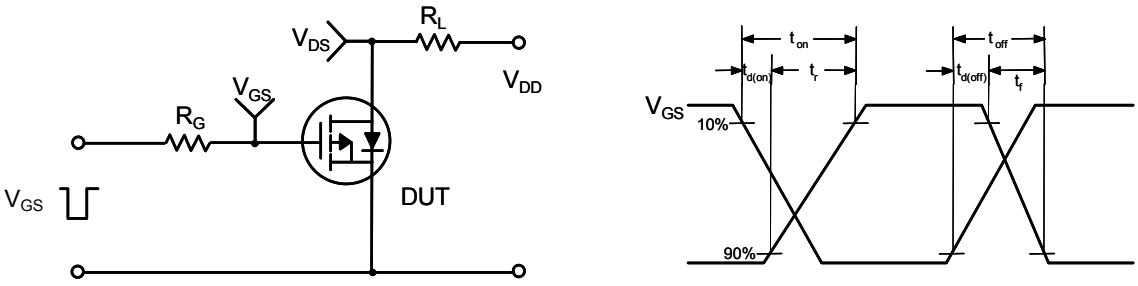


Figure 13. Resistive Switching Test Circuit & Waveforms

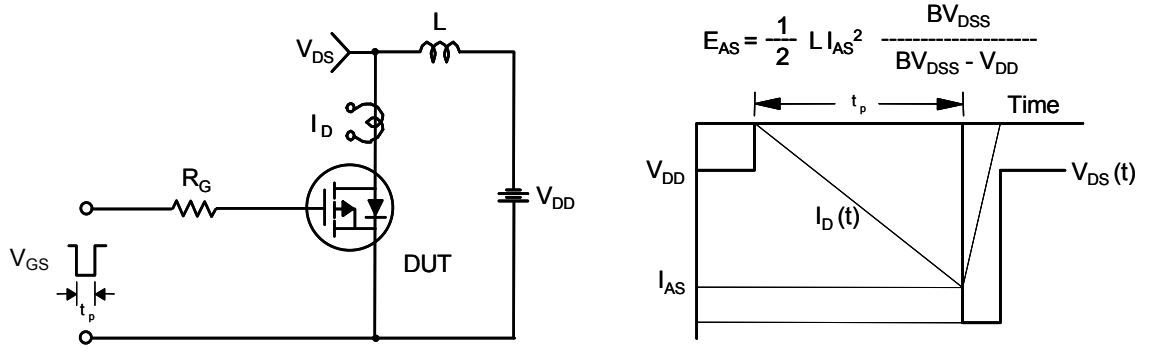


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

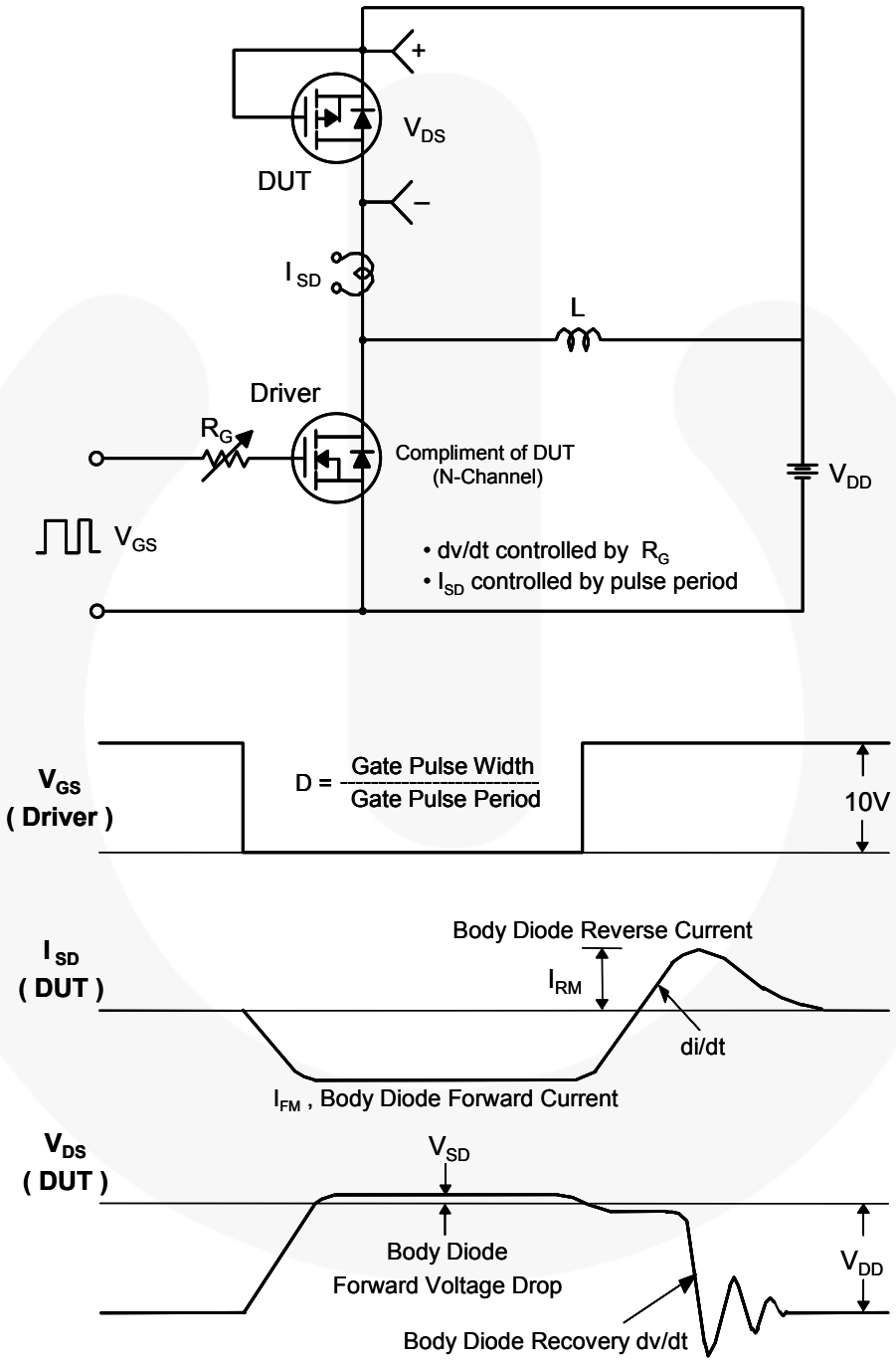
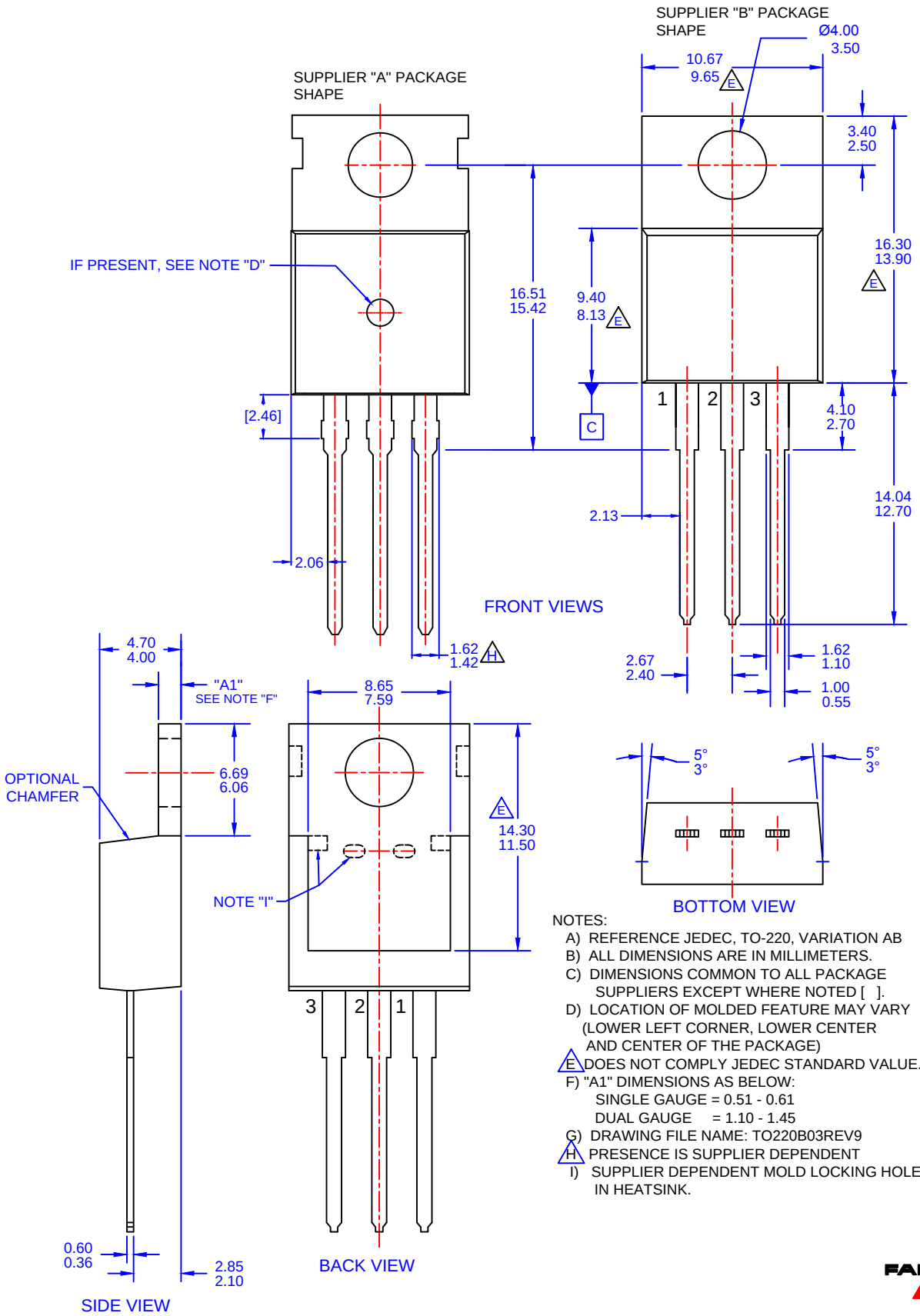


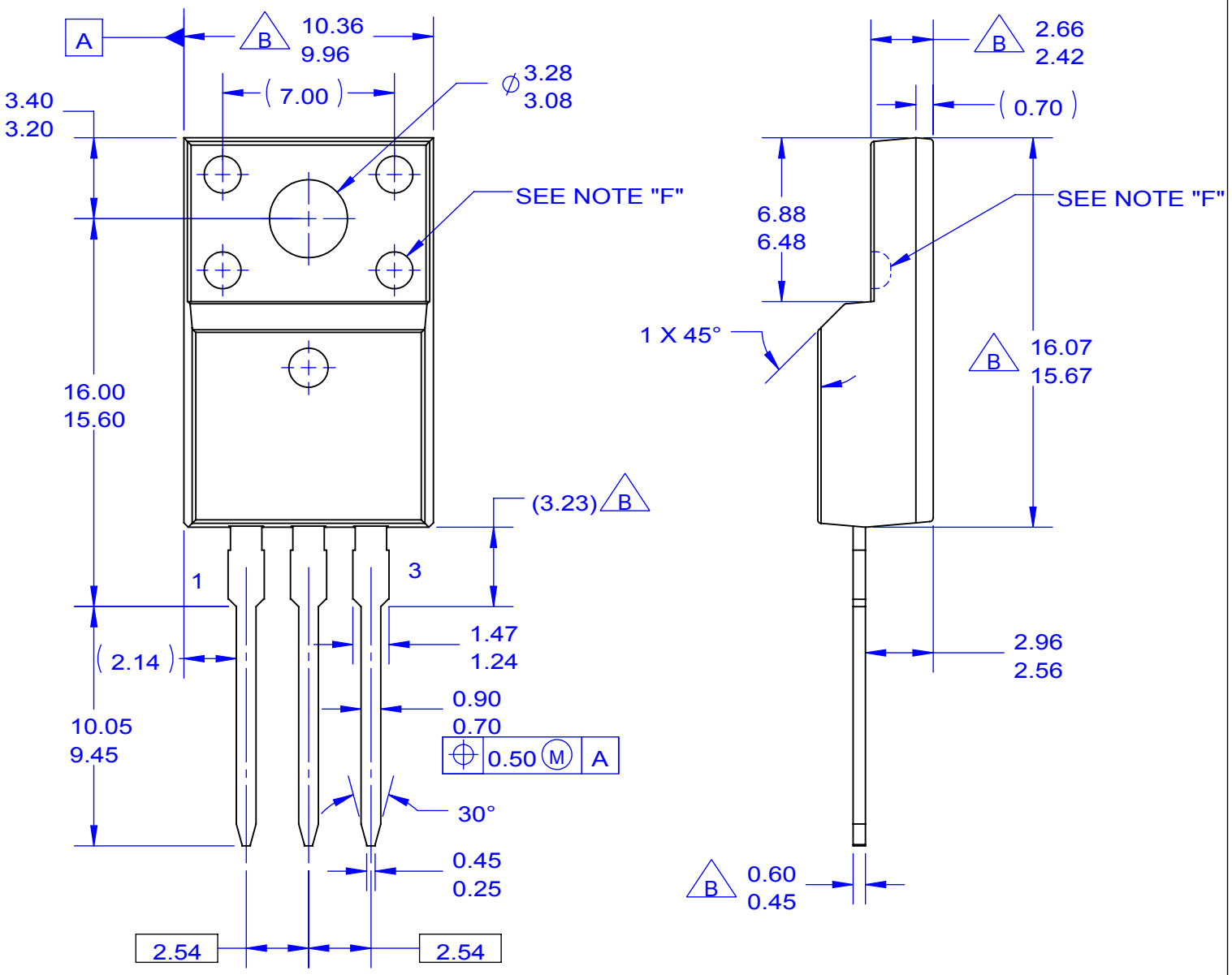
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

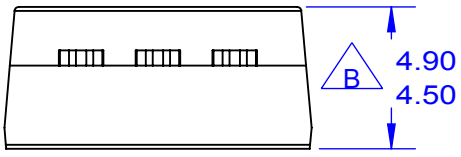


NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) DRAWING FILE NAME: TO220B03REV9
H PRESENCE IS SUPPLIER DEPENDENT
I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

FAIRCHILD





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NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV5

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