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High Temperature, 2.5 A Output Current, Gate Drive Optocoupler



FOD3125

Description

The FOD3125 is a 2.5 A Output Current Gate Drive Optocoupler, capable of driving most medium IGBTs or MOSFETs across extended industrial temperature range, -40°C to 125°C . It is ideally suited for fast switching driving of power IGBTs and MOSFETs used in motor control inverter applications, and high performance power system.

It utilizes ON Semiconductor patented coplanar packaging technology, Optoplanar[®], and optimized IC design to achieve high noise immunity, characterized by high common mode rejection.

It consists of a gallium aluminum arsenide (AlGaAs) light emitting diode optically coupled to an integrated circuit with a high-speed driver for push-pull MOSFET output stage.

Features

- Extended Industrial Temperature Range, -40°C to 125°C
- High Noise Immunity characterized by 35 kV/ μs minimum Common Mode Rejection
- 2.5 A Peak Output Current Driving Capability for Most 1200 V/ 20 A IGBT
- Use of P-channel MOSFETs at Output Stage Enables Output Voltage Swing close to the Supply Rail
- Wide Supply Voltage Range from 15 V to 30 V
- Fast Switching Speed
 - ◆ 400 ns maximum Propagation Delay
 - ◆ 100 ns maximum Pulse Width Distortion
- Under Voltage LockOut (UVLO) with Hysteresis
- Safety and Regulatory Approvals
 - ◆ UL1577, 5000 V_{RMS} for 1 minute
 - ◆ DIN EN/IEC60747-5-5 (pending approval)
- >8.0 mm Clearance and Creepage Distance (Option 'T' or 'TS')
- 1,414 V Peak Working Insulation Voltage (VIORM)
- This is a Pb-Free Device

Applications

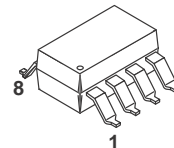
- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

Table 1. TRUTH TABLE

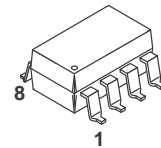
LED	$V_{\text{DD}} - V_{\text{SS}}$ "Positive Going" (Turn-on)	$V_{\text{DD}} - V_{\text{SS}}$ "Negative Going" (Turn-off)	V_{O}
Off	0 V to 30 V	0 V to 30 V	Low
On	0 V to 11 V	0 V to 9.7 V	Low
On	11 V to 14 V	9.7 V to 12.7 V	Transition
On	14 V to 30 V	12.7 V to 30 V	High

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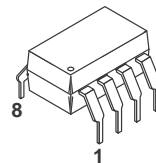
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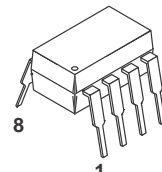
PDIP8 GW
CASE 709AD



PDIP8 GW
CASE 709AC

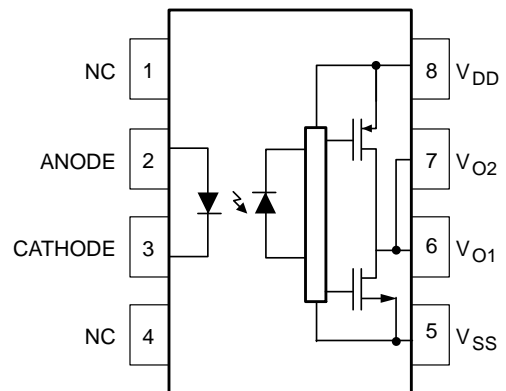


PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.6, 2.54P
CASE 646CQ

FUNCTIONAL BLOCK DIAGRAM



Note: A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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Table 2. PIN DEFINITIONS

Pin #	Name	Description
1	NC	Not Connected
2	Anode	LED Anode
3	Cathode	LED Cathode
4	NC	Not Connected
5	VSS	Negative Supply Voltage
6	VO2	Output Voltage 2 (internally connected to V _{O1})
7	VO1	Output Voltage 1
8	VDD	Positive Supply Voltage

Table 3. SAFETY AND INSULATION RATINGS

As per DIN EN/IEC 60747-5-5 (pending approval). This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Main Voltage < 150 Vrms		I-IV		
	For Rated Main Voltage < 300 Vrms		I-IV		
	For Rated Main Voltage < 450 Vrms		I-III		
	For Rated Main Voltage < 600 Vrms		I-III		
	For Rated Main Voltage < 1000 Vrms (option T, TS)		I-III		
	Climatic Classification		40/125/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V _{PR}	Input to Output Test Voltage, Method b, V _{IORM} × 1.875 = V _{PR} , 100% Production Test with t _m = 1 second, Partial Discharge < 5 pC	2651			
	Input to Output Test Voltage, Method a, V _{IORM} × 1.6 = V _{PR} , Type and Sample Test with t _m = 10 second, Partial Discharge < 5 pC	2262			
V _{IORM}	Max Working Insulation Voltage	1414			V _{peak}
V _{IOTM}	Highest Allowable Over Voltage	6000			V _{peak}
	External Creepage	≥ 8			mm
	External Clearance	≥ 7.4			mm
	External Clearance (for Option T or TS, 0.4" Lead Spacing)	≥ 10.16			mm
	Insulation Thickness	≥ 0.5			mm
T _{Case}	Case Temperature – Maximum Values Allowed in the Event of a Failure	175			°C
I _{S,INPUT}	Input Current – Maximum Values Allowed in the Event of a Failure	400			mA
P _{S,OUTPUT}	Output Power (Duty Factor ≤ 2.7 %) – Maximum Values Allowed in the Event of a Failure	700			mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V – Maximum Values Allowed in the Event of a Failure	> 10 ⁹			Ω

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Table 4. ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified.)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature	-40 to +125	$^\circ\text{C}$
T_J	Junction Temperature	-40 to +125	$^\circ\text{C}$
T_{SOL}	Lead Wave Solder Temperature (refer to page 12 for reflow solder profile)	260 for 10 sec	$^\circ\text{C}$
$I_{F(AVG)}$	Average Input Current	25	mA
f	Operating Frequency ⁽¹⁾	50	kHz
V_R	Reverse Input Voltage	5	V
$I_{O(PEAK)}$	Peak Output Current ⁽²⁾	3	A
$V_{DD} - V_{SS}$	Supply Voltage	0 to 35	V
		$T_A \geq 90^\circ\text{C}$	
$V_{O(PEAK)}$	Peak Output Voltage	0 to V_{DD}	V
$t_{R(IN)}, t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
PD_I	Input Power Dissipation ^{(3) (5)}	45	mW
PD_O	Output Power Dissipation ^{(4) (5)}	250	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exponential Waveform, $I_{O(PEAK)} \leq |2.5 A| \leq 0.3 \mu\text{s}$
2. Maximum pulse width = 10 μs , maximum duty cycle = 1.1 %.
3. Derate linearly above 87 $^\circ\text{C}$, free air temperature at a rate of 0.77 mW/ $^\circ\text{C}$.
4. Derate linearly above 100 $^\circ\text{C}$, free air temperature at a rate of 5.7 mW/ $^\circ\text{C}$.
5. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Units
T_A	Ambient Operating Temperature	-40 to +125	$^\circ\text{C}$
$V_{DD} - V_{SS}$	Power Supply	15 to 30	V
$I_{F(ON)}$	Input Current (ON)	7 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	0 to 0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ISOLATION CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	$T_A = 25^\circ\text{C}$, R.H. < 50 %, $t = 1.0$ minute, $I_{I-O} \leq 10 \mu\text{A}$, 50 Hz ^{(6) (7)}	5000			V_{RMS}
R_{ISO}	Isolation Resistance	$V_{I-O} = 500 \text{ V}$ ⁽⁶⁾		10^{11}		Ω
C_{ISO}	Isolation Capacitance	$V_{I-O} = 0 \text{ V}$, Frequency = 1.0 MHz ⁽⁶⁾		1		pF

6. Device is considered a two terminal device: pins 2 and 3 are shorted together and pins 5, 6, 7 and 8 are shorted together.

7. 5,000 V_{RMS} for 1 minute duration is equivalent to 6,000 VAC_{RMS} for 1 second duration.

Table 7. ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_F	Input Forward Voltage	$I_F = 10 \text{ mA}$	1.1	1.5	1.8	V
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/ $^\circ\text{C}$
BV_R	Input Reverse Breakdown Voltage	$I_R = 10 \mu\text{A}$	5			V

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Table 7. ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CIN	Input Capacitance	$f = 1 \text{ MHz}, V_F = 0 \text{ V}$		20		pF
IOH	High Level Output Current ⁽¹⁾	$V_O = V_{DD} - 3 \text{ V}$	-1.0	-2.0		A
		$V_O = V_{DD} - 6 \text{ V}$	-2.0			
IOL	Low Level Output Current ⁽¹⁾	$V_O = V_{SS} + 3 \text{ V}$	1.0	2.0		A
		$V_O = V_{SS} + 6 \text{ V}$	2.0			
VOH	High Level Output Voltage	$I_F = 10 \text{ mA}, I_O = -2.5 \text{ A}$	$V_{DD} - 6.25 \text{ V}$	$V_{DD} - 2.5 \text{ V}$		V
		$I_F = 10 \text{ mA}, I_O = -100 \text{ mA}$	$V_{DD} - 0.25 \text{ V}$	$V_{DD} - 0.1 \text{ V}$		
VOL	Low Level Output Voltage	$I_F = 0 \text{ mA}, I_O = 2.5 \text{ A}$		$V_{SS} + 2.5 \text{ V}$	$V_{SS} + 6.25 \text{ V}$	V
		$I_F = 0 \text{ mA}, I_O = 100 \text{ mA}$		$V_{SS} + 0.1 \text{ V}$	$V_{SS} + 0.25 \text{ V}$	
IDDH	High Level Supply Current	$V_O = \text{Open}, I_F = 7 \text{ to } 16 \text{ mA}$		2.8	3.8	mA
IDDL	Low Level Supply Current	$V_O = \text{Open}, V_F = 0 \text{ to } 0.8 \text{ V}$		2.8	3.8	mA
IFLH	Threshold Input Current Low to High	$I_O = 0 \text{ mA}, V_O > 5 \text{ V}$		2.3	5.0	mA
VFHL	Threshold Input Voltage High to Low	$I_O = 0 \text{ mA}, V_O < 5 \text{ V}$	0.8			V
VUVLO+	Under Voltage Lockout Threshold	$I_F = 1 \text{ mA}, V_O > 5 \text{ V}$	11	12.7	14	V
VUVLO-		$I_F = 10 \text{ mA}, V_O < 5 \text{ V}$	9.7	11.2	12.7	V
UVLOHYS	Under Voltage Lockout Threshold Hysteresis			1.5		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Maximum pulse width = 10 μs , maximum duty cycle = 1.1 %.

Table 8. SWITCHING CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $V_{DD} = 30 \text{ V}$, $V_{SS} = \text{Ground}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
tPHL	Propagation Delay Time to Logic Low Output	$I_F = 7 \text{ mA to } 16 \text{ mA},$ $R_g = 10 \Omega, C_g = 10 \text{ nF},$ $f = 10 \text{ kHz}, \text{ Duty Cycle} = 50 \%$	150	275	400	ns	
tPLH	Propagation Delay Time to Logic High Output		150	255	400	ns	
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $			20	100	ns	
PDD (Skew)	Propagation Delay Difference Between Any Two Parts or Channels, $(t_{PHL} - t_{PLH})$ ⁽⁹⁾			-250		250	ns
t _r	Output Rise Time (10% – 90%)				60		ns
t _f	Output Fall Time (90% – 10%)				60		ns
tUVLO ON	UVLO Turn On Delay		$I_F = 10 \text{ mA}, V_O > 5 \text{ V}$		1.6		μs
tUVLO OFF	UVLO Turn Off Delay	$I_F = 10 \text{ mA}, V_O < 5 \text{ V}$		0.4		μs	
CM _H	Common Mode Transient Immunity at Output High	$T_A = 25^\circ\text{C}, V_{DD} = 30 \text{ V},$ $I_F = 7 \text{ to } 16 \text{ mA}, V_{CM} = 2000 \text{ V}$ ⁽¹⁰⁾	35	50		kV/ μs	
CM _L	Common Mode Transient Immunity at Output Low	$T_A = 25^\circ\text{C}, V_{DD} = 30 \text{ V}, V_F = 0 \text{ V},$ $V_{CM} = 2000 \text{ V}$ ⁽¹¹⁾	35	50		kV/ μs	

9. The difference between t_{PHL} and t_{PLH} between any two FOD3125 parts under same test conditions.

10. Common mode transient immunity at output high is the maximum tolerable negative dV_{cm}/dt on the trailing edge of the common mode impulse signal, V_{cm}, to assure that the output will remain high (i.e., $V_O > 15.0 \text{ V}$).

11. Common mode transient immunity at output low is the maximum tolerable positive dV_{cm}/dt on the leading edge of the common pulse signal, V_{cm}, to assure that the output will remain low (i.e., $V_O < 1.0 \text{ V}$).

TYPICAL PERFORMANCE CURVES

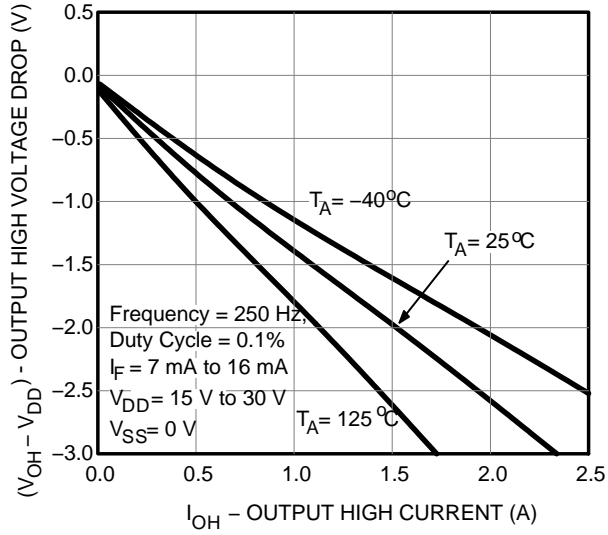


Figure 1. Output High Voltage Drop vs. Output High Current

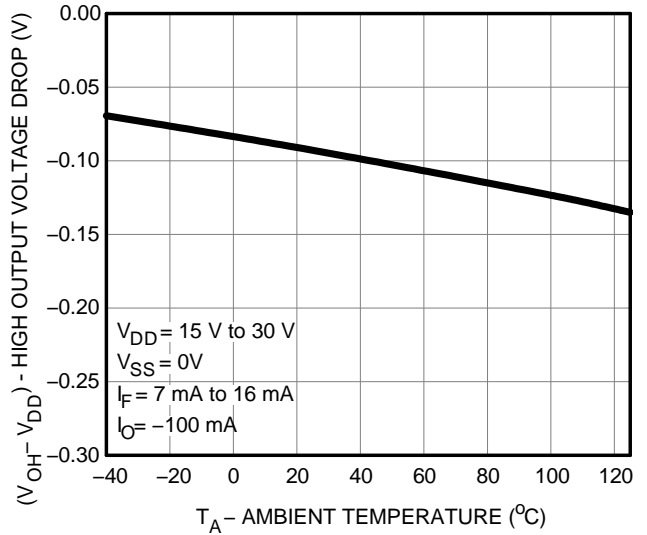


Figure 2. Output High Voltage Drop vs. Ambient Temperature

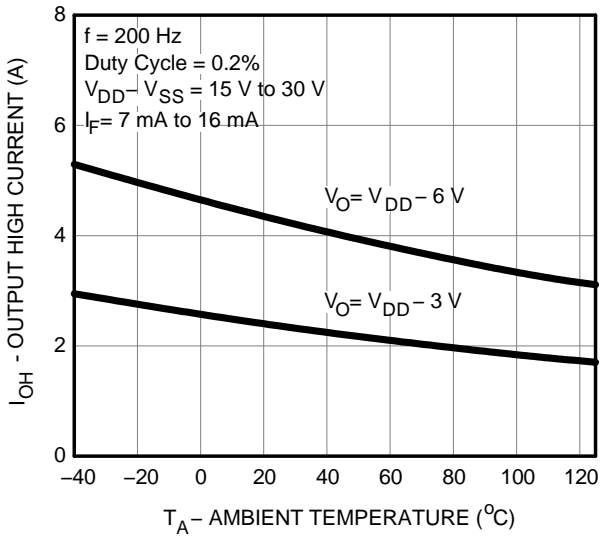


Figure 3. Output High Current vs. Ambient Temperature

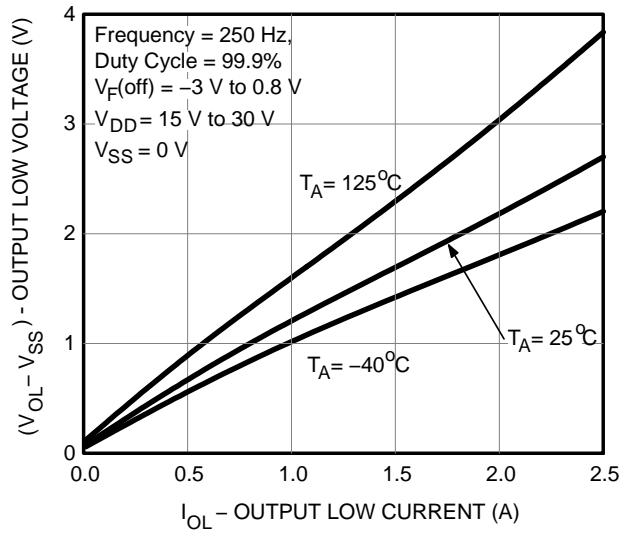


Figure 4. Output Low Voltage vs. Output Low Current

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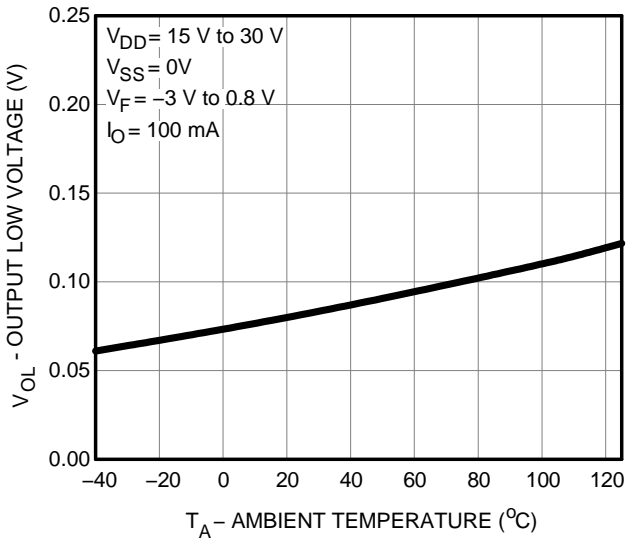


Figure 5. Output Low Voltage vs. Ambient Temperature

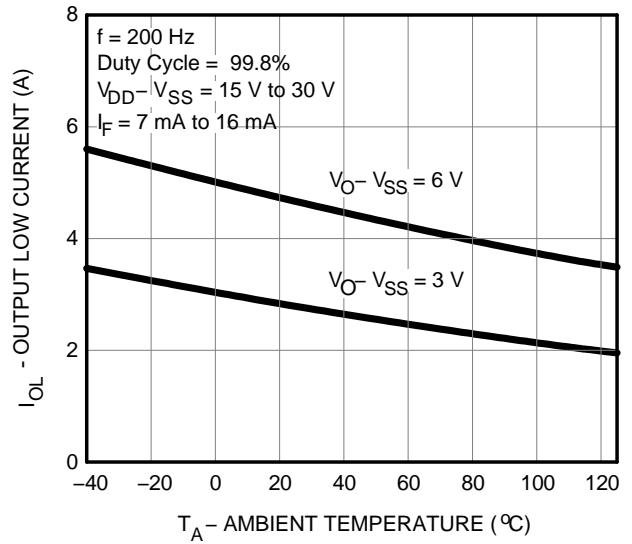


Figure 6. Output Low Current vs. Ambient Temperature

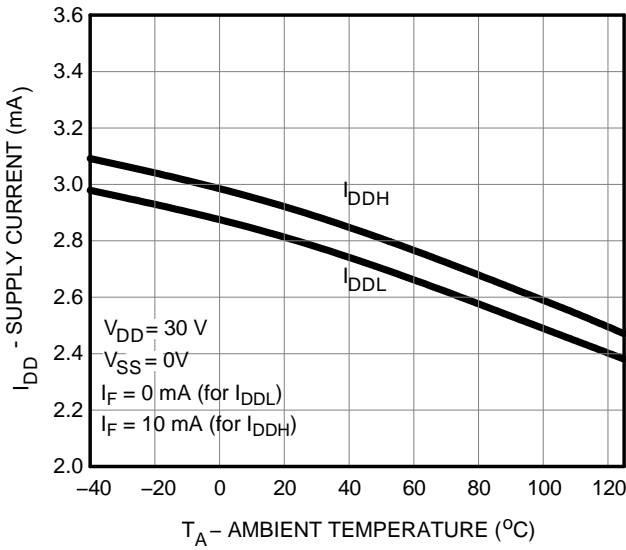


Figure 7. Supply Current vs. Ambient Temperature

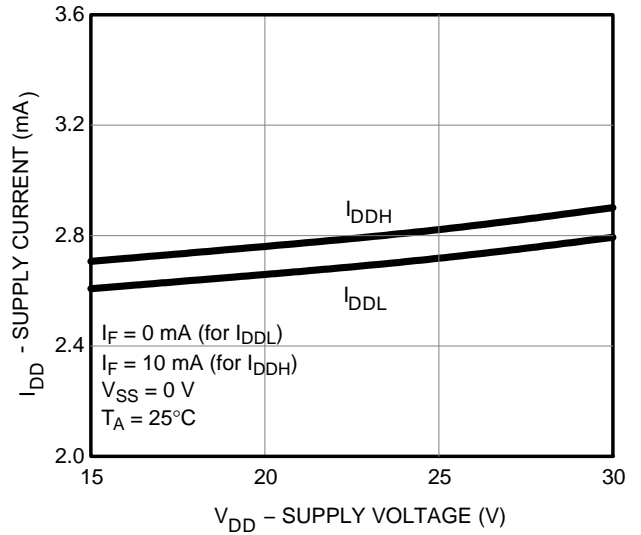


Figure 8. Supply Current vs. Supply Voltage

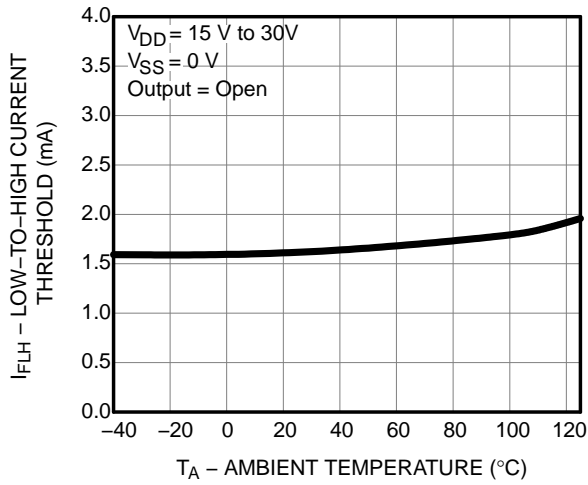


Figure 9. Low to High Input Current Threshold vs. Ambient Temperature

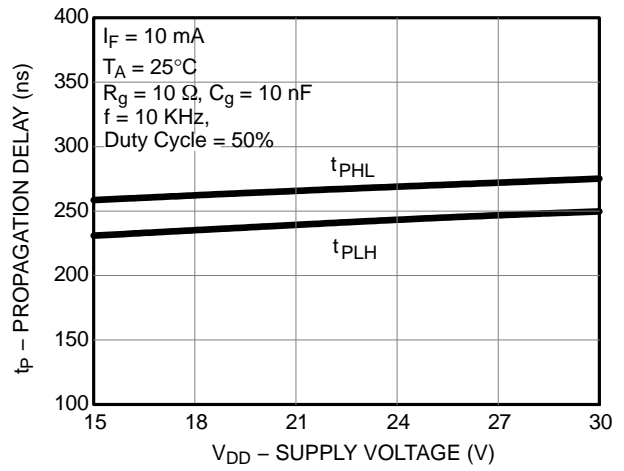


Figure 10. Propagation Delay vs. Supply Voltage

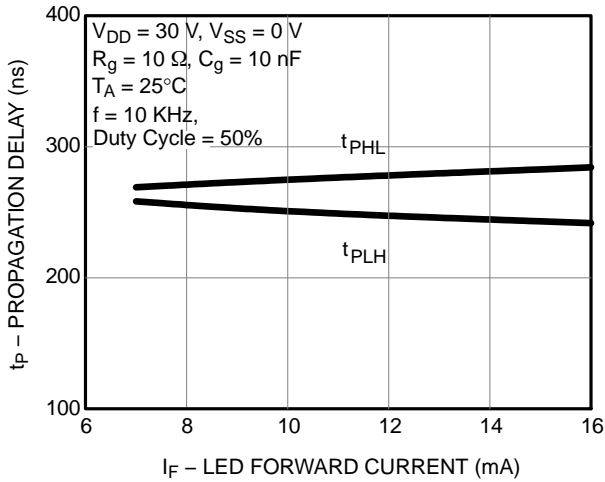


Figure 11. Propagation Delay vs. LED Forward Current

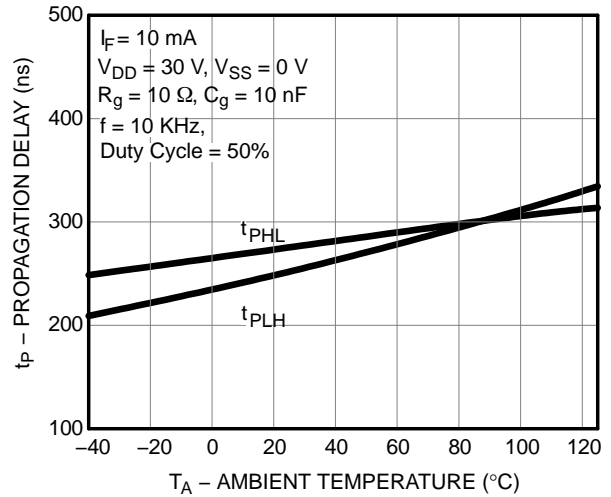


Figure 12. Propagation Delay vs. Ambient Temperature

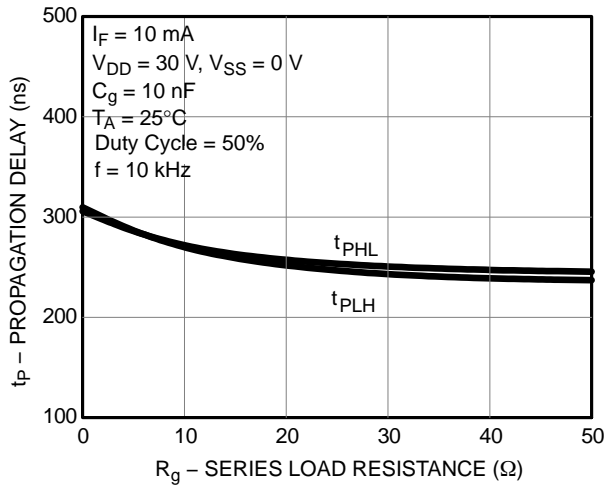


Figure 13. Propagation Delay vs. Series Load Resistance

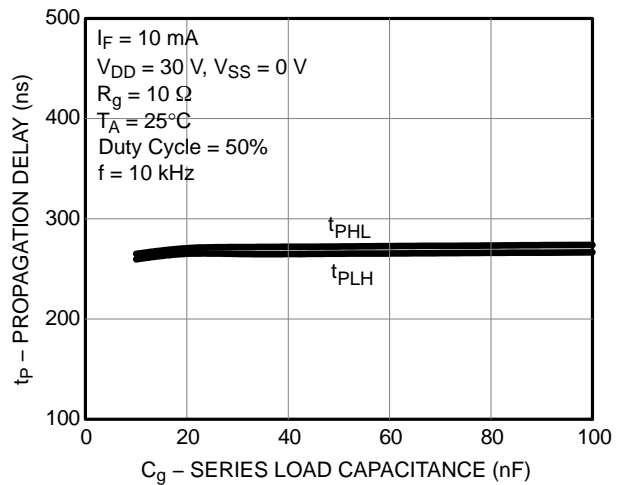


Figure 14. Propagation Delay vs. Load Capacitance

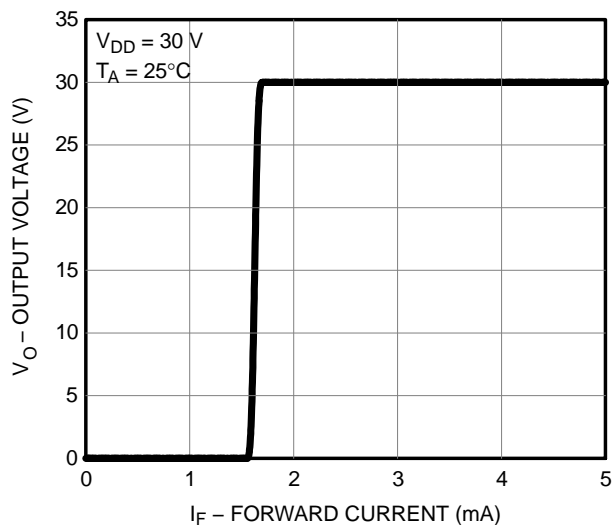


Figure 15. Transfer Characteristics

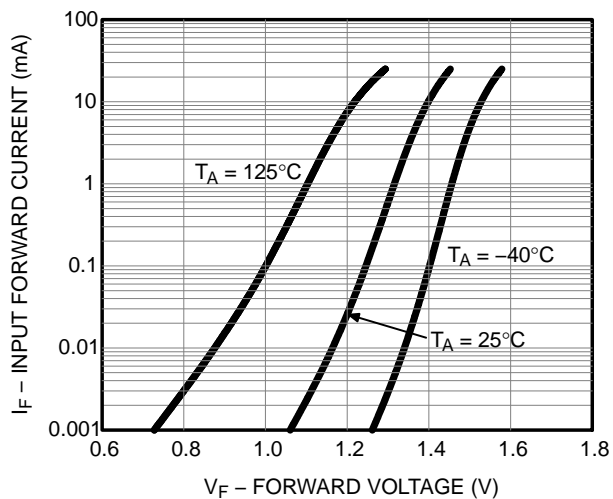


Figure 16. Input Forward Current vs. Forward Voltage

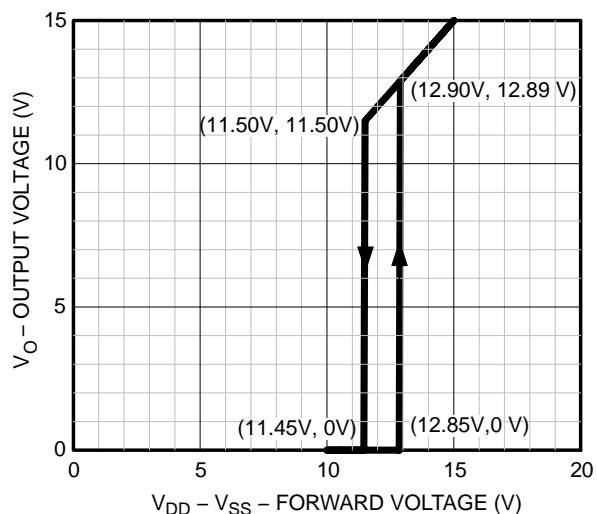


Figure 17. Under Voltage Lockout

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TEST CIRCUIT

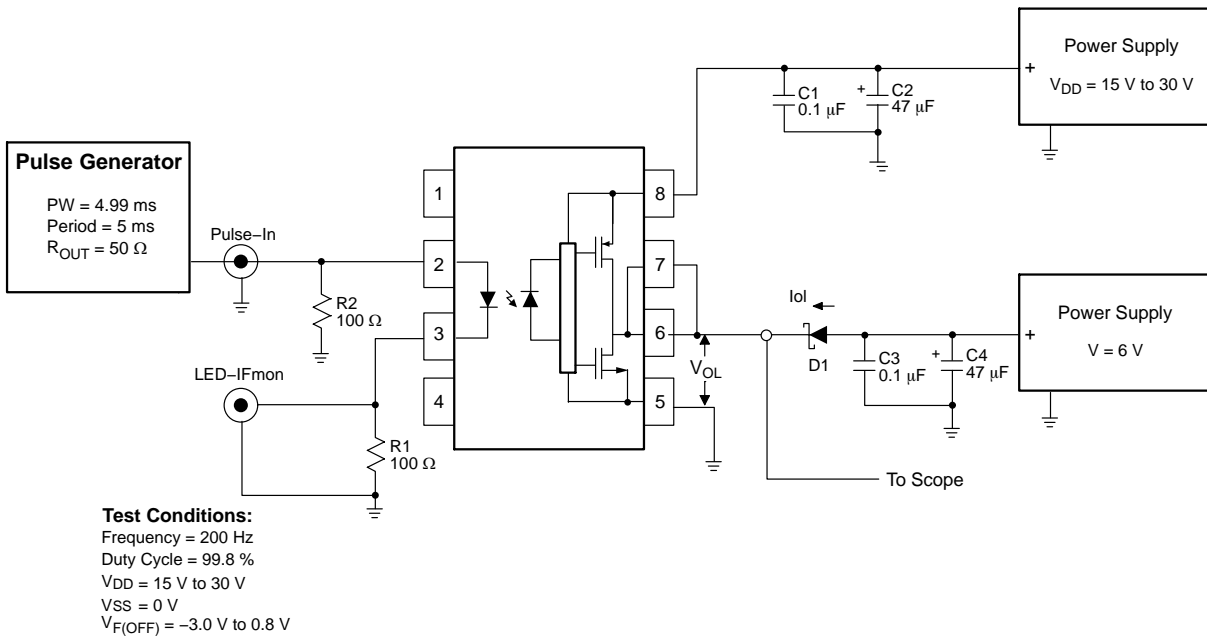


Figure 18. I_{OL} Test Circuit

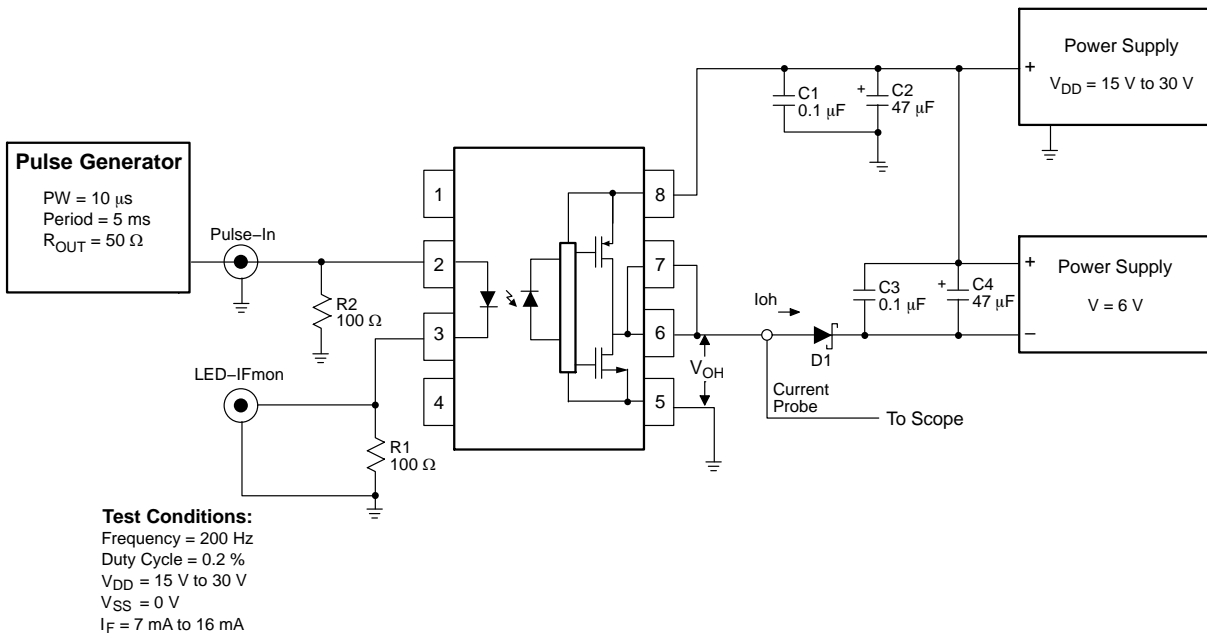


Figure 19. I_{OH} Test Circuit

FOD3125

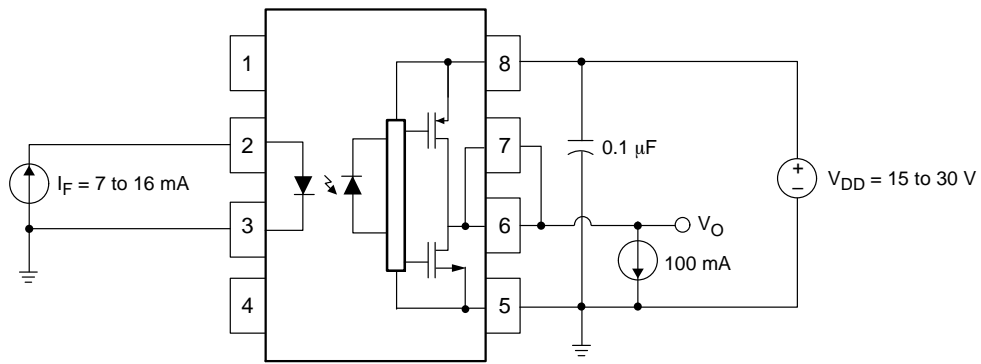


Figure 20. V_{OH} Test Circuit

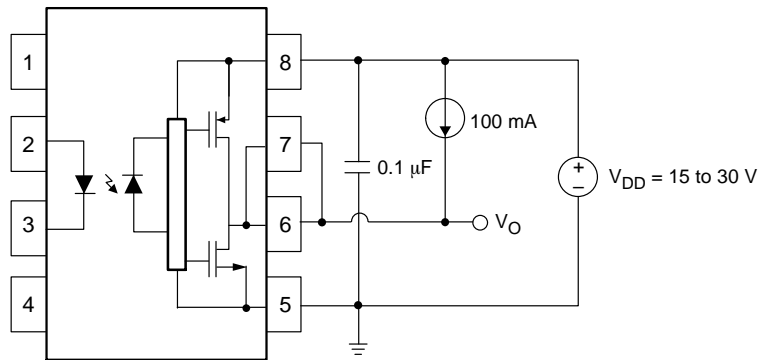


Figure 21. V_{OL} Test Circuit

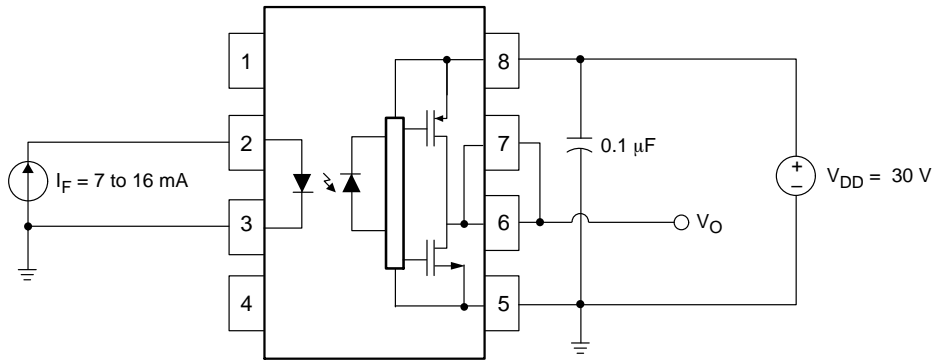


Figure 22. I_{DDH} Test Circuit

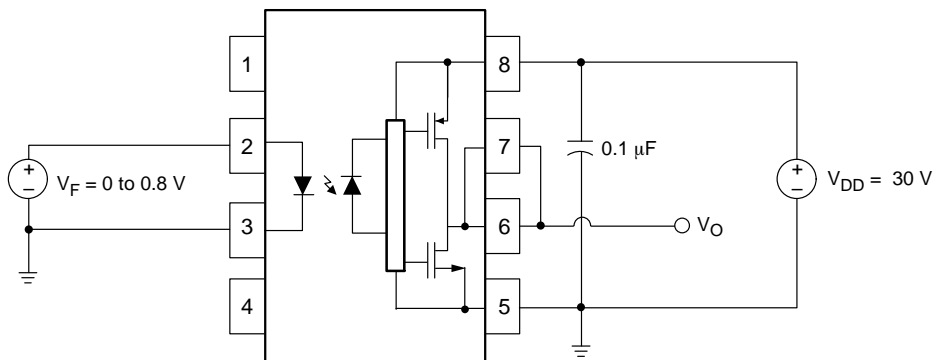


Figure 23. I_{DDL} Test Circuit

FOD3125

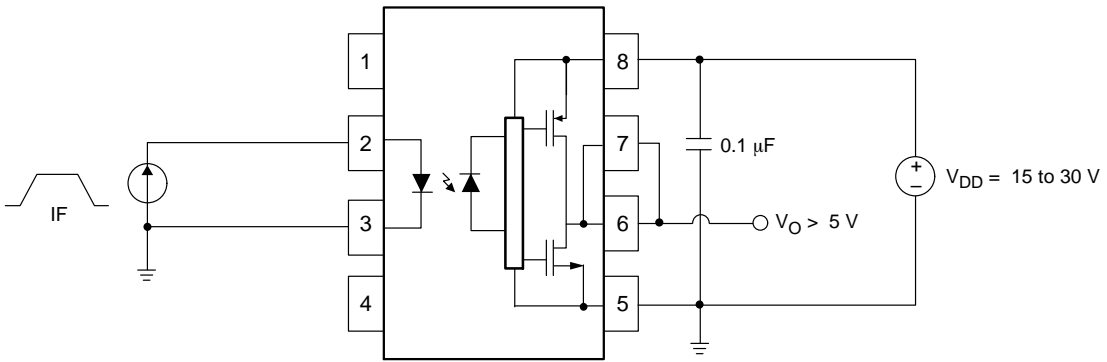


Figure 24. I_{FLH} Test Circuit

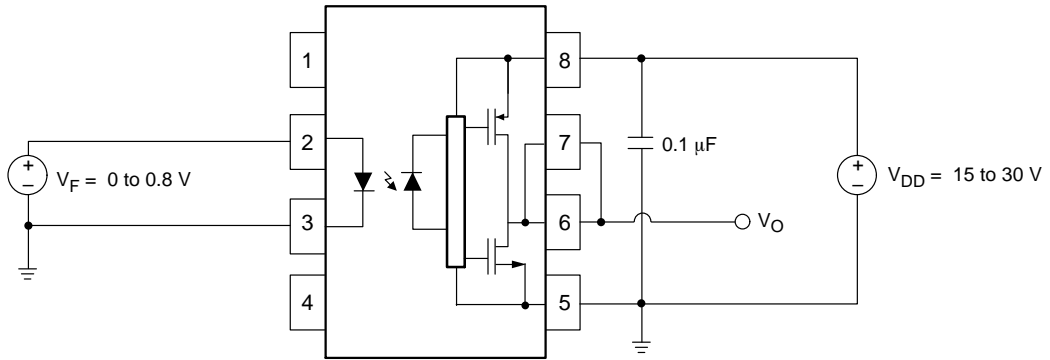


Figure 25. V_{FHL} Test Circuit

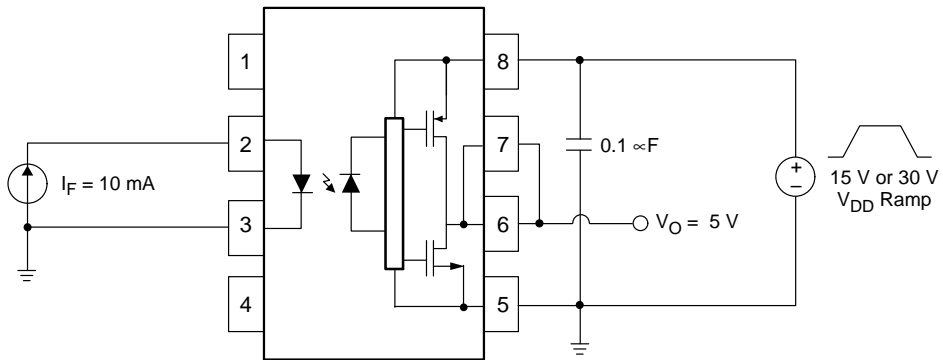


Figure 26. UVLO Test Circuit

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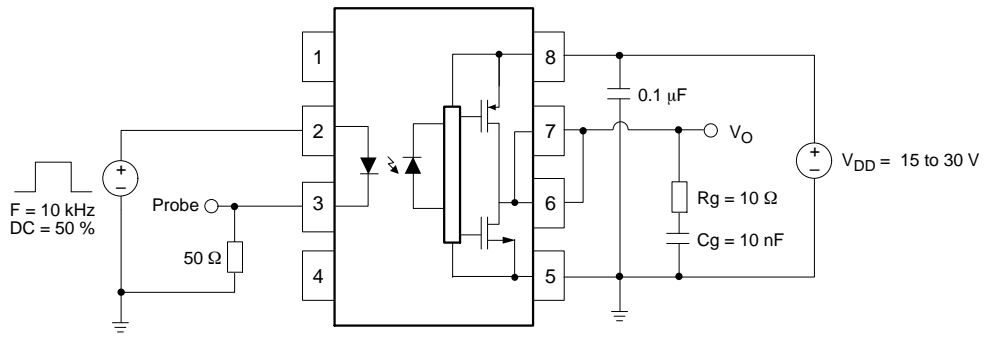


Figure 27. t_{PHL} , t_{PLH} , t_R and t_F Test Circuit and Waveforms

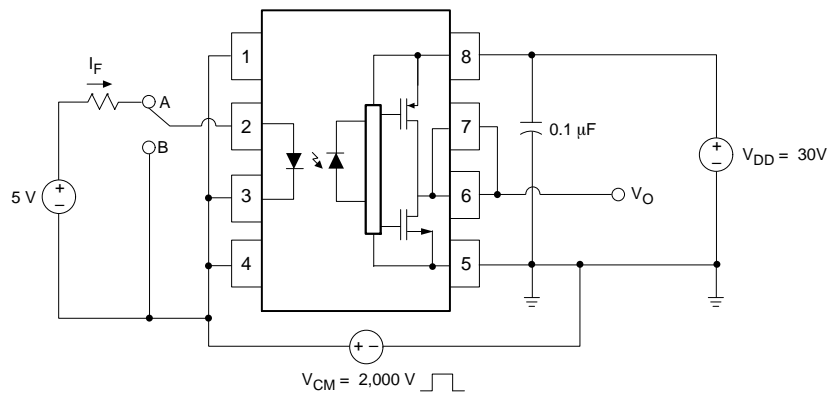
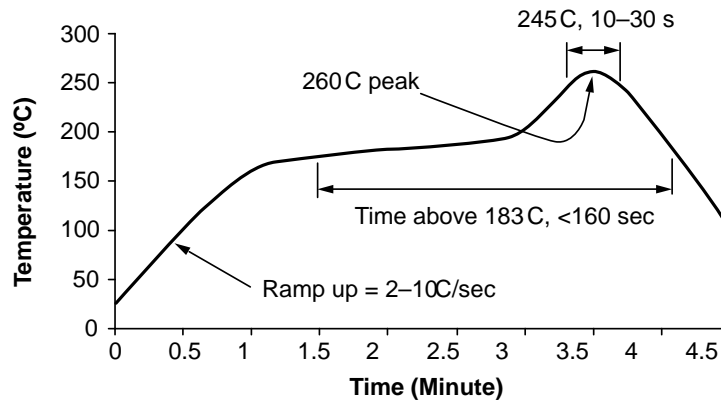


Figure 28. CMR Test Circuit and Waveforms

FOD3125

REFLOW PROFILE



Notes:

- Peak reflow temperature: 260 C (package surface temperature)
- Time of temperature higher than 183 C for 160 seconds or less
- One time soldering reflow is recommended

Figure 29. Reflow Profile

ORDERING INFORMATION

Part Number	Package	Shipping†
FOD3125	DIP 8-Pin	50 / Tube
FOD3125S	SMT 8-Pin (Lead Bend)	50 / Tube
FOD3125SD	SMT 8-Pin (Lead Bend)	1,000 / Tape & Reel
FOD3125V	DIP 8-Pin, DIN EN/IEC 60747-5-5 option (pending approval)	50 / Tube
FOD3125SV	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option (pending approval)	50 / Tube
FOD3125SDV	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option (pending approval)	1,000 / Tape & Reel
FOD3125TV	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 option (pending approval)	50 / Tube
FOD3125TSV	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 option (pending approval)	50 / Tube
FOD3125TSR2V	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 option (pending approval)	1,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

MARKING INFORMATION

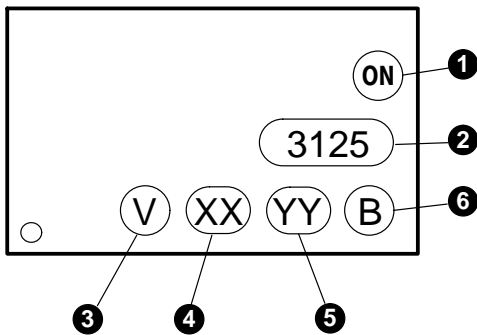


Figure 30. Device Marking

Definitions	
1	Company logo
2	Device number
3	DIN EN/IEC60747-5-5 Option (pending approval) (only appears on component ordered with this option)
4	Two digit year code, e.g., '19'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

CARRIER TAPE SPECIFICATIONS (OPTION SD)

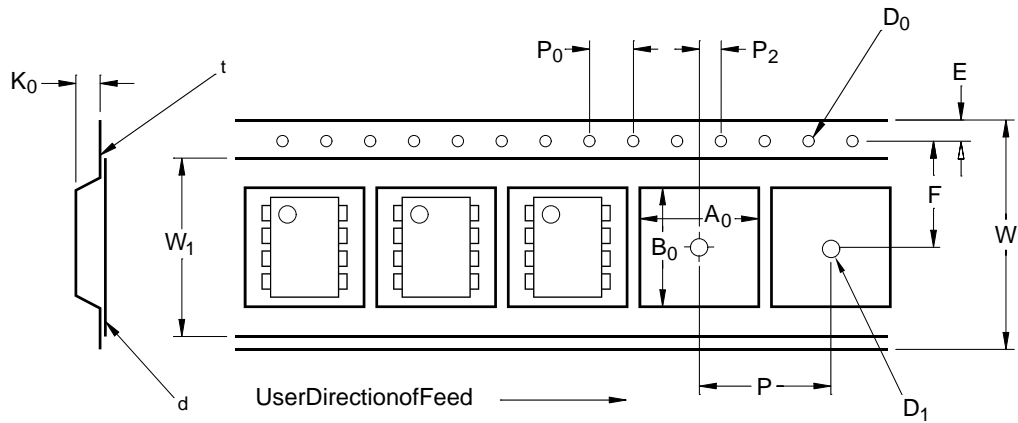


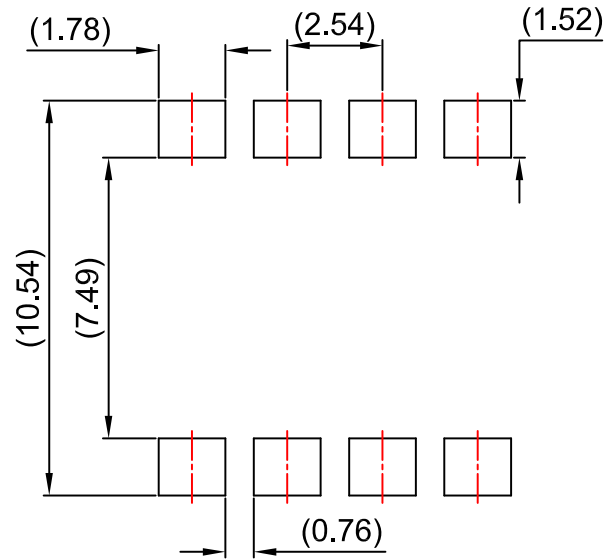
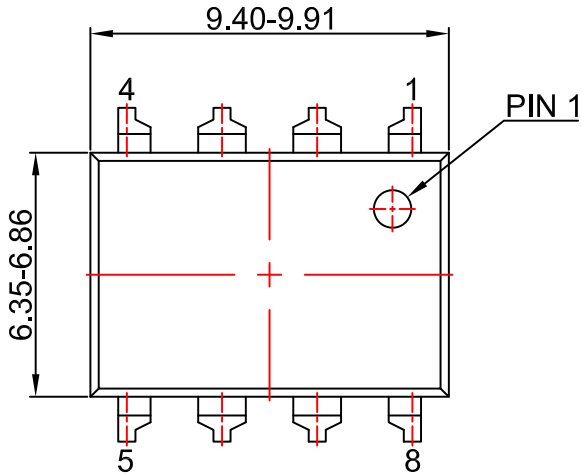
Figure 31. Carrier Tape Specifications

Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P ₀	Sprocket Hole Pitch	4.0 ± 0.1
D ₀	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P ₂		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A ₀	Pocket Dimensions	10.30 ± 0.20
B ₀		10.30 ± 0.20
K ₀		4.90 ± 0.20
W ₁	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

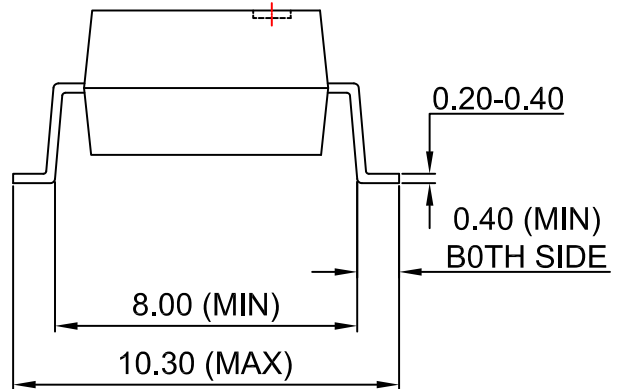
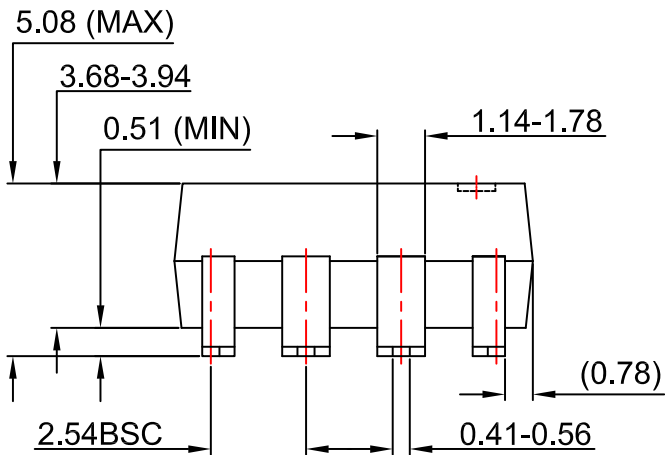
FOD3125

PACKAGE DIMENSIONS (OPTION S)

PDIP8 GW
CASE 709AC
ISSUE O



LAND PATTERN RECOMMENDATION



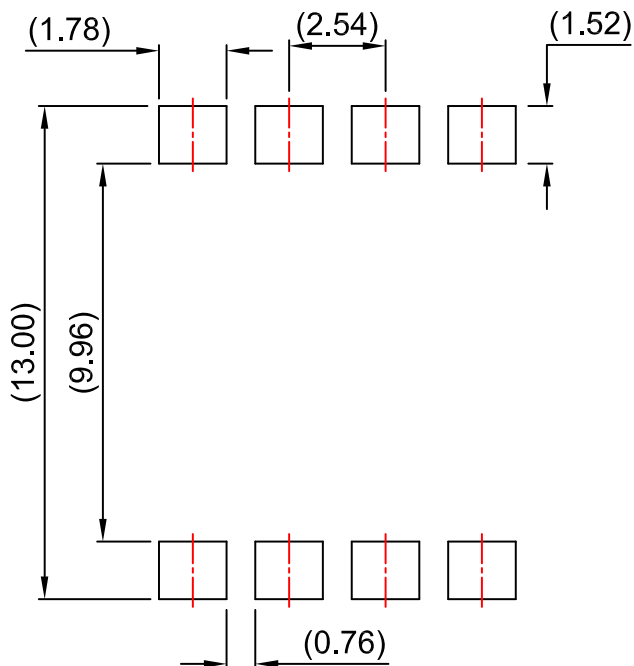
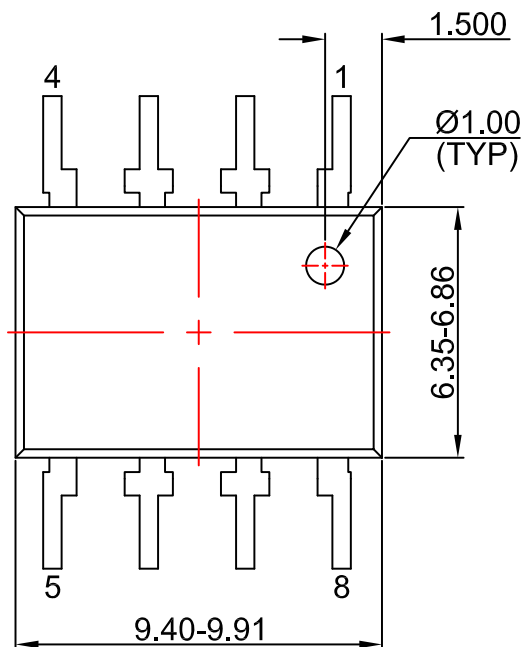
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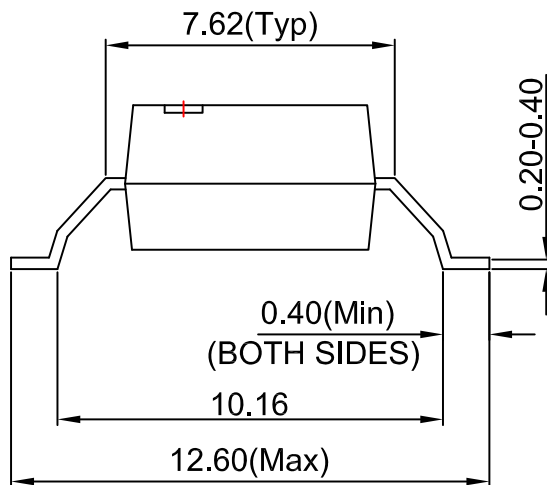
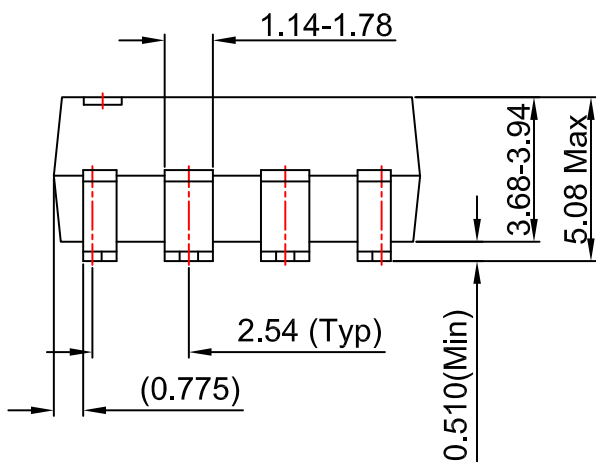
FOD3125

PACKAGE DIMENSIONS (OPTION TS)

PDIP8 GW
CASE 709AD
ISSUE O



LAND PATTERN RECOMMENDATION



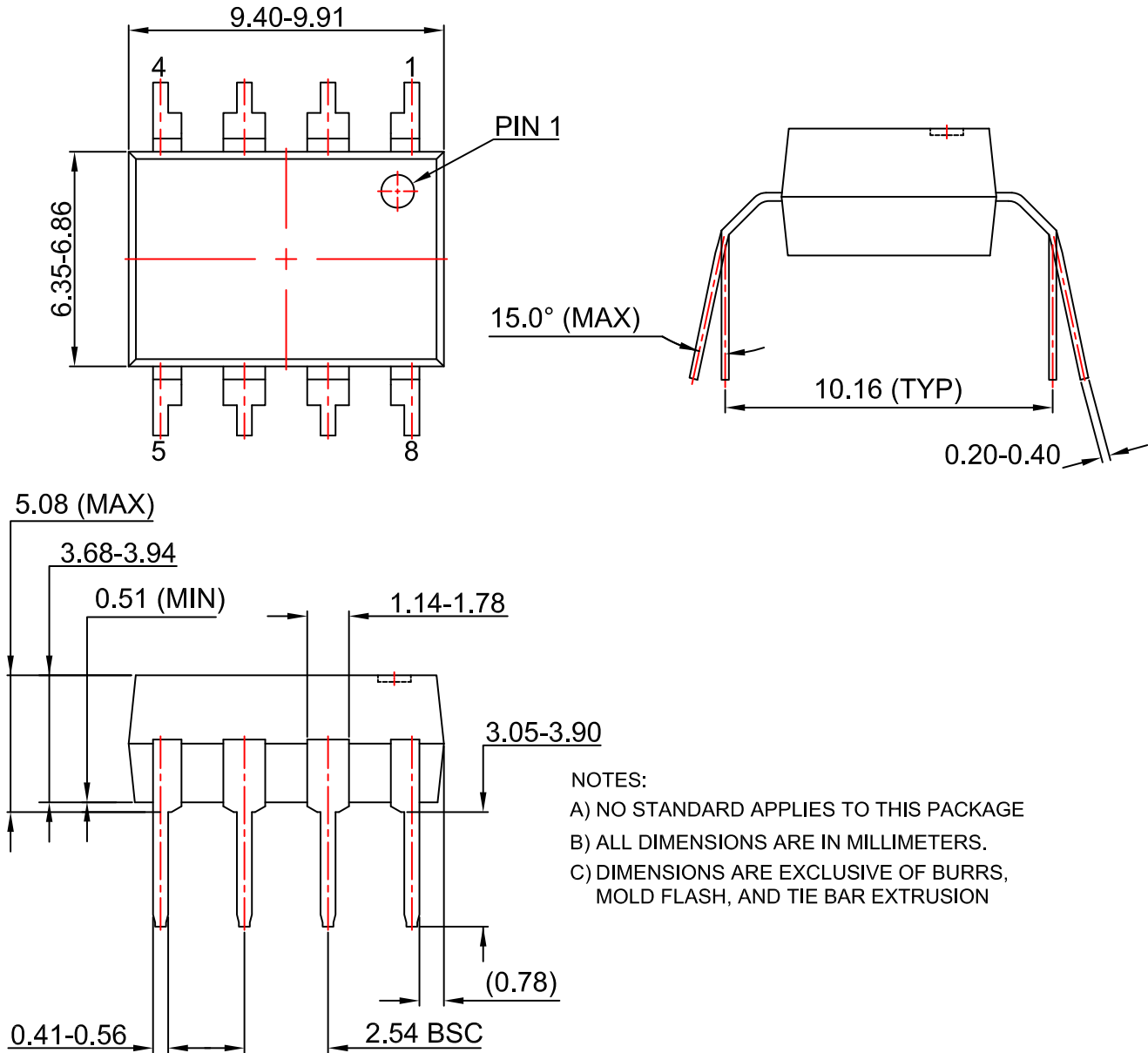
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FOD3125

PACKAGE DIMENSIONS (OPTION T)

PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

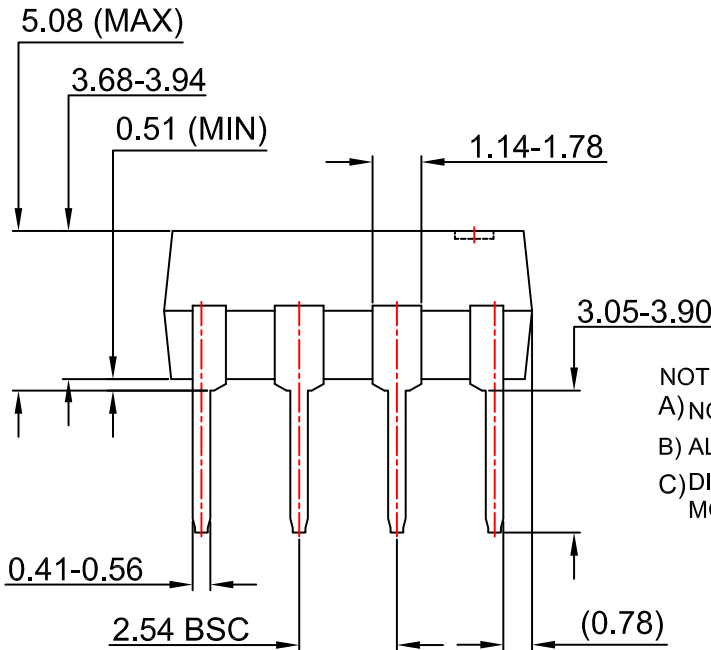
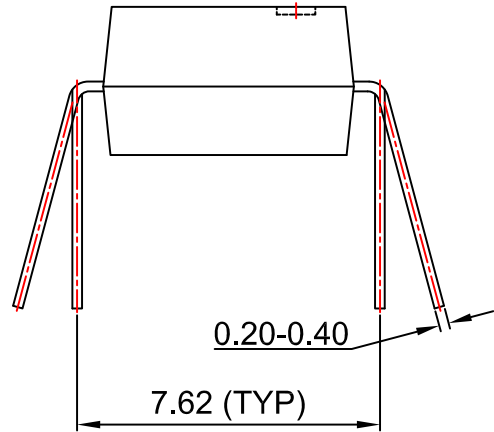
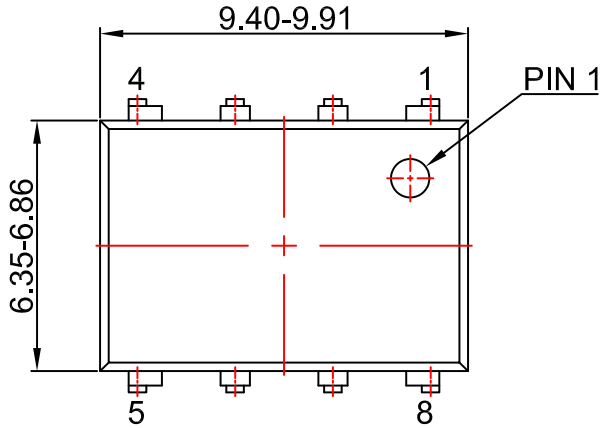


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FOD3125


PACKAGE DIMENSIONS

PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O



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