

BCT4567 Low-Power, Dual SIM Card Analog Switch

GENERAL DESCRIPTION

The BCT4567 is a quad-SPDT switch with one common control inputs targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

The switches are fully bi-directional, allowing both multiplexing and de-multiplexing operation. Break-before-make operation is guaranteed.

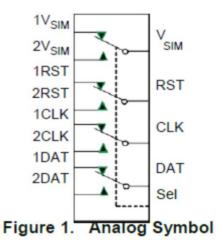
The device operates from a +1.65V to +4.5V supply and over the extended -40°C to +85°C temperature range. It is offered in 16-pin 3mm x 3mm TQFN package or 16-pin 1.8mm x 2.6mm UTQFN package.

APPLICATIONS

Dual SIM Card Switch Cell Phones Pad Digital Cameras PDAs Notebook

FEATURES

- Low 0.5Ω Ron @VCC=2.7V
- 0.06Ω On-Resistance Flatness
- Excellent 0.05Ω On-Resistance Matching
- Wide VCC Operating Range: 1.65 V to 4.5 V
- Rail-to-Rail Signal Switching Range
- Fast Switching Speed: 20nsTYP at 3.3V
- High Off Isolation: -66dB
- Crosstalk Rejection: -86dB
- -3dB bandwidth: 100MHz
- Space-Saving, TQFN 3x3-16L or UTQFN 1.8x2.6-16L Package

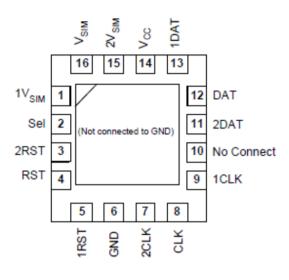


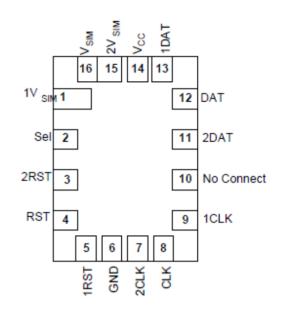
ORDERING INFORMATION

Ordering Code	Package Description	Temp Range	Top Marking	QTY/Reel
BCT4567EGE-TR	TQFN3x3-16L	–40°C to +85°C	4567	3000
BCT4567EFE-TR	UTQFN1.8x2.6-16L	–40°C to +85°C	4567	3000



Pin Configurations





Pin Description

Pin	Name	Function	
1	1VSIM	SIM supply output 2	
2	SEL	Select input	
3	2RST	RST Normally Open Terminal	
4	RST	RST Common Terminal	
5	1RST	RST Normally Closed Terminal	
6	GND	Ground	
7	2CLK	CLK Normally Open Terminal	
8	CLK	CLK Common Terminal	
9	1CLK	CLK Normally Closed Terminal	
10	NC	Not Connect	
11	2DAT	DAT Normally Open Terminal	
12	DAT	DAT Common Terminal	
13	1DAT	DAT Normally Closed Terminal	
14	VCC	Power Supply	
15	2VSIM	SIM supply output 1	
16	VSIM	SIM supply input	



Truth Table

SEL	SWITCH STATE
0	1DAT = DAT, 1RST = RST, 1CLK = CLK, $1V_{SIM} = V_{SIM}$
1	2DAT = DAT, 2RST = RST, 2CLK = CLK, $2V_{SIM} = V_{SIM}$

Absolute Maximum Ratings

VCC, SEL to GND	0.3V to +6.0V
All Other Pins to GND0.3	
Continuous Current	
Peak Current (pulsed at 1ms, 10% duty cycle)	±500mA
Continuous Power Dissipation (TA = +70°C) (15.6mW/°C above +70°C)	1.25W
Operating Temperature Range	40°C to +85°C
Storage Temperature Range	65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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Electrical Characteristics

(unless otherwise noted. Typical values are at VCC = 3.3V, TA = $+25^{\circ}C$. (Note 2)

Parameter	Symbol	Conditions		Min	Тур	Max	Units
POWER SUPPLY		1				1 1	
Supply Voltage Range	Vcc			1.65		4.5	V
Supply Current	Icc	$V_{CNTRL} = 0$ or V_{CC} , $I_{OUT} = 0$				1.0	uA
ANALOG SWITCH							
Analog Signal Range	Vsw	Switch I/O Voltage		0		VCC	V
On-Resistance	Ron	I _{ON} = -100 mA	VCC= 1.8V V _{SW} = 0, 1.8 V		0.8		Ω
		Figure 9	VCC= 2.7V V _{SW} = 0, 2.3 V		0.5		
On-Resistance Match		I _{ON} = -100 mA	VCC= 1.8V V _{SW} = 0, 1.8 V		0.1		Ω
	ΔRon	Figure 9	VCC= 2.7V V _{SW} = 0, 2.3 V		0.05		
On-Resistance RF Flatness		I _{ON} = -100 mA	VCC= 1.8V V _{SW} = 0, 1.8 V		0.12		Ω
	RFLAT	Figure 9	VCC= 2.7V V _{SW} = 0, 2.3 V		0.06		
Off-Leakage Current	IOFF	Vcc= 4.3V, nRST, nDAT, nCLK, nVSIM = 0.3 V or 3.6 V Figure 10		-1		1	uA
On-Leakage Current	ION	VCC= 4.3V, RST, DAT, CLK, VSIM = 0.3 V or 3.6 V		-1		1	uA
SEL DIGITAL INPUT	rs						
Input-Logic High	VIH	VCC=1.65V to 4.5V,	D	1.7	_		V
Input-Logic Low	VIL	VCC=1.65V to 4.5V,	0			0.4	V
nput Leakage Current	lin	VIN = 0 or VCC		-1		1	uA



Electrical Characteristics (continued) (unless otherwise noted. Typical values are at VCC = 3.3V, TA = $+25^{\circ}C$.) ⁽²⁾ Parameter Symbol Conditions Units Min Тур Max **DYNAMIC CHARACTERISTICS** $T_A = +25^{\circ}C$ $RL = 50 \Omega, CL = 35$ Turn-On Time 20 30 Pf, VSW = 1.5 V, Sel to Output Ton (VSIM,DAT,CLK, $T_A = T_{MIN}$ to Figure 11, Figure ns TMAX 50 RST) 12 $T_A = +25^{\circ}C$ Turn-Off Time $RL = 50 \Omega, CL = 35$ 15 40 Sel to Output pF, VSW = 1.5 V,TOFF (VSIM, DAT, CLK, RST) $T_A = T_{MIN}$ to Figure 11, Figure ns TMAX 50 12 $R_L = 50 \Omega, C_L =$ $T_A = +25^{\circ}C$ 35 pF V_{SW1} = 2 15 Break-Before-Make $V_{SW2} = 1.5 V$ Time $T_A = T_{MIN}$ to TRRM Figure 15 ns (VSIM, DAT, CLK, R T_{MAX} 2 ST) **Charge Injection** $C_{L} = 50 \text{ pF}, R_{GEN} = 0 \Omega, V_{GEN} = 0 V$ Q pC 100 On-Channel Bandwidth -3dB BW $R_L = 50 \Omega$, $C_L = 5 pF$ Figure 16 100 MHz (VSIM,DAT,CL K,RST) $R_L = 50 \Omega$, f = 100KHz Off-Isolation -66 dB Viso Figure 17 (VSIM, DAT, CLK, RST) $R_{L} = 50 \Omega$, f = 100KHz Crosstalk Vст -86 dB (VSIM, DAT, CLK, RST) Figure 18 VSIM,RST,CLK, DAT V_{CC} = 3.3 V, Figure 19 COFF 8 pF **Off Capacitance** VSIM,RST,CLK,DAT $V_{CC} = 3.3 V, f = 1 MHz$ 25 pF CON On Capacitance Figure 20

Note 2: Devices are 100% tested at TA = +25 $^{\circ}$ C. Limits across the full temperature range are guaranteed by design and correlation.



Test Diagrams / Timing Diagrams VON NC InA(OFF) nV_{SIM}, nRST, nCLK, or nDAT V_{SIM}, RST, CLK, or DAT A Т -V_{sw} sw **∀**GND GND GND = 0 or V V Sel V_{Sel} = 0 or V_{CC} Ron = Von / Ion Figure 9. On Resistance Figure 10. Off Leakage t_{FALL} = 2.5ns t_{RISE} = 2.5ns nV_{SIM}, nRST, V_{SIM}, RST, CLK, or DAT nCLK,ornDAT V_{cc}_..... 90% 90% V_{sw} \top Input - V_{Sel} /_{cc}/2 V_{cc}/2 dgND 10% 10% GND GND Sel V_{он _}. R and C are functions of the application 90% 90% Output - VOUT environment (see tables for specific values). C includes test fixture and stray capacitance. VOL ON

Figure 11. AC Test Circuit Load



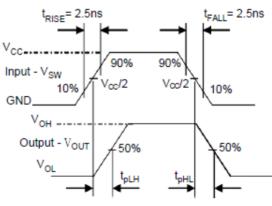


Figure 13. Propagation Delay

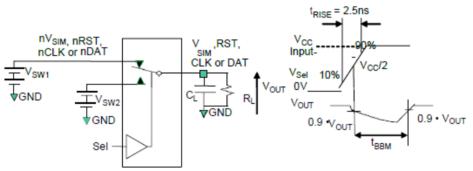


 $Q = \Delta V_{OUT} \cdot C_L$

Test Diagrams / Timing Diagrams

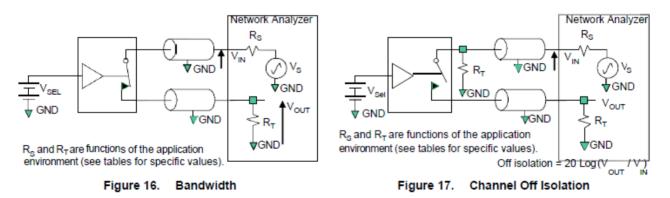
nV_{SIM}, nRST, V_{cc} -V., RST, nCLK, or nDAT Logic Input CLK, or DAT Off Off VSW 0V ḋGND \mathbf{C}_{L} Δνουτ ♥GND Vour Sel





 R_L and C_L are functions of the application environment (see tables for specific values). C_L includes test fixture and stray capacitance.







Test Diagrams /Timing Diagrams

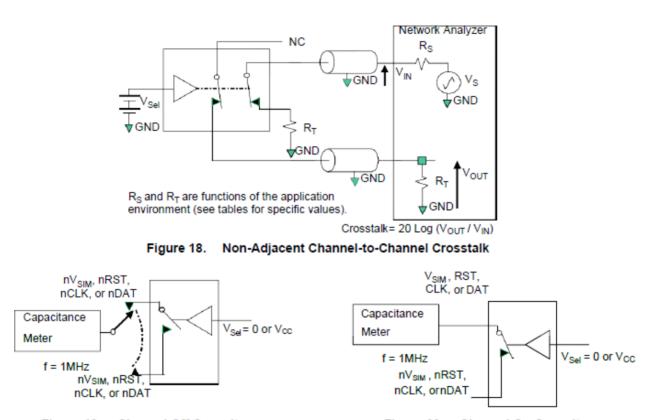
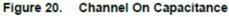


Figure 19. Channel Off Capacitance

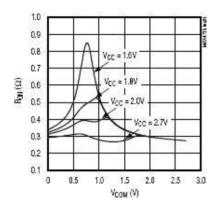




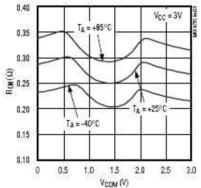
Typical Operating Characteristics

(VCC = 3V, TA = $+25^{\circ}$ C, unless otherwise noted.)

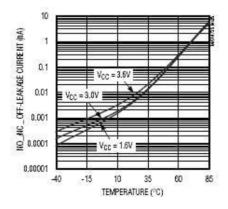
ON-RESISTANCE vs. COM_ VOLTAGE



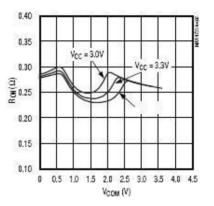
ON-RESISTANCE vs. COM_ VOLTAGE AND TEMPERATURE



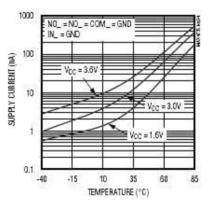
NO /NC OFF-LEAKAGE CURRENT vs. TEMPERATURE



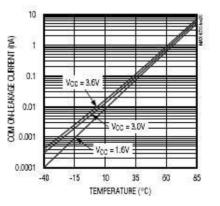
ON-RESISTANCE vs. COM_ VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



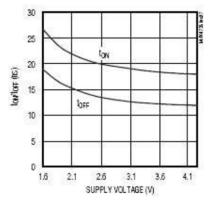
COM ON-LEAKAGE CURRENT vs. TEMPERATURE



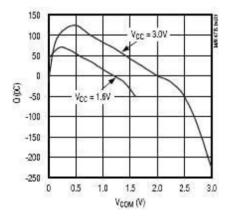
REV1.3 www.broadchip.com



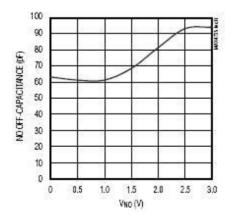
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



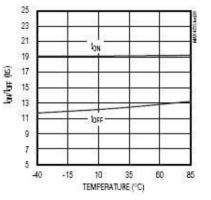
CHARGE INJECTION vs. COM_ VOLTAGE



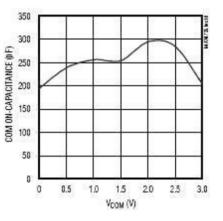
NO_ OFF-CAPACITANCE vs. NO_ VOLTAGE



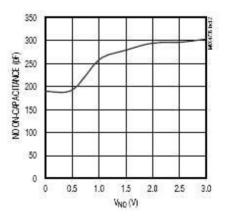
TURN-ON/OFF TIME vs. TEMPERATURE



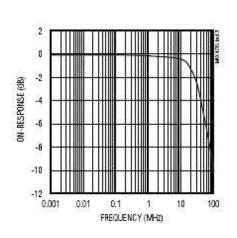
COM_ ON-CAPACITANCE vs. COM_ VOLTAGE



NO_ ON-CAPACITANCE vs. NO_ VOLTAGE

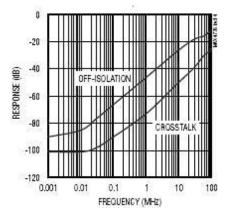






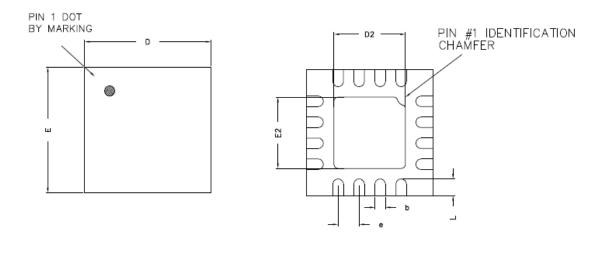
ON-RESPONSE vs. FREQUENCY

OFF-ISOLATION AND CROSSTALK vs. FREQUENCY



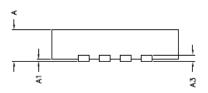


PACKAGE OUTLINE DIMENSIONS: TQFN 3x3 -16L



BOTTOM VIEW

TOP VIEW

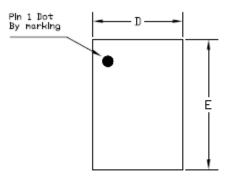


SIDE VIEW

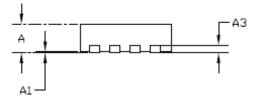
COMMON DIMENSIONS(MM)					
PKG.	W: VERY VERY THIN				
REF.	MIN.	NOM.	MAX		
A	0.70	0.75	0.80		
A1	0.00	-	0.05		
A3	0.2 REF.				
D	2.95	3.00	3.05		
E	2.95	3.00	3.05		
b	0.18	0.25	0.30		
L	0.30	0.40	0.50		
D2	1.55	1.70	1.80		
E2	1.55	1.70	1.80		
е	0.5 BSC				



PACKAGE OUTLINE DIMENSIONS: UTQFN 1.8x2.6 -16L







<u>SIDE VIEW</u>

COMMON DIMENSIONS(MM)					
PKG.	UT:ULTRA THIN				
REF.	MIN.	NDM.	МАХ		
Α	>0,50	0.55	0.60		
A1	0.00	_	0,05		
A3	0.15 RFF.				
D	1,75	1,80	1,85		
E	2.55	2.60	2,65		
L	0,30	0,40	0.50		
b	0.15	0.20	0,25		
e	0.40 BSC				