VP3881

High-Efficiency Boost/SEPIC/Flyback DC/DC Controller

General Description

The VP3881 is a versatile controller designed for use in Boost, SEPIC and Flyback power converter and topologies that needs an external low-side N-MOSFET acting as primary switch. Besides cycle-by-cycle current limiting, current mode control scheme also makes it wide bandwidth and good transient response. The current limit can be programmed simply with an external resistor.

The switching frequency can be set in any value between 100kHz and 1MHz with a resistor or any external clock source. The VP3881 can be operated at high switching frequency to save the solution board size. While entering shutdown mode, the VP3881 only sinks 10μA and it allows power supply sequencing. It has built-in protection circuits such as thermal shutdown, under-voltage lockout, short circuit protection, and overvoltage protection. Internal soft-start circuitry reduces the inrush current at start-up.

VP3881 is available in small DFN10 3x3 green package.

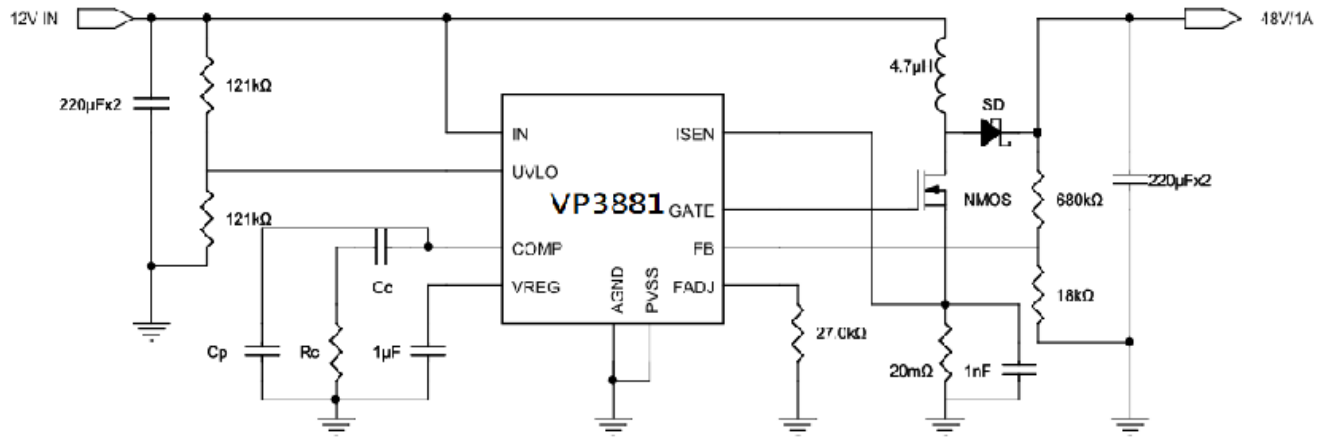
Features

- Wide Input Voltage from 2.97V to 60V
- Reference Voltage with ±3.0% Accuracy
- Adjustable 100kHz~1MHz Clock Frequency
- Wide Output Voltage up to 80V
- 10μA Shutdown Current
- 1A Peak Current Limit Using Internal Driver
- Current Mode Operation
- Internal 4/2Ω MOSFET Switch
- External RC Compensation
- Internal Soft-Start
- High Efficiency at Light Loads
- Cycle-By-Cycle Current Limit
- Over Temperature Protection
- Adjustable Input UVLO Threshold Voltage
- DFN10 3x3 Green Package with RoHS Compliant

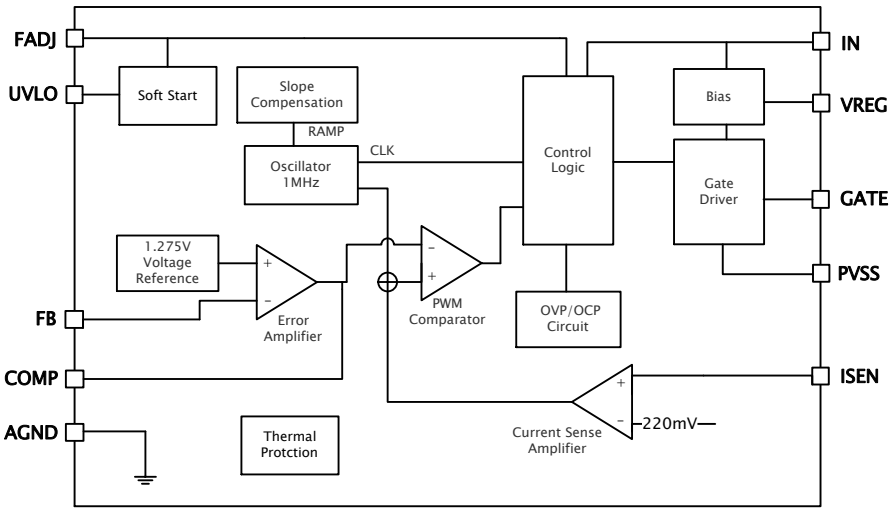
Applications

- Portable Speakers
- Offline Power Supply
- Battery Powered Device
- Automotive
- Photovoltaic Inverters

Typical Application

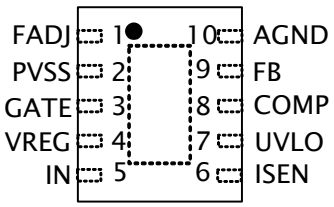


Functional Block Diagram



Pin Assignments And Descriptions

TDFN10
Top View



TDFN10	Pin	I/O/P	Function Description
1	FADJ	I	Frequency Adjust/Synchronization/Shutdown. A resistor connected from this pin to ground simply sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the clock. Pull on this pin for ≥ 30 μs will turn the device off and the device will then very few current about 5μA from the supply.
2	PVSS	P	Power Ground. Connect to exposed pad.
3	GATE	O	Gate Drive. Connect this terminal to the gate pin of the external MOSFET.
4	VREG	O	Drive Supply Voltage. A bypass capacitor must be connected from this pin to ground. Do not bias this pin with external power source.
5	IN	P	Power Supply Input.
6	ISEN	I	Current Sense. Use an external resistor in series with ground to measure the voltage drop.
7	UVLO	I	Under Voltage Lockout. Use a proper ratio resistor divider network to determine the voltage input to allow switching and the hysteresis to disable switching.
8	COMP	I	Compensation. Use an RC/C network to do proper loop compensation.
9	FB	I	Output Feedback. Connect the external resistor divider network from output to this pin to sense output voltage. The FB pin voltage is regulated to internal 1.275V reference voltage.
10	AGND	P	Analog Ground. Connect to exposed pad.

Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

Symbol	Parameter	Limit	Unit
V_{IN}	Supply voltage range	-0.3 to 65	V
V_{LV} (COMP/UVLO/FB/FADJ/ GATE)	Low voltage range	-0.3 to 6	V
V_{CC}(VREG)	Regulator output pin range	-0.3 to 5	V
V_{ISEN}	Current sense pin range	-0.4 to 0.6	V
T_{JMAX}	Junction temperature range MAX.	150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
Electrostatic discharge	Human body model	2	kV
Electrostatic discharge	Machine model	200	V

(*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

Recommended Operating Conditions

Symbol	Parameter	Specification		Unit
		Min	Max	
V_{IN}	Supply voltage	2.97	60	V
f_{OSC}	Switching voltage range	0.1	1	MHz
T_J	Operating Junction range	-40	125	°C

Thermal Information

Thermal Metric Parameter		LM3481DNG10	Unit
		TDFN	
$\theta_{JC(top)}$	Thermal resistance (Junction to Case (top))	54	°C/W
θ_{JA}	Thermal resistance (Junction to Air)	49	°C/W
θ_{JB}	Thermal resistance (Junction to Board)	21	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21	°C/W

Electrical Characteristics

V_{IN}=12V, R_{FADJ}=40kΩ, T_J=25℃, unless otherwise specified (* 1)

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ	Max	
V_{FB}	Feedback voltage	V_{COMP}=1.4V, 3V<V_{IN}<60V			1.275		V
I_{STBY}	Standby current in shutdown mode	V_{FADJ}=3V	V_{IN}=12V		14		μA
			V_{IN}=5V		10		
V_{UVLO}	Under voltage lockout	V_{UVLO} Ramp down		1.345		1.517	V
I_{UVLO}	UVLO source current	V_{EN} = 3V			4.5		μA
V_{UVLOSD}	UVLO Shutdown voltage			0.55	0.7	0.82	V
V_{COMP}	COMP pin voltage	V_{FB}=1.275V			1		V
$R_{DS(ON)}$	High-side switch $R_{DS(ON)}$ (*1)	V_{IN}=5V, I_{GATE}=0.2A			4		Ω
	Low-side switch $R_{DS(ON)}$ (*1)	V_{IN}=5V, I_{GATE}=0.2A			2		
A_{VOL}	Error amplifier voltage gain	V_{COMP}=1.4V, I_{EAO}=100μA			60		V/V
g_M	Error amplifier trans-conductance	V_{COMP}=1.4V			430		μ℧
V_{GATE}	Maximum GATE driving swing	V_{IN}<5.8V			V_{IN}		V
		V_{IN}≥5.8V			5.2		
f_{OSC}	Oscillation frequency	R_{FADJ}=40kΩ		0.4	0.475	0.555	MHz
D_{MAX}	Maximum duty cycle	R_{FADJ}=40kΩ			85		%
ΔV_{LINE}	Voltage line regulation	3V<V_{EN}<60V			0.02		%/V
ΔV_{LOAD}	Voltage load regulation	I_{EAO} Source/Sink			±0.5		%/A
$t_{MIN(ON)}$	Minimum on-time					571	nS
I_{SUPPLY}	Supply Current	R_{FADJ}=40kΩ			3.3		mA
V_{SENSE}	Current sense threshold voltage			120	170	200	mV
V_{SC}	Overload current limit sense voltage			160	200	350	mV
V_{SL}	Internal compensation ramp				90		mV
V_{OVP}	Output overvoltage protection	V_{COMP}=1.4V		26	85	135	mV
$V_{OVP(HYS)}$	Output overvoltage protection hysteresis	V_{COMP}=1.4V		28	70	106	mV

Electrical Characteristics (cont.)

V_{IN}=12V, R_{FADJ}=40kΩ, T_J=25℃, unless otherwise specified (* 1)

Symbol	Parameter	Test Condition	Specification			Unit
			Min	Typ	Max	
I_{EAO}	Error amplifier output current (Source/Sink)	Source,V_{COMP} = 1.4V, V_{FB} = 0V	450	525	700	μA
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V	80	110	140	
V_{EAO}	Error amplifier output voltage	Upper Limit V_{FB}=0V, COMP pin floating		2.5		V
		Lower Limit V_{FB}=1.4V		0.78		
V_{SD}	Shutdown signal threshold on FADJ pin(*2)	Output = High Level ; Chip Disable		1.26		V
		Output = Low Level ; Chip Enable		0.63		
t_{SS}	Soft start delay	V_{FB} = 1.2V, COMP pin floating	8.7	15	21.3	mS
t_R	GATE pin rising time	Cgs = 3000pF, V_{GATE} = 0V to 3V		18		nS
t_F	GATE pin falling time	Cgs = 3000pF, V_{GATE} = 3V to 0V		12		nS
I_{SD}	Shutdown pin current FADJ pin	V_{SD}=0V		10		μA
T_{SD}	Thermal shutdown			175		℃
$T_{SD(HYS)}$	Thermal shutdown hysteresis			10		℃

(*1): Stress beyond those listed at “absolute maximum rating” table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up “recommended operation conditions” table.
(*2) The FADJ pin should be pulled to VIN through a resistor to turn the regulator off. The voltage on the FADJ pin must be above the maximum limit for Output = High Level to keep the regulator off and must be below the limit for Output = Low Level to keep the regulator on.

Functional Descriptions

The VP3881 employs the current-mode, adjustable frequency pulse-width modulation (PWM) architecture. It operates at adjustable switching frequency under medium to high load current conditions.

Overvoltage and UVLO Protection

The VP3881 uses FB pin to detect overvoltage occurrence. The overvoltage protection should be triggered at the voltage rises to $V_{FB}+V_{OVP}$. When OVP occurs only the MOSFET will be turned off, the output voltage will drop. VP3881 will switch when the voltage on FB pin is less then ($V_{OVP}+V_{FB}-V_{OVP(HYS)}$).

The VP3881 provides UVLO pin to program enable and disable thresholds. The voltage on UVLO pin would be compared with internal reference 1.43V. Figure 1 shows how the UVLO detection works.

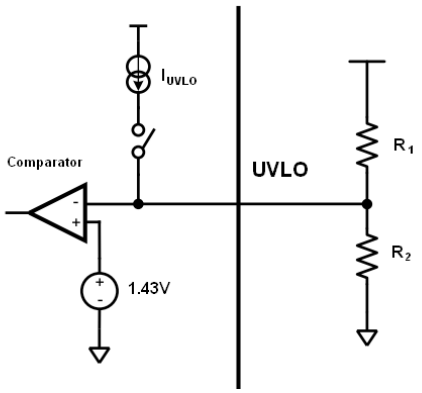


Figure 1. UVLO Pin Configuration

The R1/R2 network programs the enable threshold voltage V_{EN}. When the VP3881 is enabled the I_{UVLO} will source 4.5μA current flows the R_2 which causes a hysteresis. Hence the disable threshold, V_{SH}, is lower then the enable threshold V_{EN}.

$$R_2 = \frac{1.43V}{I_{UVLO}} \times \left(1 + \frac{1.43V - V_{SH}}{V_{EN} - 1.43V}\right)$$

$$R_1 = R_2 \times \left(\frac{V_{EN}}{1.43V} - 1\right)$$

Select appropriate value of V_{EN}, V_{SH} and use above two equations to determine the value of R_1 and R_2.

Bias Voltage

VP3881 generates the internal bias voltage from IN input voltage if it does not exceeds 6V. When V_{IN} is higher then 6V the VP3881 will use internal regulation to bias the chip. To improve the stability of the bias, an external capacitor of 0.47μF~4.7μF is strongly recommended to add on VREG terminal.

In any case, do not add external voltage on VREG pin or the chip would be damaged.

Frequency Adjust

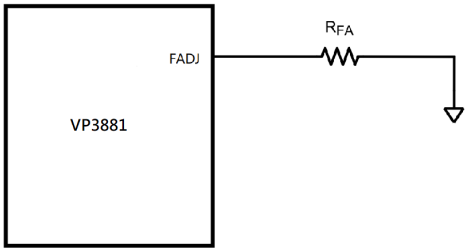


Figure 2. Frequency Adjustment

As shown in figure 2, the switching frequency can be adjusted from 100kHz to 1MHz by an external resistor in series with FADJ terminal and ground. The following equation is used to calculate resistor value.

a. When Fs < 300KHz the calculate as below,

$$R_{FADJ} = \frac{23\times10^3}{f_s} - 6.76$$

b. When Fs > 300KHz the calculate as below,

$$R_{FADJ} = \frac{23\times10^3}{f_s} - 8.76$$

Where f_S is in kHz and R_{FADJ} is in kΩ.

Clock Synchronization

With internal RC oscillator, VP3881 is able to be synchronized to an external clock by connecting to the FADJ terminal with R_{FADJ} in series with ground as

Functional Descriptions (cont.)

shown in figure 3.

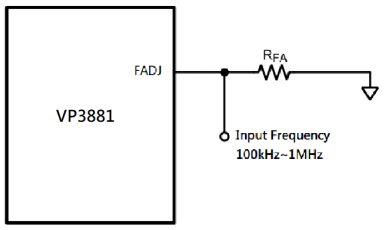


Figure 3. Clock Synchronization

Shutdown

The FADJ pin can be used as a shutdown pin. If the high signal pulls up this pin, VP3881 will stop the switching and then enter the shutdown state. In this state, VP3881 consumes only 10μA typically.

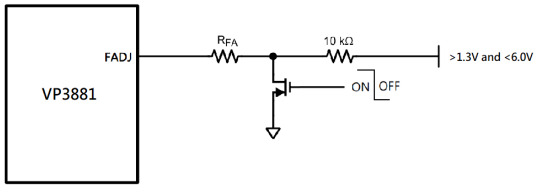


Figure 4. Shutdown Operation

The use of shutdown control in frequency adjustment mode is quite simple. Connects the FADJ pin to ground will force the VP3881 runs at specified frequency and pulls this pin high will shutdown the IC. In both frequency and synchronization mode, pulls FADJ pin high lasting then 30us will also force the VP3881 enter the shutdown state. An example is shown in figure 4. However, the voltage on the FADJ pin should be always less than the absolute maximum of 6 V to avoid any damage to the device.

Slope Compensation

VP3881 employs current mode control scheme. It has many advantages such as cycle-by-cycle current limit for the switch and easier to parallel power stages because automatic current sharing. The compensation ramp is already added in VP3881 and the slope of the default compensation ramp could satisfy most applications.

Overvoltage Protection

The VP3881 has overvoltage protection for the output. OVP occurrence is detected by sensing feedback (FB) pin. When the voltage at FB pin is over $V_{FB}+V_{OVP}$, overvoltage protection is triggered and the drive pin and the GATE pin will be tied-low.

Once the voltage at FB pin is lower then $V_{FB}+(V_{OVP}-V_{OVP(HYS)})$, the VP3881 will begin to switch again. Be aware that the error amplifier is still in operation during OVP event.

Short Circuit Protection

The ISEN pin is used to sense the over-current occurrence. If the difference between ISEN pin and ground is greater then 200mV, the current limit will be activated. The comparator will decrease the switching frequency by the factor of 8 and maintains this condition until the over-current (short) event is removed.

Programming Output Voltage

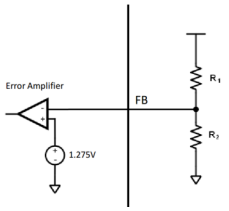


Figure 5. FB Pin Resistor Network

While enabling the VP3881, the voltage divider taped to FB pin programs the default output voltage with the equation:

$$V_{OUT} = 1.275V \times \frac{R_2 + R_1}{R_2}$$

In real application, keep R_2 around 10~20kΩ and select R_1 according to the required output voltage. Place the voltage divider near the FB pin and keep the connecting trance away from the noisy nodes like GATE.

Application Information

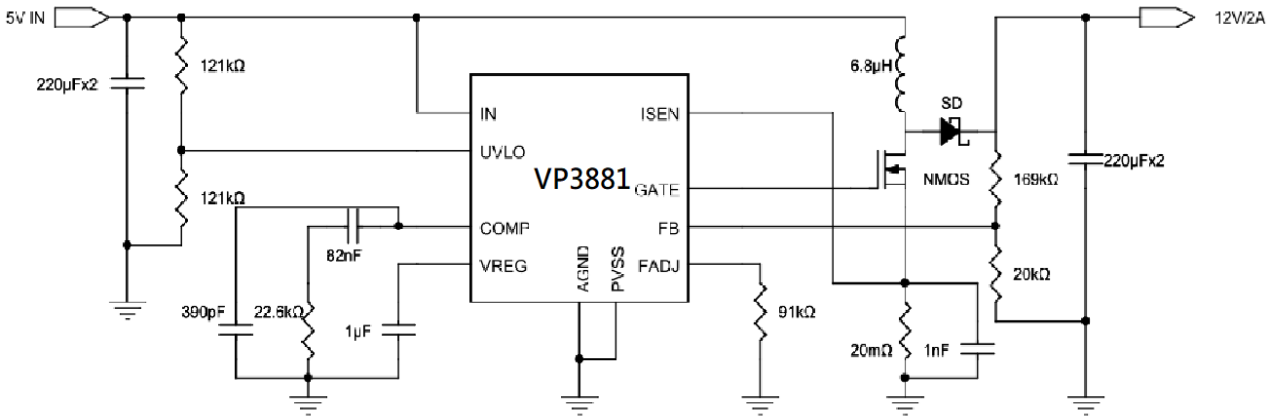


Figure 6. VP3881 Typical Boost Application

Basic Boost Operation

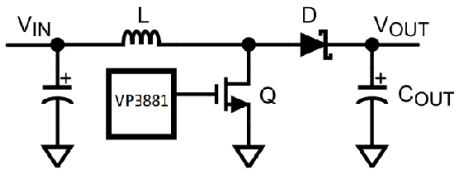


Figure 7. Simplified Boost Topology.

The most widely used topology of VP3881 is the boost operation and its simplified topology is shown in figure 7. The boost regulator operates in two cycles. In first cycle, the N-CH MOSFET is turned on and the energy is stored in the inductor and the load current is only supplied by the output capacitor due to the diode is reverse biased. Equivalent circuit is shown in figure 8. In the other cycle, the N-ch MOSFET is turned off and the energy stored in the inductor would be passed to the output capacitor (and the load). See figure 9 for equivalent circuit. Since the duty cycle is the on time/off time ratio of MOSFET. The output voltage can be obtained by:

$$V_{OUT} = \frac{V_{IN}}{1-D}$$

Considering the voltage drop across the MOSFET and the Schottky diode:

$$V_{OUT} + V_D - V_Q = \frac{V_{IN} - V_Q}{1-D}$$

Where V_D is the forward voltage drop of the Schottky diode, and the V_Q is channel voltage drop of the N-CH MOSFET.

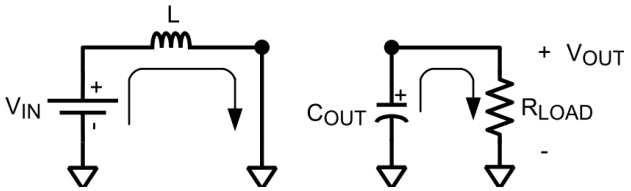


Figure 8. Boost operation when MOSFET is on

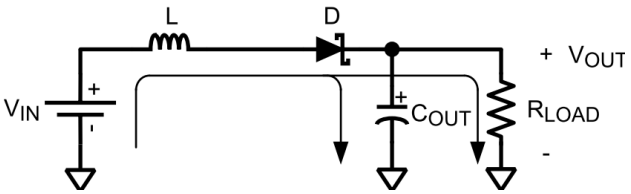


Figure 9. Boost operation when MOSFET is off

To calculate a cost-effective boost system, several parameters needed to be well considered: Input voltage (V_{IN}), output voltage (V_{OUT}), output current (I_{OUT}) and PWM switching frequency (f_{PWM}). Hence the parameter of the components should be carefully chosen with proper calculation.

Power Inductor Selection

The inductor storages and releases energy in every cycle of the PWM switching cycle. A core size with higher rating should be selected. If the core is not properly applied, core saturation or high

Application Information (cont.)

wire resistance will result bad efficiency. Please refer VP3881 EVB User Guide for calculating guidelines.

The VP3881 PWM frequency can be set at high frequency. To minimize the inductor size, it is simply to increase the switching frequency. However, the peak current of the inductor can be extremely larger then the output current, especially under light load conditions.

Diode Selection

The selection of the diode is based on two parameters: peak reverse voltage and average current. The peak diode reverse voltage for a boost regulator is simply equal to the output voltage plus reasonable safety margin. The diode current contains both the output load current and peak inductor current. The diode must be able to handle more then the inductor peak current. The peak current is obtained by the following formula:

$$I_{D(Peak)} = \frac{I_{OUT}}{1-D} + \Delta i_L$$

Where I_{OUT} is the output current and Δi_L is the peak inductor current.

The diode could be a dominator of power efficiency. To improve the efficiency, it is recommended to use a lower V_F Schottky diode with good heat sinking package.

MOSFET Selection

The maximum drain to source voltage of the N-ch MOSFET must be greater then the output voltage in boost operation since the V_{DS} is approximately equal to the output voltage when the MOSFET is off.

The on-state channel resistance $r_{DS(ON)}$ of the N-ch MOSFET is proportional to the conduction loss by the following equation:

$$P_{LOSS\_COND(MAX)} = \left(\frac{I_{OUT(\max)}}{1-D_{MAX}}\right)^2 D_{MAX} \cdot r_{DS(ON)}$$

where D_{MAX} is the maximum duty cycle.
And the switching loss may be the major portion of the total power loss while increasing the switching frequency. Since it is very difficult to estimate due to dynamic characteristics of the MOSFET, it is better to choose the MOSFET which parameter has lower Q_{GD} and Q_{GS} in general cases.

Input Capacitor Selection

The input capacitor should be capable of handling the average current. Although the input capacitor is not critical in a boost application, lower capacitance values could cause impedance interactions. A good quality of low ESR capacitor should be chosen in range of 100μF to 220μF.

In order to minimize the noise disturbance especially V_{IN} is lower than 8V, it is good to use a 20Ω and a 0.1μF bypass capacitor close attached to IN pin. The typical connection is shown in figure 10.

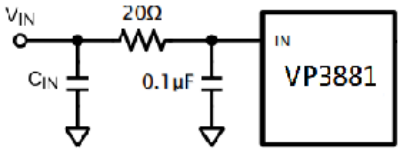


Figure 10. Input Bypassing Circuit

Output Capacitor Selection

The output capacitor in the boost operation shall provides all the output current while the MOSFET is off and needs the ability to handle the large output currents. The RMS current of the output capacitor is:

$$I_{C\_OUT(RMS)} = \sqrt{(1-D)\left[I_{OUT}{}^2 \frac{D}{(1-D)^2} + \frac{\Delta i_L{}^2}{3}\right]}$$

Application Information (cont.)

where $\Delta i_L=(V_{IN}*D)/(2*L*f_{PWM})$

It is recommended to use low ESR and ESL capacitors at output for improving efficiency and reducing ripple voltage. Surface mount tantalums, OSCON or multi-layer ceramic capacitors are usually chosen for better performance.

VREG Capacitor Selection

As described in function description, the VREG pin needs to be bypassed with a capacitor which has good performance in high frequency. It supplies the transient current required by the gate driver. The range of 0.47μF to 4.7μF multi-layer ceramic capacitor would be good for most cases. Please note the capacitor shell be place close to the VREG pin.

Application Information (cont.)

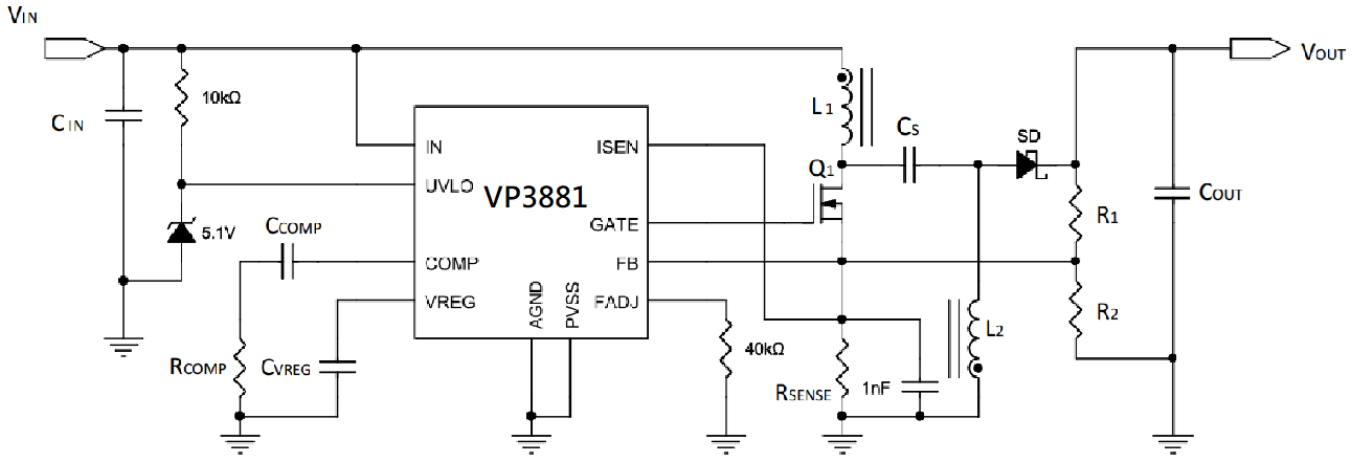


Figure 11. VP3881 Typical SEPIC Application

Basic Operation

VP3881 can also be used in SEPIC application because of it controls low-side of NMOSFET. Figure 11 shows the VP3881 typical SEPIC application. This configuration allows the input voltage higher or lower then output voltage. For both stepping-up and stepping-down configuration, two inductors are needed. The two inductors can be individual inductor or two windings of a coupled transformer. For reducing input ripple it is better to use the coupled windings of transformers for both inductors.

The advantage of SEPIC structure over a boost converter is input and output isolation. The input and the output of pure boost converter is always connected through an inductor unless external switch is added. For SEPIC structure, a capacitor isolates the input from the output and provides protection against shorted or malfunctioning load. Hence, the SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In pure boost converter, the output can only fall to the input voltage minus a diode drop and never turn off the output.

To properly pick up the components for the application, the following parameters need to be examined: Input voltage range, output voltage, output current range and the switching frequency. These four main parameters will affect the operating characteristic of the application.

MOSFET Selection

Four parameters will dominate the selection of the MOSFET: minimum threshold voltage $V_{TH(MIN)}$, the On-resistance $R_{DS(ON)}$, the total gate charge Qg, the reverse transfer capacitance Css and the maximum drain to source voltage $V_{DS(MAX)}$.

The peak switch voltage in SEPIC application is:

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE}$$

Hence the VDS(MAX) of MOSFET shell be:

$$V_{DS(MAX)} > V_{SW(PEAK)}$$

The peak switch current is determined by:

$$I_{SW(PEAK)} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2}$$

Where ΔI_{L1} and ΔI_{L2} are the peak-to-peak ripple currents of the inductors respectively.

The RMS current through the switch is given by:

$$I_{SW(RMS)} = \sqrt{\left[I_{SW(PEAK)}^2 - I_{SW(PEAK)}(\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3} \right] D}$$

Application Information (cont.)

Power Diode Selection

The diode must be selected to handle the peak current and the peak reverse voltage. In SEPIC application, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is $V_{IN}+V_{OUT}$. Similar to the boost converter, the average diode current is equal to the output current. In order to improve the efficiency, Schottky diodes are recommended.

Inductor Selection

The inductors shall be chosen carefully to satisfy constant current mode requires calculations of the following parameters:

Inductor average current:

$$I_{L1(AVG)} = \frac{D \times I_{OUT}}{1-D}$$

$$I_{L2(AVG)} = I_{OUT}$$

Peak-to-peak ripple current:

$$\Delta I_{L1} = \frac{D \times (V_{IN} - V_O)}{f_S \times L_1}$$

$$\Delta I_{L2} = \frac{D \times (V_{IN} - V_O)}{f_S \times L_2}$$

Maintaining the condition $I_L > \Delta I_L/2$ to ensure continuous conduction mode yields the following minimum values for L_1 and L_2:

$$L_1 > \frac{(1-D) \times (V_{IN} - V_O)}{f_S \times I_{OUT} \times 2}$$

$$L_2 > \frac{D \times (V_{IN} - V_O)}{f_S \times I_{OUT} \times 2}$$

Peak current in the inductor, to ensure the inductor does not saturate:

$$I_{L1(PK)} = \frac{D \times I_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2}$$

$$I_{L2(PK)} = I_{OUT} + \frac{\Delta I_{L2}}{2}$$

$I_{L1(PK)}$ must be lower than the maximum current rating set by the current sense resistor.

The value of L_1 can be increased above the minimum recommended value to reduce input ripple and output ripple. However, once ΔI_{L1} is less than 20% of $I_{L1(AVG)}$, the benefit to output ripple is minimal.

By increasing the value of L_2 above the minimum recommendation, ΔI_{L2} can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2} \right) \times ESR$$

where ESR is the equivalent series resistance of the output capacitor.

If L_1 and L_2 are wound on the same core, then $L_1=L_2=L$. All the equations above will hold true if the inductance is replaced by 2L.

Input Capacitor Selection

Like boost structure, SEPIC has an inductor at the input. The inductor ensures that the input capacitor sees fairly low ripple currents and the capacitor should be capable of handling the input RMS current. In SEPIC application, lower values can cause impedance interactions. Therefore a good quality capacitor such as polymer tantalum, OS-con or multilayer ceramic capacitors is recommended in the range from 100 µF to 220 µF.

To improve the performance especially when V_{IN} is under 8V, the input RC low pass filter could be added. Refer the input capacitor selection in boost controller application for details.

Output Capacitor Selection

The output capacitors directly affect the output

Application Information (cont.)

ripple. Use capacitors with low ESR and ESL at the output for higher efficiency and lower ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, OS-Con, or multi-layer ceramic capacitors are recommended at the output for low ripple.

Sense Resistor Selection

The peak current through the MOSFET, $I_{SW(PEAK)}$, can be adjusted using the current sense resistor, R_{SEN} , to limit at certain output current. R_{SEN} can be selected using the following equation:

$$R_{SEN} = \frac{V_{SENSE} - D \times (V_{SL} + \Delta V_{SL})}{I_{SW(PEAK)}}$$

SEPIC Capacitor Selection

The SEPIC capacitor C_S depends on the SEPIC RMS current listed below:

$$I_{SEPIC(RMS)} = \sqrt{I_{SW(RMS)} + (I_{L1(PEAK)} - I_{L1(PEAK)}\Delta I_{L1} + \Delta I_{L1}{}^2)(1-D)}$$

The voltage rating of the SEPIC capacitor must be greater then the maximum input voltage, and the AC(RMS) current flows through the capacitor is relative to the output power. The best choice are tantalum capacitors because of the high RMS current ratings relative to size. Large value of ceramic capacitors could be used, lower value capacitor will cause larger changes in voltage across the capacitor due to the higher current and results in low conversion efficiency. There exists an energy balance between SEPIC capacitor C_S and L_1. Consider the energy balance and the ripple voltage across the SEPIC capacitor, the minimum value for C_S can be given by:

$$C_S \geq L_1 \frac{I_{OUT}{}^2}{V_{IN} - V_{OUT}}$$

Input Capacitor Selection

Like the boost application, the input inductor L1 causes the input current waveform is continuous and triangle. The inductor also ensures that the input capacitor seems fairly low ripple current changes. But the input capacitor shall be large enough to handle the RMS current. A good quality capacitor in range of 100µF to 220µF should be selected to prevent impedance interactions or switching noise. Just like boost operation, an RC bypass circuit shown in figure 9 is good to be place close to IN pin to improve performance especially when V_{IN} below 8V.

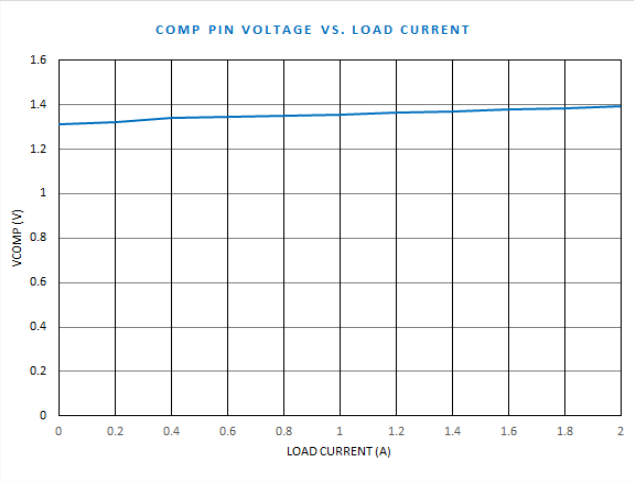
Output Capacitor Selection

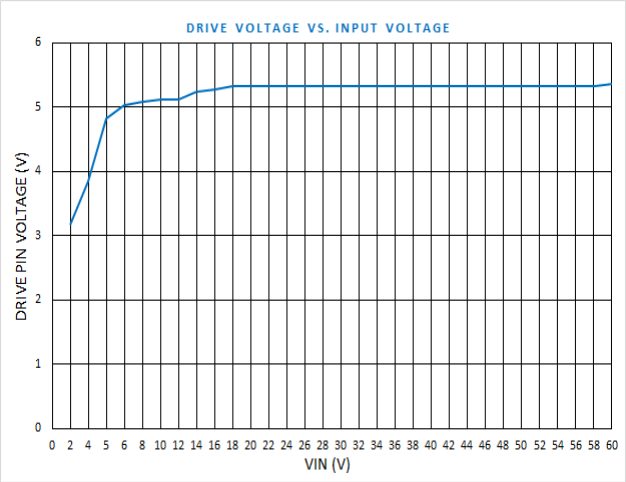
The selection of output capacitor is also like the boost operation. The output capacitor shall have the ability to handle large ripple currents. The RMS current through the output capacitor is:

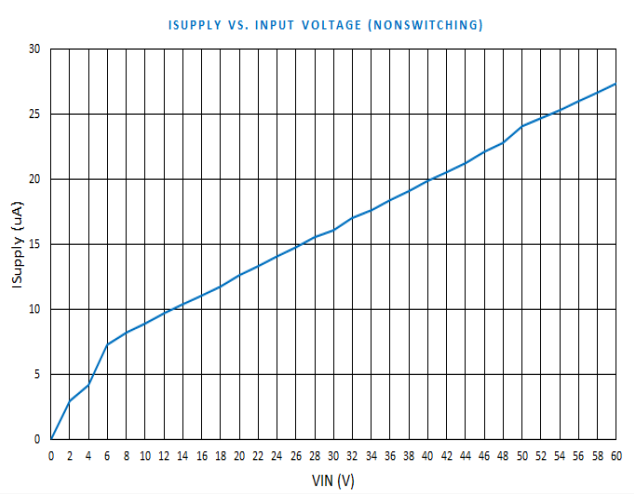
$$I_{C\_OUT(RMS)} = \sqrt{\left[I_{SW(PEAK)}{}^2 - I_{SW(PEAK)}(\Delta I_{L1} + \Delta I_{L1}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3}\right](1-D) - I_{OUT}{}^2}$$

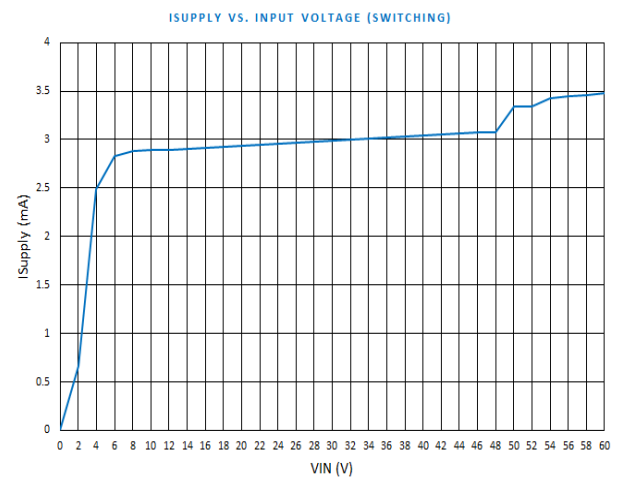
It is recommended to use low ESR and ESL capacitors at output for improving efficiency and reducing ripple voltage. Surface mount tantalums, OS-CON or multi-layer ceramic capacitors are usually chosen for better performance.

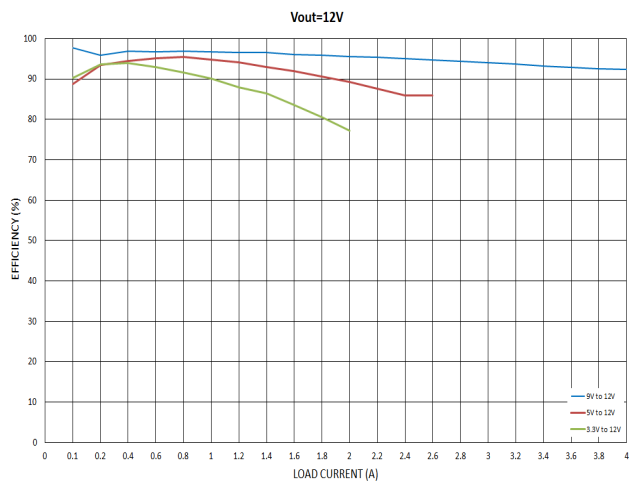
Typical Characteristic

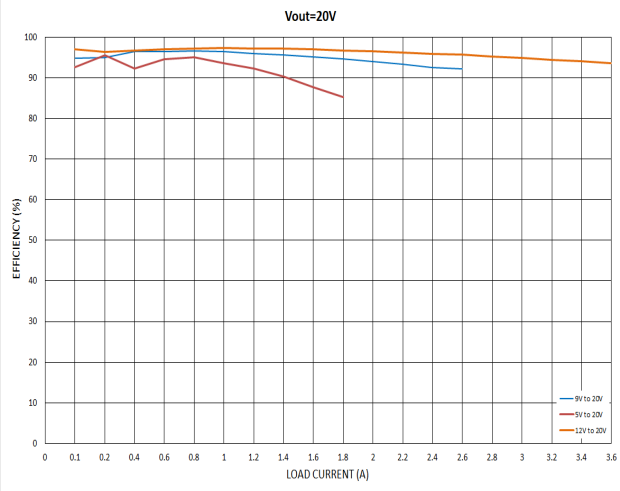




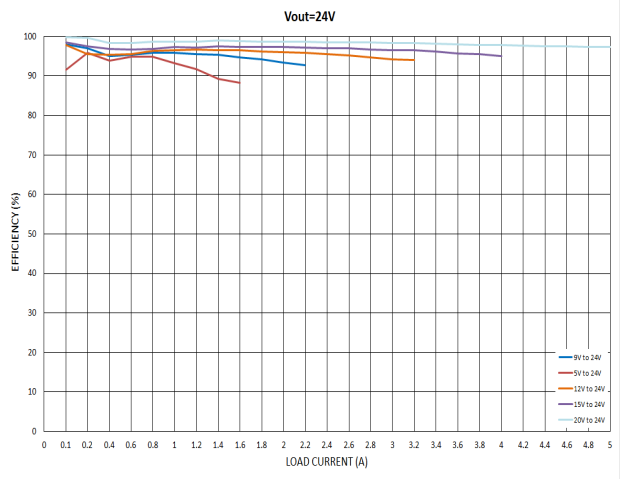


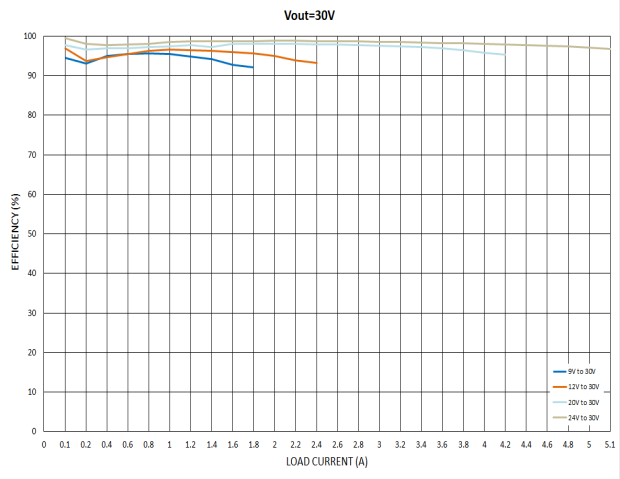


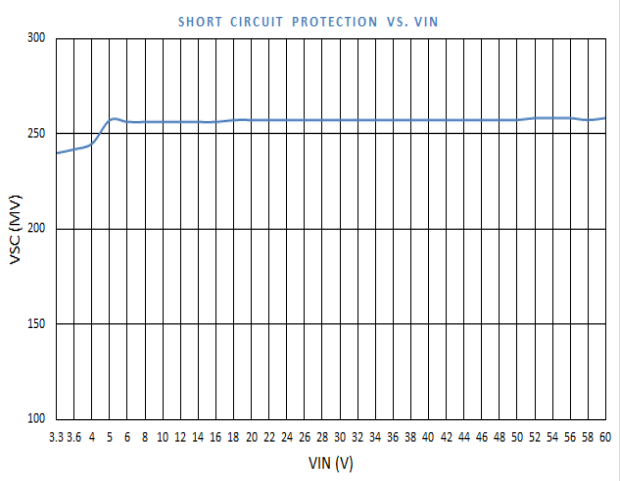


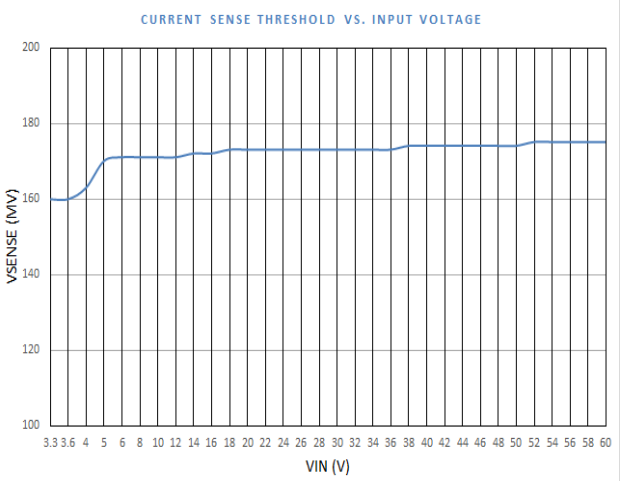


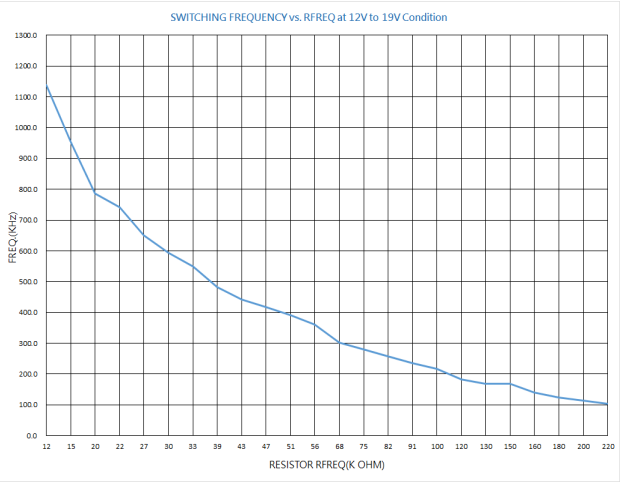
Typical Characteristic (cont.)





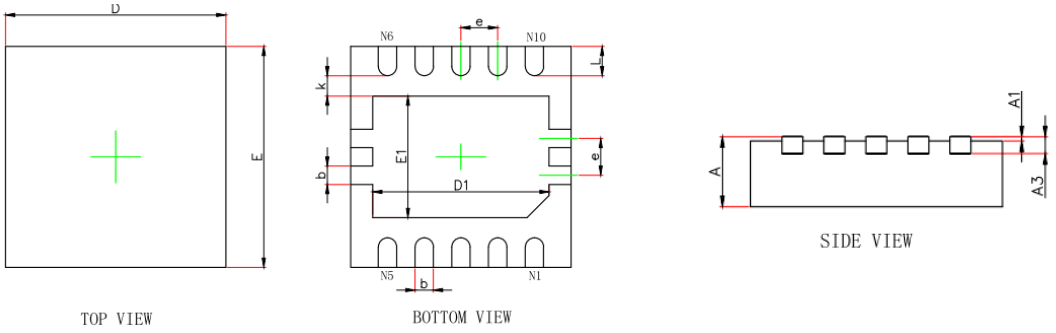






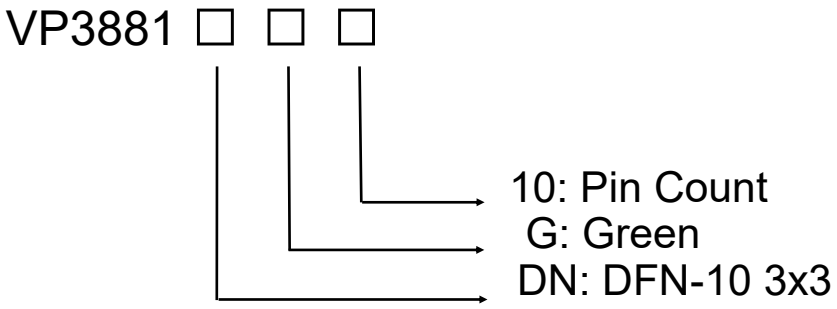
Package Information

TDFN10



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.300	2.500	0.091	0.098
E1	1.550	1.750	0.061	0.069
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

Ordering Information



Part No.	Q`ty/Reel
VP3881DNG10	2,500

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