Ultra Fast High PSRR

Low Noise CMOS Voltage Regulator

LR5213 Series

■ INTRODUCTION

The LR5213 series are a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection, ultra low noise, low power consumption and low dropout voltage, which can prolong battery life in portable electronics. The LR5213 series work with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications. The LR5213 series consume less than 0.1μA in shutdown mode and have fast turn-on time less than 50μs.The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

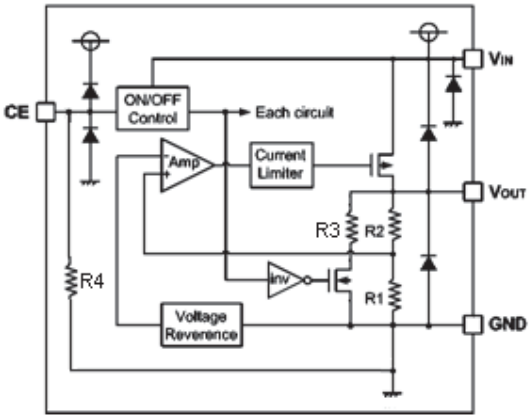
■ FEATURES

- Low Output Noise：
  40μV_{RMS}(10Hz~100kHz)
- Low Dropout Voltage：50mV@100mA
- Low Quiescent Current：50μA
- High Ripple Rejection：80dB@10kHz
- Excellent Line and Load Transient Response
- Operating Voltage Range：1.8V～6.0V
- Output Voltage Range：1.05V ~ 5.0V
- High Accuracy：±2%（Typ.）
- Built-in Current Limiter, Short-Circuit Protection
- TTL- Logic-Controlled Shutdown Input

■ APPLICATIONS

- Cellular and Smart Phones
- Laptop, Palmtops and PDA
- Digital Still and Video Cameras
- Portable Audio Video Equipments
- Radio control systems
- Battery-Powered Equipments

■ BLOCK DIAGRAM



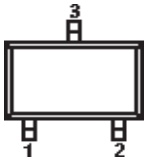
■ ORDER INFORMATION

LR5213①②③④⑤

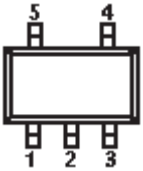
DESIGNATOR	SYMBOL	DESCRIPTION
①	A	Without EN
	B	High Active, pull-down resistor R4 built in, with C_{OUT} discharge resistor
	C	High Active, No pull-down resistor No C_{OUT} discharge resistor
②③	Integer	Output Voltage e.g.1.05V=② ③A1 e.g.1.8V=②③:18
④	M/MA/MC/MY	Package:SOT-23-3
	M/MF/ML	Package:SOT-23-5
	P/PT	Package:SOT-89-3
	F	Package:DFN1×1-4
⑤		2% Accuracy
	1	1% Accuracy

■ PIN CONFIGURATION

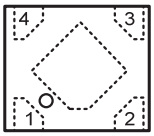
SOT-23-3



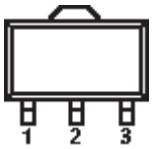
SOT-23-5



DFN1×1-4



SOT-89-3



SOT-23-3

PIN NUMBER				SYMBOL	FUNCTION
M	MA	MC	MY		
1	2	3	3	V_{SS}	Ground
2	1	2	1	V_{OUT}	Output
3	3	1	2	V_{IN}	Power Input Pin

SOT-23-5

PIN NUMBER			SYMBOL	FUNCTION
M	MF	ML		
1	1	5	V_{IN}	Power Input Pin
2	2	2	V_{SS}	Ground
3	——	1	CE	Chip Enable Pin
4	3/4	3	NC	No Connection
5	5	4	V_{OUT}	Output Pin

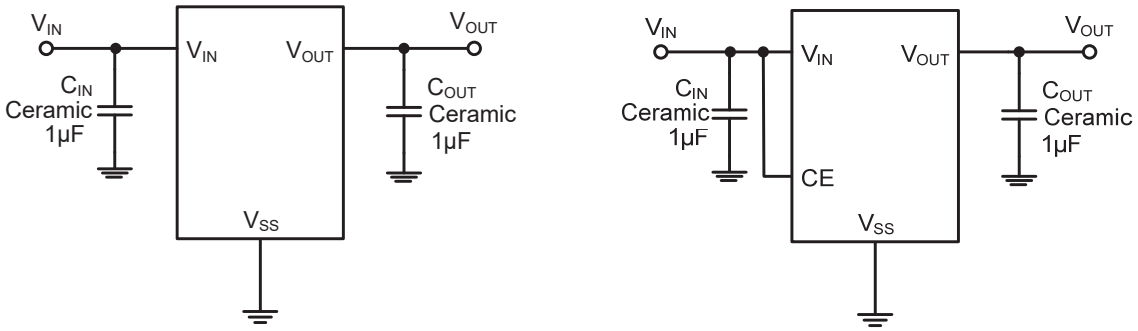
DFN1×1-4

PIN NUMBER	SYMBOL	FUNCTION
F		
1	V_{OUT}	Output Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	V_{IN}	Power Input Pin
EP	Thermal PAD	Ground

SOT-89-3

PIN NUMBER		SYMBOL	FUNCTION
P	PT		
1	2	V_{SS}	Ground
3	1	V_{OUT}	Output
2	3	V_{IN}	Power Input Pin

■ TYPICAL APPLICATION



■ ABSOLUTE MAXIMUM RATINGS(1)

(Unless otherwise specified, T_A=25°C)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage(2)		V_{IN}	-0.3~7	V
Output Voltage(2)		V_{OUT}	-0.3~V_{IN}+0.3	V
Output Current		I_{OUT}	600	mA
Power Dissipation	SOT-23	P_D	0.4	W
	DFN1×1-4		0.4	W
	SOT-89		0.6	W
Operating free air temperature range		T_A	-40~85	°C
Operating Junction Temperature Range(3)		T_j	-40~125	°C
Storage Temperature		T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	°C
ESD rating(4)		Human Body Model -(HBM)	4	kV
		Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings may* cause permanent damage to the device. These are stress ratingsonly, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2)All voltages are with respect to network ground terminal.

(3)This IC includes over temperature protection that is intended toprotect the device during momentary overload. Junction temperature willexceed 125°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

(4)ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pFcapacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	1.8		6	V
Operating junction temperature range, T_j	0		125	°C
Operating free air temperature range, T_A	0		85	°C

■ ELECTRICAL CHARACTERISTICS

LR5213 Series (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, T_A=25℃,unless otherwise specified)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.(5)	MAX.	UNITS
Output Voltage		$V_{OUT}(E)$(6)	I_{OUT}=1mA	V_{OUT}(7) *0.98	V_{OUT}(7)	V_{OUT}(7) *1.02	V
Supply Current		I_{SS}	I_{OUT}=0		50	100	μA
Standby Current		I_{STBY}	CE = V_{SS}		0.1	1	μA
Output Current		I_{OUT}	—	500			mA
Dropout Voltage		V_{DO}(8)	I_{OUT} =100mA V_{OUT}≥3.3V		50		mV
Load Regulation		ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA		1		mV
Line Regulation		$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤6V		0.01	0.2	%/V
Output Voltage Temperature Characteristics		$\frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$	I_{OUT} =10mA -40≤T≤+85		50		ppm
Short Current		I_{Short}	V_{OUT} =V_{SS}		50		mA
Input Voltage		V_{IN}	—	1.8		6.0	V
Power Supply Rejection Rate	100Hz	PSRR	I_{OUT}=50mA		75		dB
	1kHz				80		
	10kHz				80		
CE "High" Voltage		V_{CE}"H"		1.5		V_{IN}	V
CE "Low" Voltage		V_{CE}"L"				0.3	V
C_{OUT} Auto-Discharge Resistance		$R_{DISCHRG}$	V_{IN}=5V, V_{OUT}=3.0V, V_{CE}=V_{SS}		60		Ω

(5) Typical numbers are at 25°C and represent the mostlikely norm.

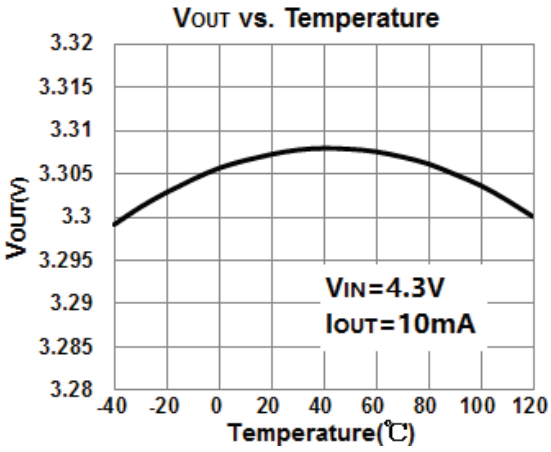
(6)$V_{OUT}(E)$: Effective Output Voltage (Ie. The output voltage when V_{IN}= (V_{OUT} +1.0V) andmaintain acertain I_{OUT} Value).

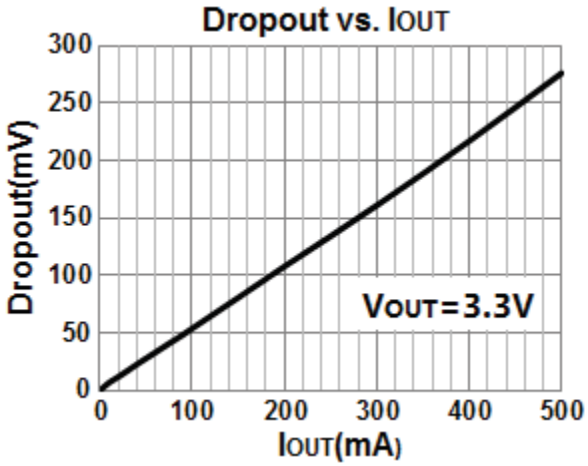
(7)V_{OUT}: Specified Output Voltage.

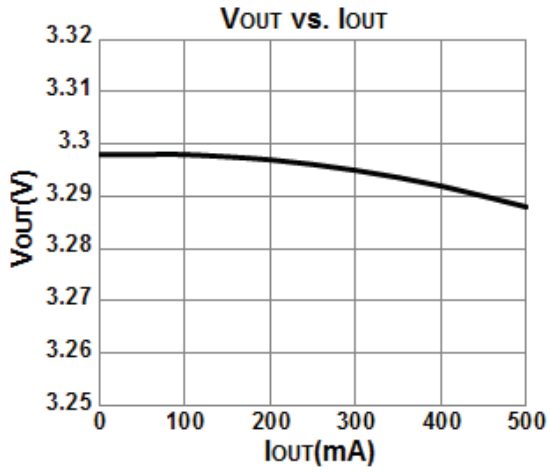
(8)V_{DO} : The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

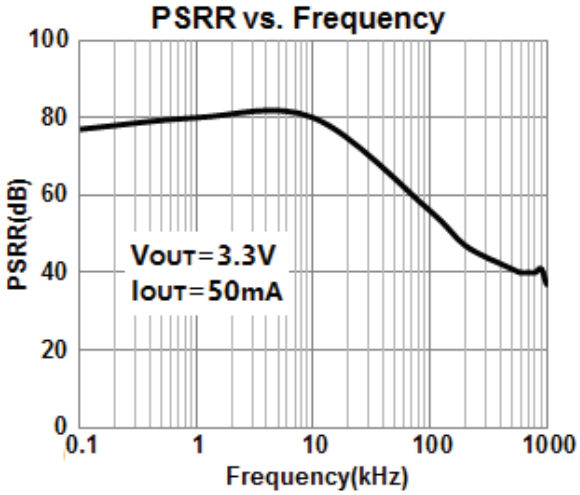
■ TYPICAL PERFORMANCE CHARACTERISTICS

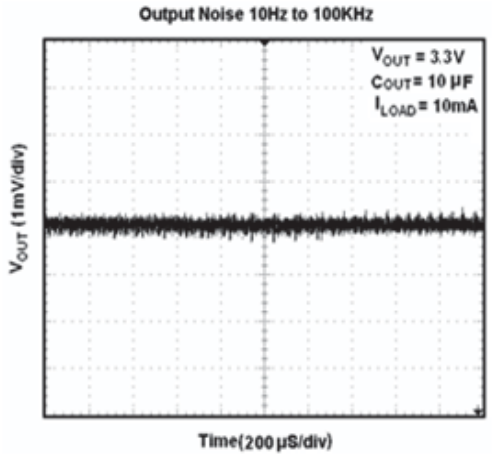
(V_{CE}=V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, T_A=25℃,unless otherwise specified)

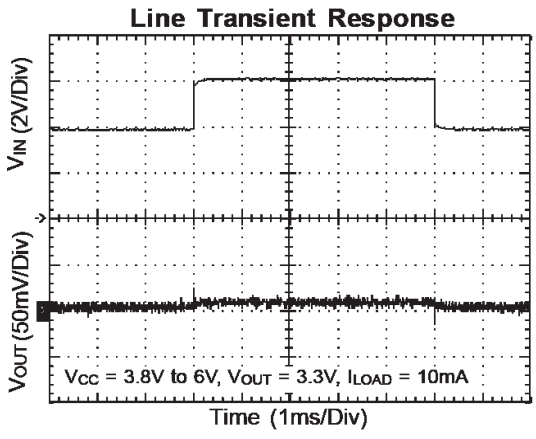




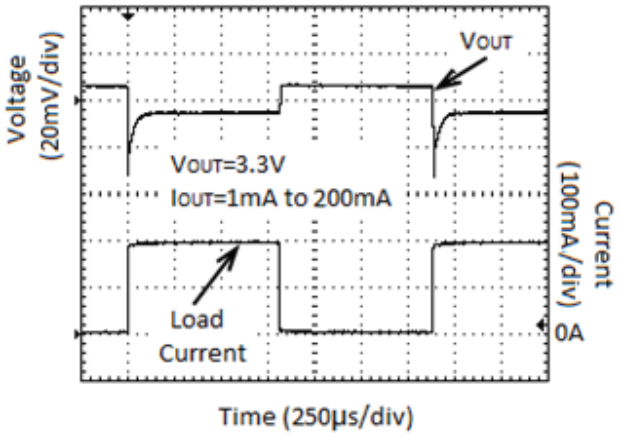


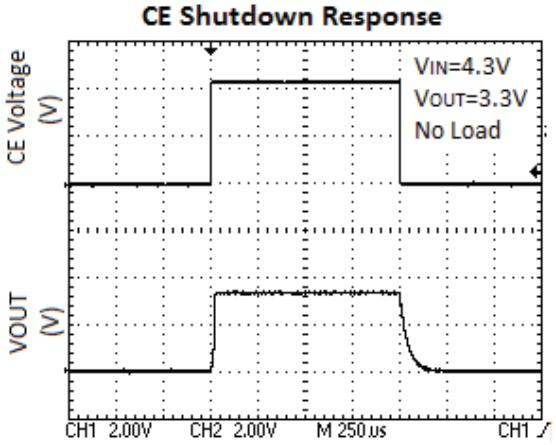






■ TYPICAL PERFORMANCE CHARACTERISTICS





COUT Auto-Discharge Function

LR5213B series can discharge the electric charge in the output capacitor (C_{OUT}), when a low signal to the CE pin, which enables a whole IC circuit turn off, is inputted via the N-channel transistor located between the V_{OUT} pin and the V_{SS} pin (cf. BLOCK DIAGRAM). The C_{OUT} auto-discharge resistance value is set at60Ω(V_{OUT}=3.0V @ V_{IN}=5.0V at typical). The discharge time of the output capacitor (C_{OUT}) is set by the C_{OUT} auto-discharge resistance (R) and the output capacitor (C_{OUT}). By setting time constant of a C_{OUT} auto-discharge resistance value [$R_{DISCHRG}$] and an output capacitor value (C_{OUT}) as τ(τ=C x $R_{DISCHRG}$), the output voltage after discharge via the N-channel transistor is calculated by the following formulas.

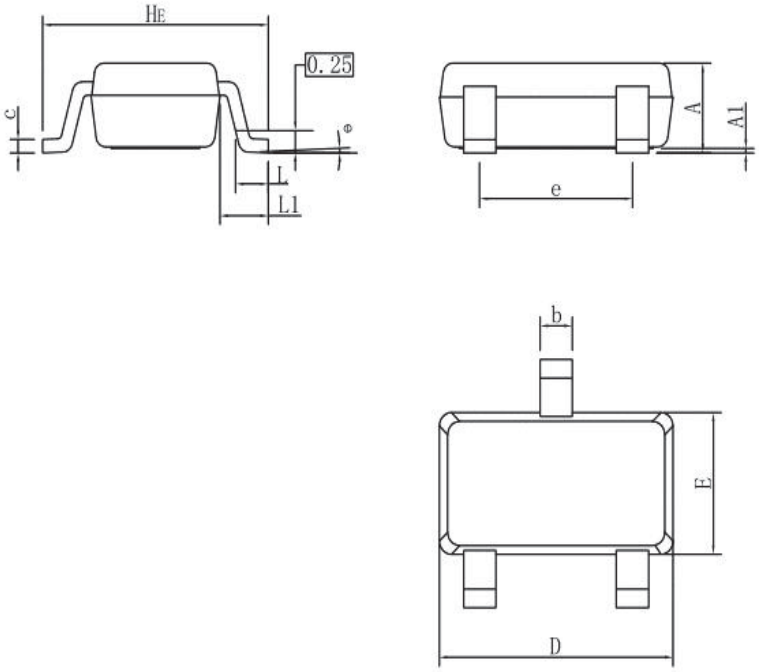
$$V = V_{OUT(E)} \times e^{-t/\tau},\ or\ t=\tau ln\ (\ V / V_{OUT(E)}\ )$$

(V : Output voltage after discharge, $V_{OUT(E)}$: Output voltage, t: Discharge time,

τ: C_{OUT} auto-discharge resistance $R_{DISCHRG}$×Output capacitor (C_{OUT}) value C)

■ PACKAGING INFORMATION

• SOT-23-3 PACKAGE OUTLINE DIMENSIONS



DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°
All Dimensions in mm			

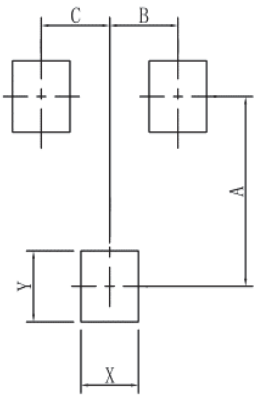
GENERAL NOTES

1.Top package surface finish Ra0.4±0.2um

2.Bottom package surface finish Ra0.7±0.2um

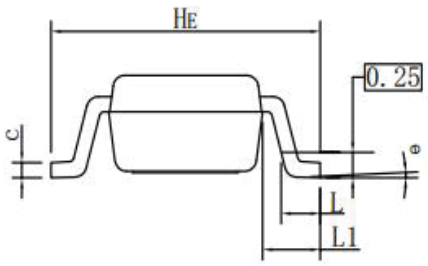
3.Side package surface finish Ra0.4±0.2um

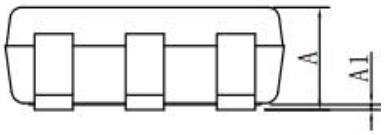
SOLDERING FOOTPRINT

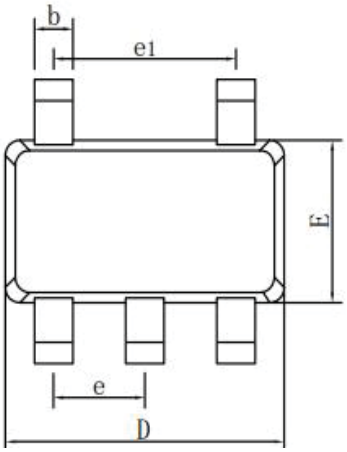


DIM	(mm)
X	0.80
Y	0.90
A	2.40
B	0.95
C	0.95

• SOT-23-5 PACKAGE OUTLINE DIMENSIONS







DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	0.85	0.95	1.05
e1	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°

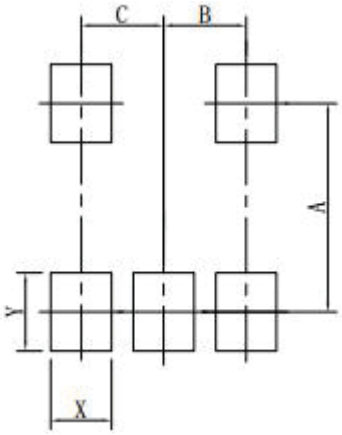
GENERAL NOTES

1.Top package surface finish Ra0.4±0.2um

2.Bottom package surface finish Ra0.7±0.2um

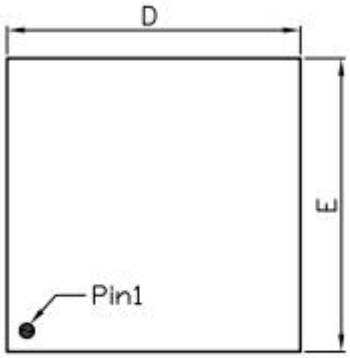
3.Side package surface finish Ra0.4±0.2um

SOLDERING FOOTPRINT

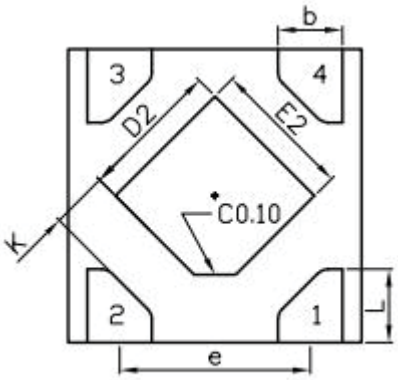


DIM	(mm)
X	0.70
Y	0.90
A	2.40
B	0.95
C	0.95

- **DFN1×1-4 PACKAGE OUTLINE DIMENSIONS**

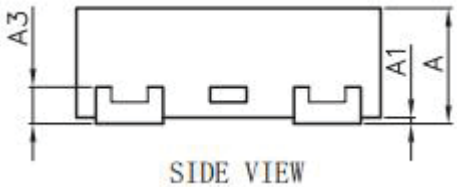


TOP VIEW



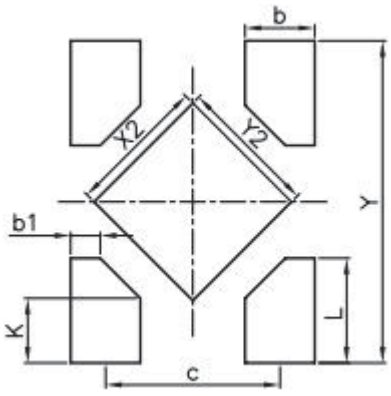
BOTTOM VIEW

DFN1010			
DIM	MIN	NOR	MAX
A	0.34	0.37	0.40
A1	0.01	0.02	0.05
b	0.17	0.22	0.25
L	0.20	0.25	0.30
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
e	0.65		
A3	0.127REF.		
K	0.15	-	-
All Dimensions in mm			



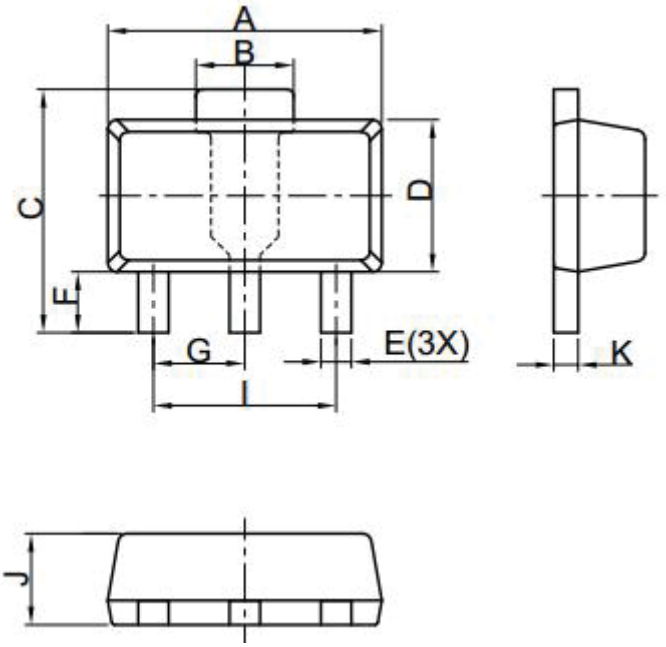
SIDE VIEW

SOLDERING FOOTPRINT



DFN1010	
DIM	(mm)
X2	0.52
Y2	0.52
L	0.39
Y	1.20
K	0.24
b	0.26
c	0.65
b1	0.11

● SOT-89-3 PACKAGE OUTLINE DIMENSIONS

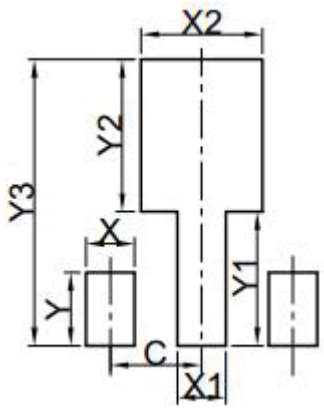


DIM	MIN	NOR	MAX
A	4.40	4.50	4.60
B	1.40	1.60	1.80
C	3.90	4.00	4.25
D	2.40	2.50	2.60
E	0.40	0.50	0.58
F	0.90	1.00	1.20
G	1.50 BSC		
I	3.00 BSC		
J	1.40	1.50	1.60
K	0.34	0.40	0.50
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

SOLDERING FOOTPRINT



DIM	(mm)
X	0.80
Y	1.20
X1	0.80
Y1	2.20
X2	2.00
Y2	2.50
C	1.50
Y3	4.70

■ DEVICE MARKING AND REEL SPECTION

Device(9)	Package	Output Voltage(10)	Marking(11)(12)	Shipping
LR5213AxxM	SOT-23-3	1.05V~5.0V	1AX	3K/Reel
LR5213AxxMA	SOT-23-3	1.05V~5.0V	1MX	3K/Reel
LR5213AxxMC	SOT-23-3	1.05V~5.0V	1CX	3K/Reel
LR5213AxxMY	SOT-23-3	1.05V~5.0V	1YX	3K/Reel
LR5213AxxMF	SOT-23-5	1.05V~5.0V	1FX	3K/Reel
LR5215BxxM	SOT-23-5	1.05V~5.0V	1BX	3K/Reel
LR5213BxxMR	SOT-23-5	1.05V~5.0V	1RX	3K/Reel
LR5213AxxP	SOT-89-3	1.05V~5.0V	1DX	1K/Reel
LR5213AxxPT	SOT-89-3	1.05V~5.0V	1TX	1K/Reel
LR5213BxxF	DFN1X1-4	1.05V~5.0V	HX	10K/Reel

(9) : "xx" represents output voltage, eg"18" express that the output voltage is 1.8V

(10): Output voltage varies from 1.05V to 5.0V, 0.1V an interval

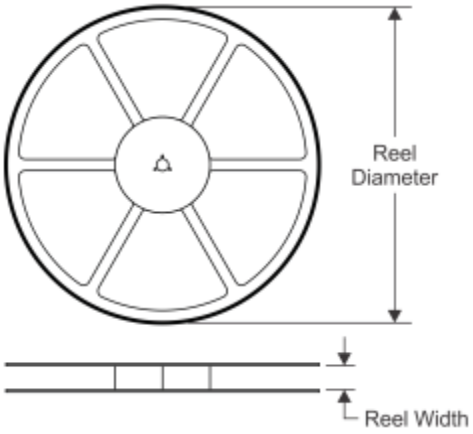
(11): The last letter "X" changes along with the output voltage, as figure below

(12): There are additional marking, which relates to the date code

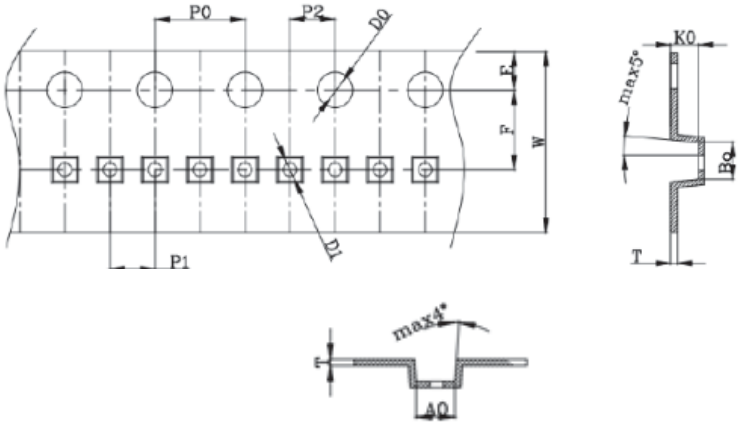
Voltage	....	1.0	1.2	1.5	1.8	2.5	2.7	2.8	3.0	3.3	3.6	4.0	4.2	5.0	....
Symble	....	D	E	F	G	H	I	J	K	L	M	N	T	P	....

■ TAPE AND REEL INFORMATION

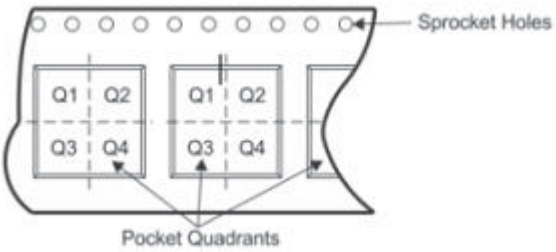
REEL DEMENSIONS



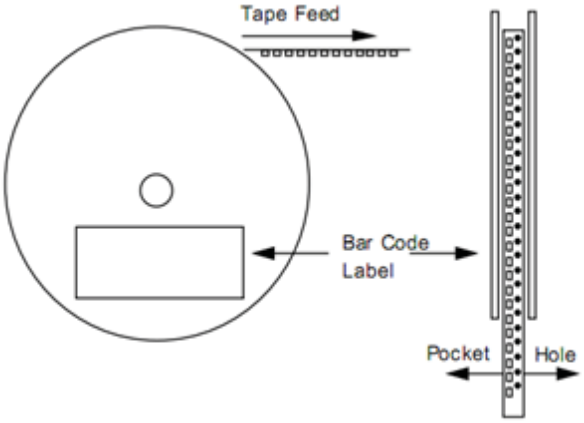
TAPE DEMENSIONS



PIN1 ORIENTATION



ROLLING ORIENTATION



Device	Package	Reel Diameter (mm)	Reel width (mm)	P0 (mm)	P1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	PIN1
LR5213AxxM	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR5213AxxMC	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR5213AxxMY	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR5213AxxMF	SOT-23-5	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.25±0.05	3.15±0.05	1.5±0.05	8.0±0.1	Q3
LR5213BxxM	SOT-23-5	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.25±0.05	3.15±0.05	1.5±0.05	8.0±0.1	Q3
LR5213BxxML	SOT-23-5	178±1	9.6±1.2	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	$12.0^{+0.3}_{-0.1}$	Q3
LR5213AxxP	SOT-89-3	178±1	$13.0^{+1}_{-0.5}$	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	$12.0^{+0.3}_{-0.1}$	NA
LR5213AxxPT	SOT-89-3	178±1	$13.0^{+1}_{-0.5}$	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	$12.0^{+0.3}_{-0.1}$	NA
LR5213BxxF	DFN1X1-4	178±1	9.6±1.2	4.00±0.1	2.00±0.05	1.16±0.05	1.16±0.05	0.5±0.05	8.00±0.1	Q3