MC74HCT366A

Hex 3-State Inverting Buffer with Common Enables and LSTTL Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT366A is identical in pinout to the LS366. The device inputs are compatible with standard CMOS or LSTTL outputs.

This device is a high–speed hex buffer with 3–state outputs and two common active–low Output Enables. When either of the enables is high, the buffer outputs are placed into high–impedance states. The HCT366A has inverting outputs.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These are Pb–Free Devices*

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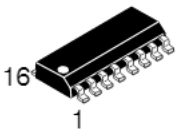
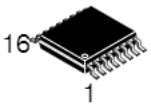


SOIC–16
D SUFFIX
CASE 751B



TSSOP–16
DT SUFFIX
CASE 948F

A	=	Assembly Location
WL, L	=	Wafer Lot
Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb–Free Package

(Note: Microdot may be in either

ORDERING INFORMA

See detailed ordering and shipping informa
dimensions section on page 2 of this data

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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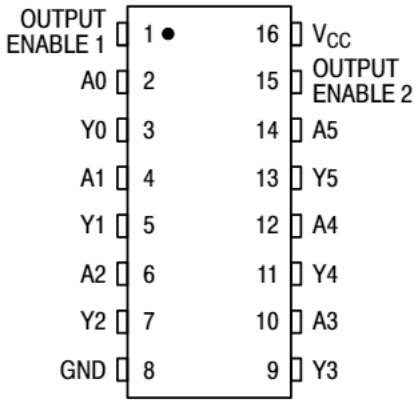

Figure 1. Pin Assignment

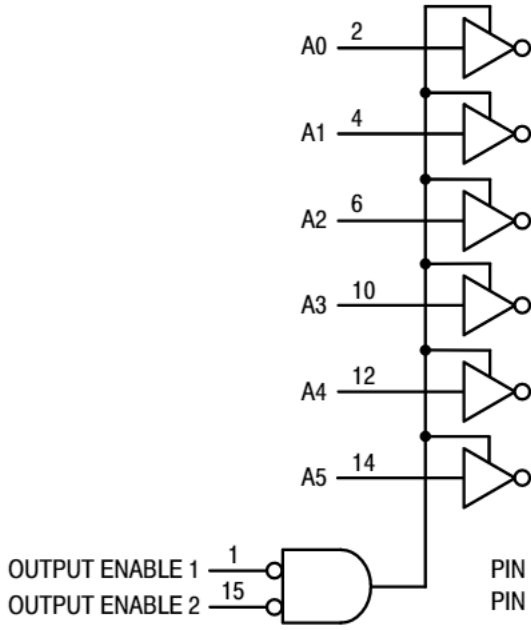

Figure 2. Logic Diagram

FUNCTION TABLE

Inputs			Output
Enable 1	Enable 2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

X = don't care
Z = high impedance

ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT366ADG	SOIC−16 (Pb−Free)	48 Units / Rai
MC74HCT366ADR2G		2500 Units / Re
MC74HCT366ADTR2G	TSSOP−16 (Pb−Free)	2500 Units / Re
NLVHCT366ADTRG*		2500 Units / Re

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qu Capable.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Package†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device co
circuitry to guard
due to high static v
fields. However, p
be taken to avoid a
voltage higher than
voltages to this hig
cuit. For proper op
V_{out} should be co
range GND ≤ (V_{in}
Unused inputs
tied to an appropr
level (e.g., either
Unused outputs m

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 3.0 V	0	600	
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V, $\|I_{out}\|$ ≤ 20 μA	4.5 to 5.5	2.0	2.0	
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V, $\|I_{out}\|$ ≤ 20 μA	4.5 to 5.5	0.80	0.80	
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH}, $\|I_{out}\|$ ≤ 20 μA	2.0	1.9	1.9	
			4.5	4.4	4.4	
			6.0	5.9	5.9	
		V_{in} = V_{IH}, $\|I_{out}\|$ ≤ 3.6 mA	3.0	2.48	2.34	
		$\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	
		$\|I_{out}\|$ ≤ 7.8 mA	6.0	5.48	5.34	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL}, $\|I_{out}\|$ ≤ 20 μA	2.0	0.1	0.1	
			4.5	0.1	0.1	
			6.0	0.1	0.1	
		V_{in} = V_{IL}, $\|I_{out}\|$ ≤ 3.6 mA	3.0	0.26	0.33	
		$\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	
		$\|I_{out}\|$ ≤ 7.8 mA	6.0	0.26	0.33	

		$\|I_{out}\| \leq 7.8$ mA	6.0	0.26	0.33	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	