

# MC74HC259A

## 8-Bit Addressable Latch 1-of-8 Decoder

### High-Performance Silicon-Gate CMOS

The MC74HC259A is identical in pinout to the LS259. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC259A has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the HC259A as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

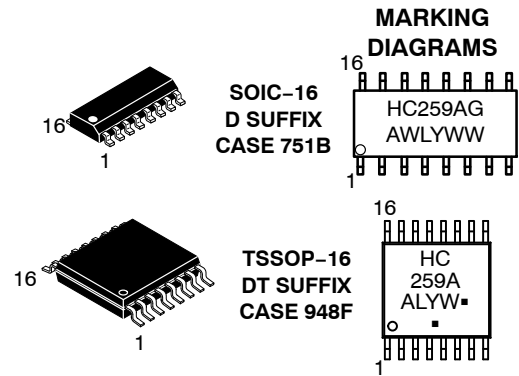
#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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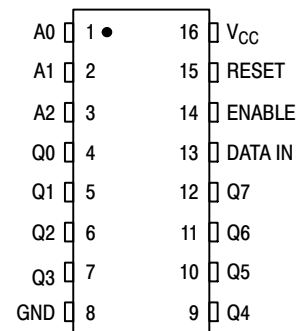
<http://onsemi.com>



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or  $\blacksquare$  = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT



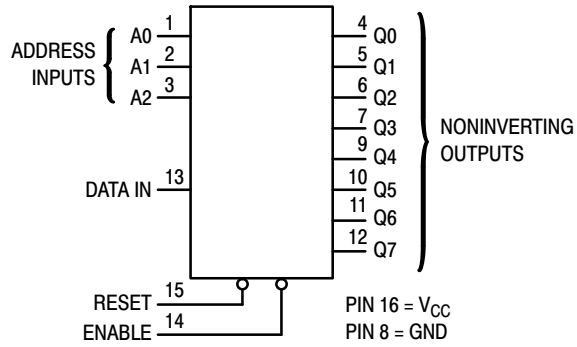
#### MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC74HC259A



**LATCH SELECTION TABLE**

Address Inputs			Latch Addressed
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

**Figure 1. Logic Diagram**

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Package TSSOP Package	500 450	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)			
	V <sub>CC</sub> = 2.0 V	0	1000	ns
	V <sub>CC</sub> = 3.0 V	0	600	
	V <sub>CC</sub> = 4.5 V	0	500	
	V <sub>CC</sub> = 6.0 V	0	400	

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Data to Output (Figures 2 and 7)	2.0	125	160	175	ns
		3.0	45	60	70	
		4.5	32	32	42	
		6.0	25	28	33	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Address Select to Output (Figures 3 and 7)	2.0	150	175	200	ns
		3.0	60	70	80	
		4.5	32	40	45	
		6.0	28	30	35	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Enable to Output (Figures 4 and 7)	2.0	150	175	200	ns
		3.0	60	70	80	
		4.5	32	40	45	
		6.0	28	30	35	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Output (Figures 5 and 7)	2.0	110	125	160	ns
		3.0	36	45	60	
		4.5	22	26	32	
		6.0	19	23	28	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 7)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	-	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
		30			

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Address or Data to Enable (Figure 6)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>h</sub>	Minimum Hold Time, Enable to Address or Data (Figure 6)	2.0	1	1	1	ns
		3.0	1	1	1	
		4.5	1	1	1	
		6.0	1	1	1	
t <sub>w</sub>	Minimum Pulse Width, Reset or Enable (Figure 4 or 5)	2.0	70	90	100	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

# MC74HC259A

## SWITCHING WAVEFORMS

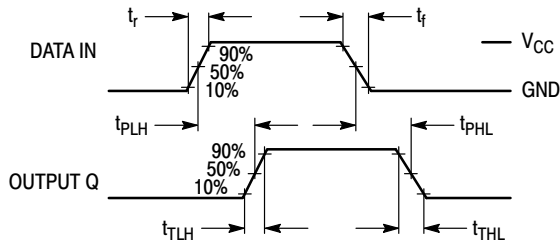


Figure 2.

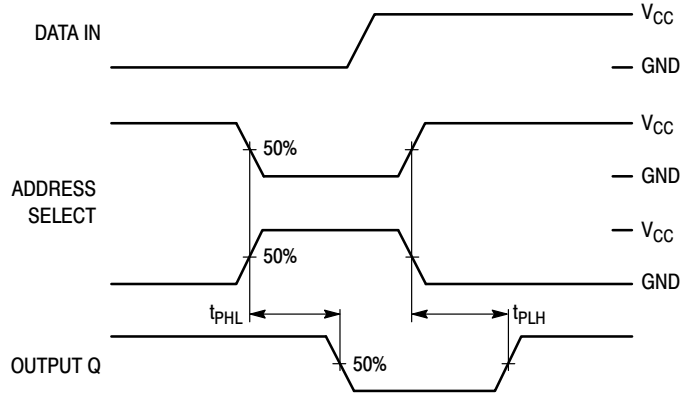


Figure 3.

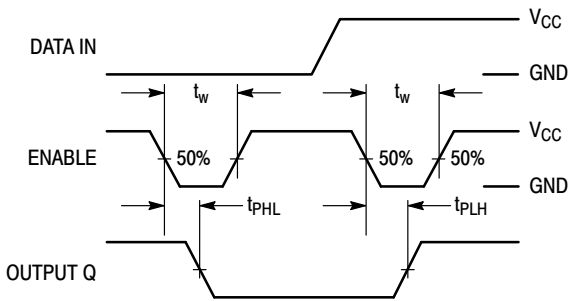


Figure 4.

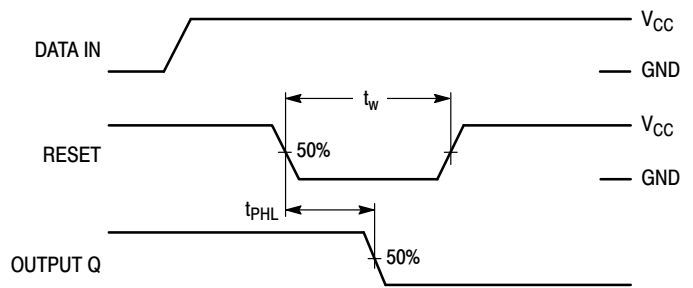


Figure 5.

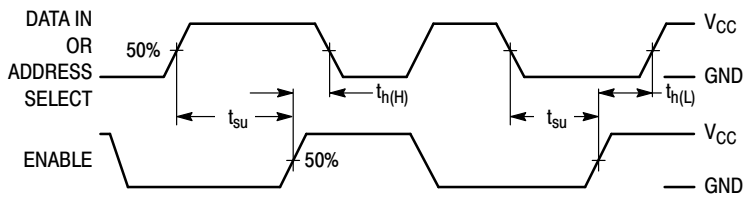
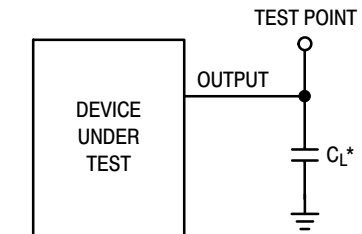


Figure 6.



\*Includes all probe and jig capacitance

Figure 7. Test Circuit

# MC74HC259A

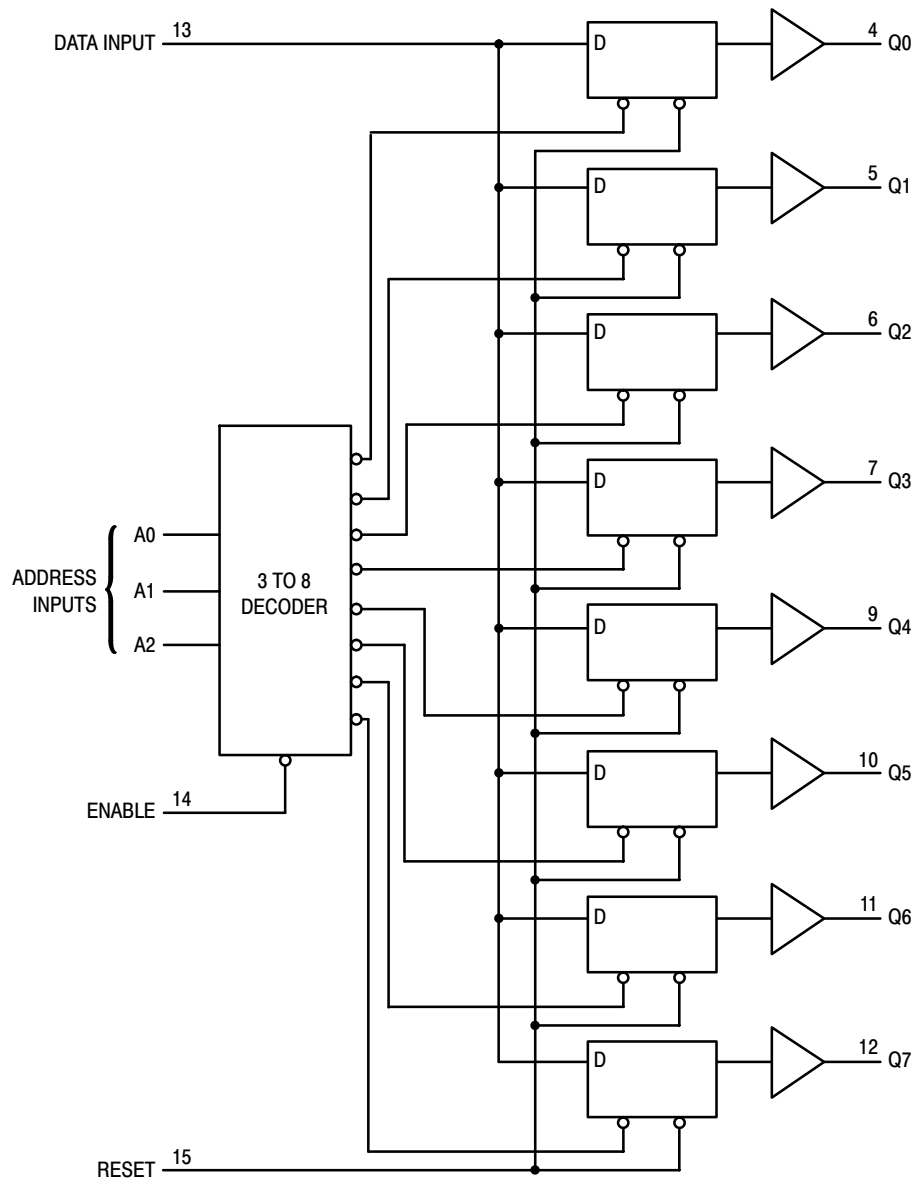


Figure 8. Expanded Logic Diagram

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74HC259ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC259ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC74HC259ADTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
MC74HC259ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
NLVHC259ADR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



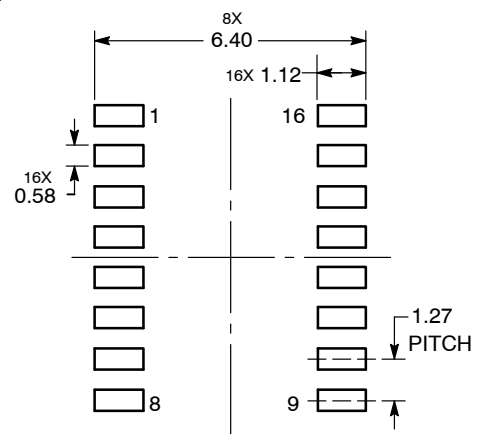
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |   |   |   |   |
|---|---|---|---|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR<br/>2. BASE<br/>3. EMITTER<br/>4. NO CONNECTION<br/>5. EMITTER<br/>6. BASE<br/>7. COLLECTOR<br/>8. COLLECTOR<br/>9. BASE<br/>10. EMITTER<br/>11. NO CONNECTION<br/>12. EMITTER<br/>13. BASE<br/>14. COLLECTOR<br/>15. EMITTER<br/>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE<br/>2. ANODE<br/>3. NO CONNECTION<br/>4. CATHODE<br/>5. CATHODE<br/>6. NO CONNECTION<br/>7. ANODE<br/>8. CATHODE<br/>9. CATHODE<br/>10. ANODE<br/>11. NO CONNECTION<br/>12. CATHODE<br/>13. CATHODE<br/>14. NO CONNECTION<br/>15. ANODE<br/>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1<br/>2. BASE, #1<br/>3. EMITTER, #1<br/>4. COLLECTOR, #1<br/>5. COLLECTOR, #2<br/>6. BASE, #2<br/>7. EMITTER, #2<br/>8. COLLECTOR, #2<br/>9. COLLECTOR, #3<br/>10. BASE, #3<br/>11. EMITTER, #3<br/>12. COLLECTOR, #3<br/>13. COLLECTOR, #4<br/>14. BASE, #4<br/>15. EMITTER, #4<br/>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1<br/>2. COLLECTOR, #1<br/>3. COLLECTOR, #2<br/>4. COLLECTOR, #2<br/>5. COLLECTOR, #3<br/>6. COLLECTOR, #3<br/>7. COLLECTOR, #4<br/>8. COLLECTOR, #4<br/>9. BASE, #4<br/>10. EMITTER, #4<br/>11. BASE, #3<br/>12. EMITTER, #3<br/>13. BASE, #2<br/>14. EMITTER, #2<br/>15. BASE, #1<br/>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1<br/>2. DRAIN, #1<br/>3. DRAIN, #2<br/>4. DRAIN, #2<br/>5. DRAIN, #3<br/>6. DRAIN, #3<br/>7. DRAIN, #4<br/>8. DRAIN, #4<br/>9. GATE, #4<br/>10. SOURCE, #4<br/>11. GATE, #3<br/>12. SOURCE, #3<br/>13. GATE, #2<br/>14. SOURCE, #2<br/>15. GATE, #1<br/>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE<br/>2. CATHODE<br/>3. CATHODE<br/>4. CATHODE<br/>5. CATHODE<br/>6. CATHODE<br/>7. CATHODE<br/>8. CATHODE<br/>9. ANODE<br/>10. ANODE<br/>11. ANODE<br/>12. ANODE<br/>13. ANODE<br/>14. ANODE<br/>15. ANODE<br/>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH<br/>2. COMMON DRAIN (OUTPUT)<br/>3. COMMON DRAIN (OUTPUT)<br/>4. GATE P-CH<br/>5. COMMON DRAIN (OUTPUT)<br/>6. COMMON DRAIN (OUTPUT)<br/>7. COMMON DRAIN (OUTPUT)<br/>8. SOURCE P-CH<br/>9. SOURCE P-CH<br/>10. COMMON DRAIN (OUTPUT)<br/>11. COMMON DRAIN (OUTPUT)<br/>12. COMMON DRAIN (OUTPUT)<br/>13. GATE N-CH<br/>14. COMMON DRAIN (OUTPUT)<br/>15. COMMON DRAIN (OUTPUT)<br/>16. SOURCE N-CH</p> |   |

### SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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