

# MC74HCT14A

## Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

### High-Performance Silicon-Gate CMOS

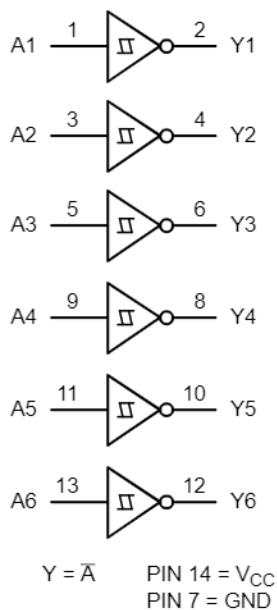
The MC74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

The HCT14A is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

#### LOGIC DIAGRAM



ON Semiconductor®

<http://onsemi.com>

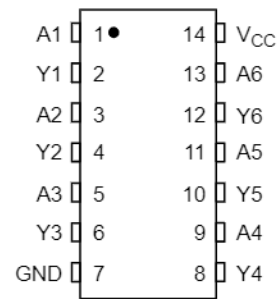


SOIC-14 NB  
 D SUFFIX  
 CASE 751A

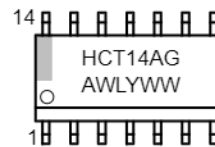


TSSOP-14  
 DT SUFFIX  
 CASE 948G

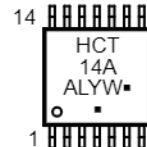
#### PIN ASSIGNMENT



#### MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

Input A	Output Y
L	H
H	L

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC74HCT14A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_I$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 25$	mA
$I_O$	DC Output Sink Current	$\pm 25$	mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 50$	mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 50$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}\text{C}$
$T_J$	Junction Temperature under Bias	+150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance	SOIC TSSOP 125 170	$^{\circ}\text{C}/\text{W}$
$P_D$	Power Dissipation in Still Air at 85 $^{\circ}\text{C}$	SOIC TSSOP 500 450	mW
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating	Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3) > 4000 > 300 > 1000	V
$I_{Latchup}$	Latchup Performance	Above $V_{CC}$ and Below GND at 85 $^{\circ}\text{C}$ (Note 4)	$\pm 300$ mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_I, V_O$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	$^{\circ}\text{C}$
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	-	(Note 5)	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. No Limit when  $V_I \approx 50\% V_{CC}$ ,  $I_{CC} > 1 \text{ mA}$ .
6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

# MC74HCT14A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Temperature Limit						Unit
				-55°C to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
V <sub>H</sub> max	Maximum Hysteresis Voltage	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
V <sub>H</sub> min	Minimum Hysteresis Voltage	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0.4		
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>I</sub> < V <sub>T-</sub> min  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		V <sub>I</sub> < V <sub>T-</sub> min  I <sub>out</sub>   ≤ 4.0 mA	4.5	3.98		3.84		3.7		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>I</sub> ≥ V <sub>T+</sub> max  I <sub>out</sub>   ≤ 20 μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		V <sub>I</sub> ≥ V <sub>T+</sub> max  I <sub>out</sub>   ≤ 4.0 mA	4.5		0.26		0.33		0.4	
I <sub>IK</sub>	Maximum Input Leakage Current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5		1.0		10		40	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>I</sub> = 2.4 V, Any One Input V <sub>I</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C		25°C to 125°C				mA
				2.9		2.4				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

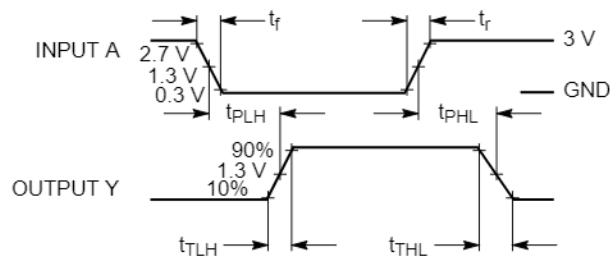
## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF; Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	Test Conditions	Figures	Guaranteed Limit						Unit
				-55°C to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (L to H)	V <sub>CC</sub> = 5.0 V ±10% C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns	1 & 2		32		40		48	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output	V <sub>CC</sub> = 5.0 V ±10% C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns	1 & 2		15		19		22	ns

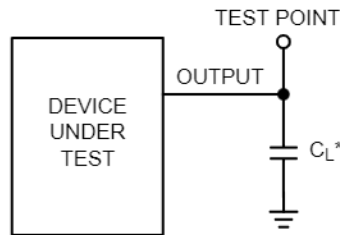
C <sub>PD</sub>	Power Dissipation Capacitance, per Inverter (Note 7)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		32		

7. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HCT14A



**Figure 1. Switching Waveforms**



\*Includes all probe and jig capacitance.

**Figure 2. Test Circuit**

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74HCT14ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
NLV74HCT14ADG*		
MC74HCT14ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HCT14ADR2G*		
MC74HCT14ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HCT14ADTR2G*		

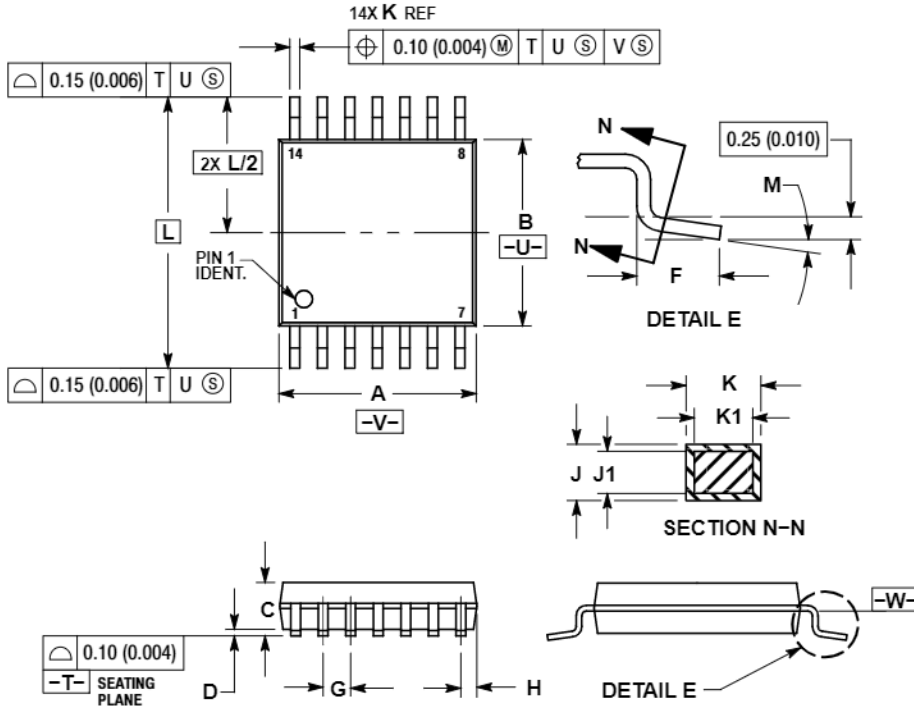
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC74HCT14A

## PACKAGE DIMENSIONS

TSSOP-14  
CASE 948G  
ISSUE B

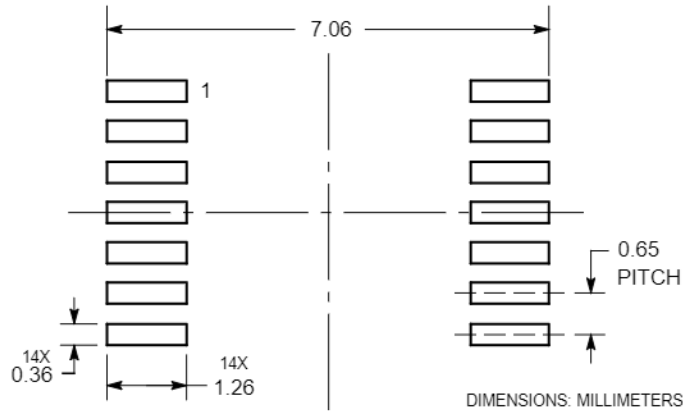


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC	---	0.026 BSC	---
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC	---	0.252 BSC	---
M	0°	8°	0°	8°

### SOLDERING FOOTPRINT\*

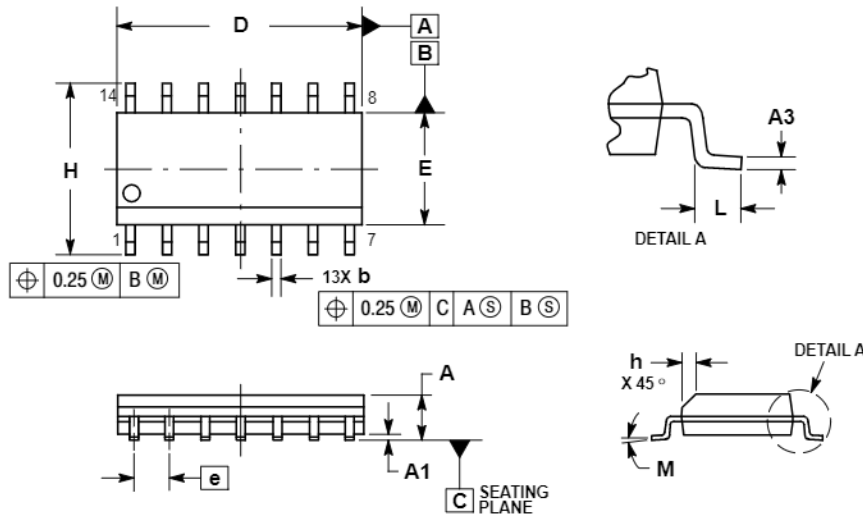


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HCT14A

## PACKAGE DIMENSIONS

SOIC-14 NB  
CASE 751A-03  
ISSUE K

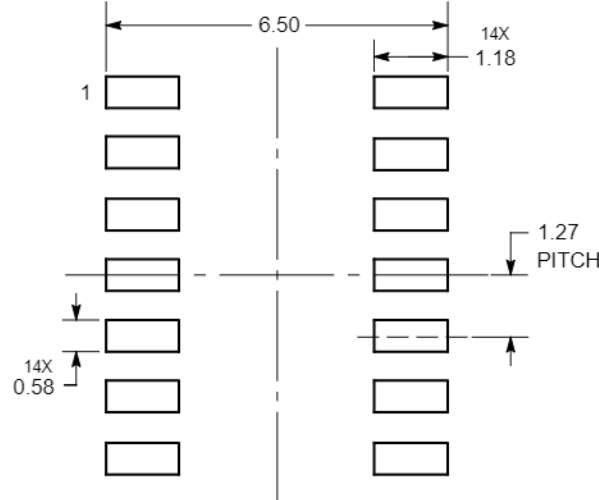


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5817-1050

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)  
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative