

MC74HC574A

Octal 3-State Noninverting D Flip-Flop

High-Performance Silicon-Gate CMOS

The MC74HC574A is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Data meeting the set-up time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574A is identical in function to the HC374A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

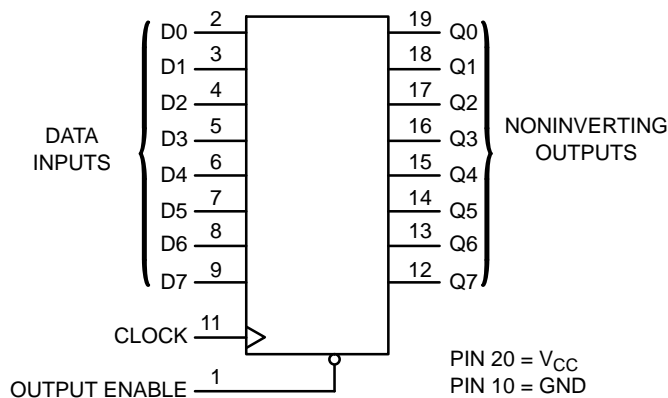
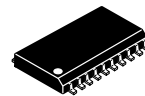


Figure 1. Logic Diagram



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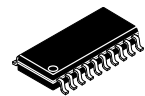
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SOIC-20
DW SUFFIX
CASE 751D

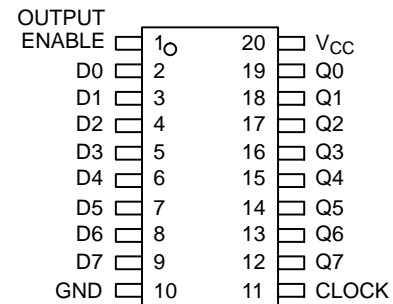


TSSOP-20
DT SUFFIX
CASE 948E

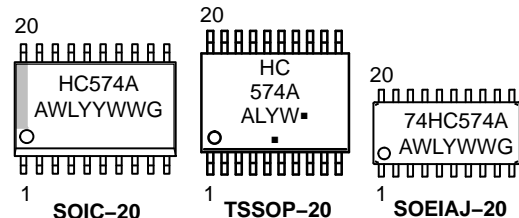


SOEIAJ-20
F SUFFIX
CASE 967

PIN ASSIGNMENT



MARKING DIAGRAMS



- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or \blacksquare = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | Output | |
|--------|-----------------|--------|-----------|
| OE | Clock | D | Q |
| L | \nearrow | H | H |
| L | \nearrow | L | L |
| L | L,H, \searrow | X | No Change |
| H | X | X | Z |

X = Don't Care
Z = High Impedance

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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| Design Criteria | Value | Units |
|---------------------------------|--------|---------|
| Internal Gate Count* | 66.5 | ea. |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | μ W |
| Speed Power Product | 0.0075 | μ J |

*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|---------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----------------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V_I | DC Input Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| V_O | DC Output Voltage (Note 1) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | ± 20 | mA |
| I_{OK} | DC Output Diode Current | ± 35 | mA |
| I_O | DC Output Sink Current | ± 35 | mA |
| I_{CC} | DC Supply Current per Supply Pin | ± 75 | mA |
| I_{GND} | DC Ground Current per Ground Pin | ± 75 | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | $^{\circ}$ C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | $^{\circ}$ C |
| T_J | Junction Temperature under Bias | +150 | $^{\circ}$ C |
| θ_{JA} | Thermal Resistance | SOIC TSSOP 96 128 | $^{\circ}$ C/W |
| P_D | Power Dissipation in Still Air at 85 $^{\circ}$ C | SOIC TSSOP 500 450 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F_R | Flammability Rating | Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in | |
| V_{ESD} | ESD Withstand Voltage | Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) > 4000 > 300 > 1000 | V |
| $I_{Latchup}$ | Latchup Performance | Above V_{CC} and Below GND at 85 $^{\circ}$ C (Note 5) | ± 300 mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------|------------------------------------------------------|----------------------------------------------------------|-------------------------|--------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_I, V_O | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | -55 | +125 | $^{\circ}$ C |
| t_r, t_f | Input Rise and Fall Time (Figure 2) | $V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V | 0 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
| | | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 2.48 | 2.34 | 2.2 | V |
| | | | 4.5 | 3.98 | 3.84 | 3.7 | |
| | | | 6.0 | 5.48 | 5.34 | 5.2 | |
| | | | | | | | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IL} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 0.26 | 0.33 | 0.4 | |
| | | | 4.5 | 0.26 | 0.33 | 0.4 | |
| | | | 6.0 | 0.26 | 0.33 | 0.4 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 6.0 | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4.0 | 40 | 160 | μA |

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|----------------------------------------|------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
| | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| f _{max} | Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 5) | 2.0 | 6.0 | 4.8 | 4.0 | MHz |
| | | 3.0 | 15 | 10 | 8.0 | |
| | | 4.5 | 30 | 24 | 20 | |
| | | 6.0 | 35 | 28 | 24 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Clock to Q (Figures 2 and 5) | 2.0 | 160 | 200 | 240 | ns |
| | | 3.0 | 105 | 145 | 190 | |
| | | 4.5 | 32 | 40 | 48 | |
| | | 6.0 | 27 | 34 | 41 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 2.0 | 150 | 190 | 225 | ns |
| | | 3.0 | 100 | 125 | 150 | |
| | | 4.5 | 30 | 38 | 45 | |
| | | 6.0 | 26 | 33 | 38 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 2.0 | 140 | 175 | 210 | ns |
| | | 3.0 | 90 | 120 | 140 | |
| | | 4.5 | 28 | 35 | 42 | |
| | | 6.0 | 24 | 30 | 36 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, any Output (Figures 2 and 5) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance, Output in High-Impedance State | | 15 | 15 | 15 | pF |

| C _{PD} | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF |
|-----------------|-----------------------------------------------------|-----------------------------------------|--|--|----|
| | | 24 | | | |
| | | | | | |

*Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

TIMING REQUIREMENTS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | Figure | V _{CC} Volts | Guaranteed Limit | | | | | | Unit |
|---------------------------------|-----------------------------------|--------|--------------------------|------------------|------|--------|------|---------|------|------|
| | | | | -55 to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| t _{su} | Minimum Setup Time, Data to Clock | 4 | 2.0 | 50 | | 65 | | 75 | | ns |
| | | | 3.0 | 40 | | 50 | | 60 | | |
| | | | 4.5 | 10 | | 13 | | 15 | | |
| | | | 6.0 | 9.0 | | 11 | | 13 | | |
| t _h | Minimum Hold Time, Clock to Data | 4 | 2.0 | 5.0 | | 5.0 | | 5.0 | | ns |
| | | | 3.0 | 5.0 | | 5.0 | | 5.0 | | |
| | | | 4.5 | 5.0 | | 5.0 | | 5.0 | | |
| | | | 6.0 | 5.0 | | 5.0 | | 5.0 | | |
| t _w | Minimum Pulse Width, Clock | 2 | 2.0 | 75 | | 95 | | 110 | | ns |
| | | | 3.0 | 60 | | 80 | | 90 | | |
| | | | 4.5 | 15 | | 19 | | 22 | | |
| | | | 6.0 | 13 | | 16 | | 19 | | |
| t _r , t _f | Maximum Input Rise and Fall Times | 2 | 2.0 | | 1000 | | 1000 | | 1000 | ns |
| | | | 3.0 | | 800 | | 800 | | 800 | |
| | | | 4.5 | | 500 | | 500 | | 500 | |
| | | | 6.0 | | 400 | | 400 | | 400 | |

MC74HC574A

SWITCHING WAVEFORMS

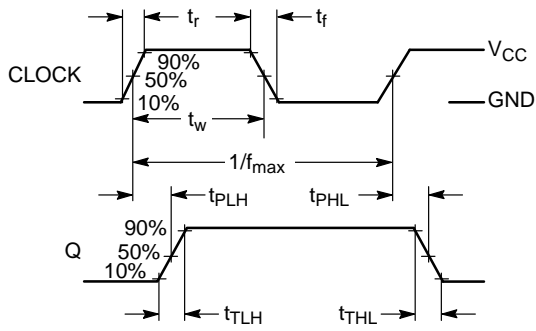


Figure 2.

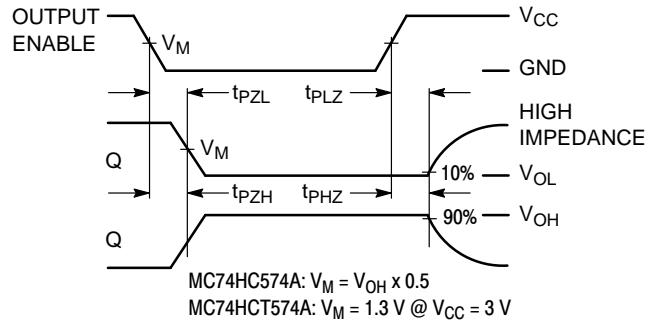


Figure 3.

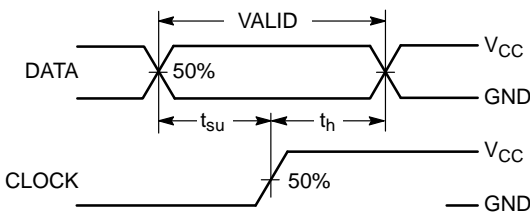
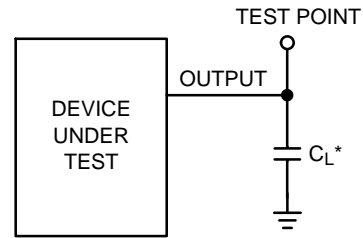
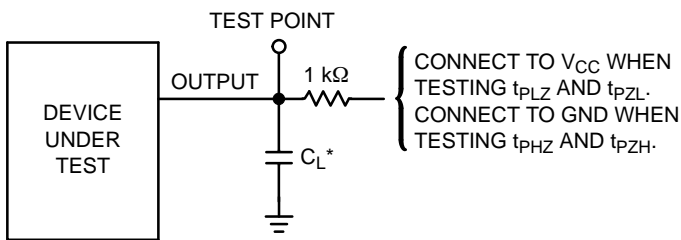


Figure 4.



*Includes all probe and jig capacitance.

Figure 5.



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

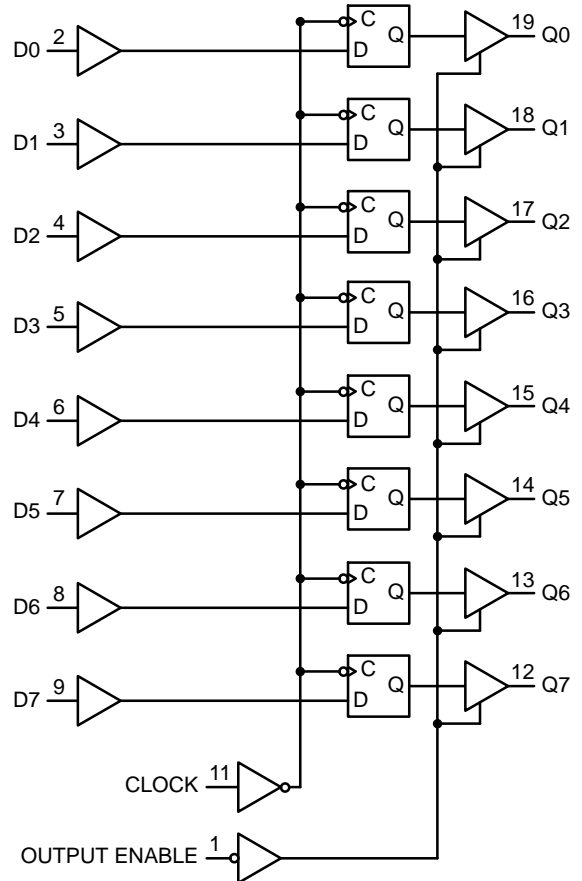


Figure 7. Expanded Logic Diagram

MC74HC574A

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------------|---------------------------|------------------|
| MC74HC574ADWG | SOIC-20 WIDE (Pb-Free) | 38 Units / Rail |
| MC74HC574ADWR2G | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel |
| MC74HC574ADTR2G | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |
| NLV74HC574ADTR2G* | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |
| MC74HC574AFELG | SOEIAJ-20 (Pb-Free) | 2000 Tape & Reel |

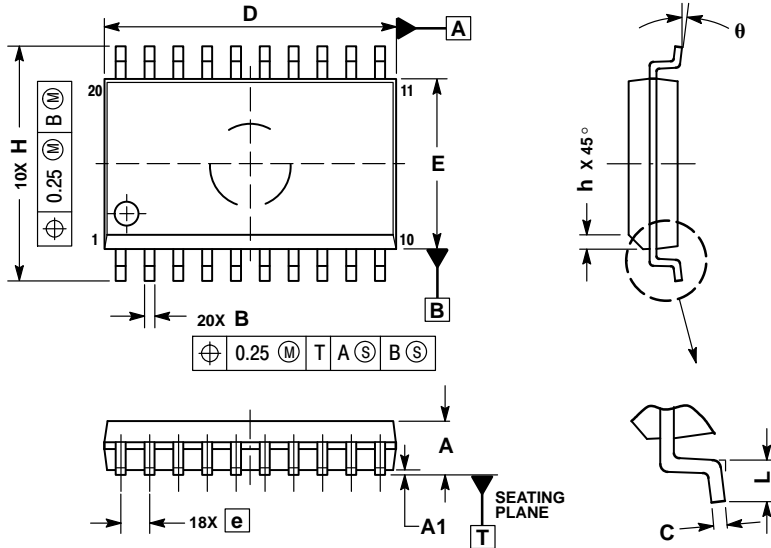
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC74HC574A

PACKAGE DIMENSIONS

SOIC-20
DW SUFFIX
CASE 751D-05
ISSUE G



NOTES:

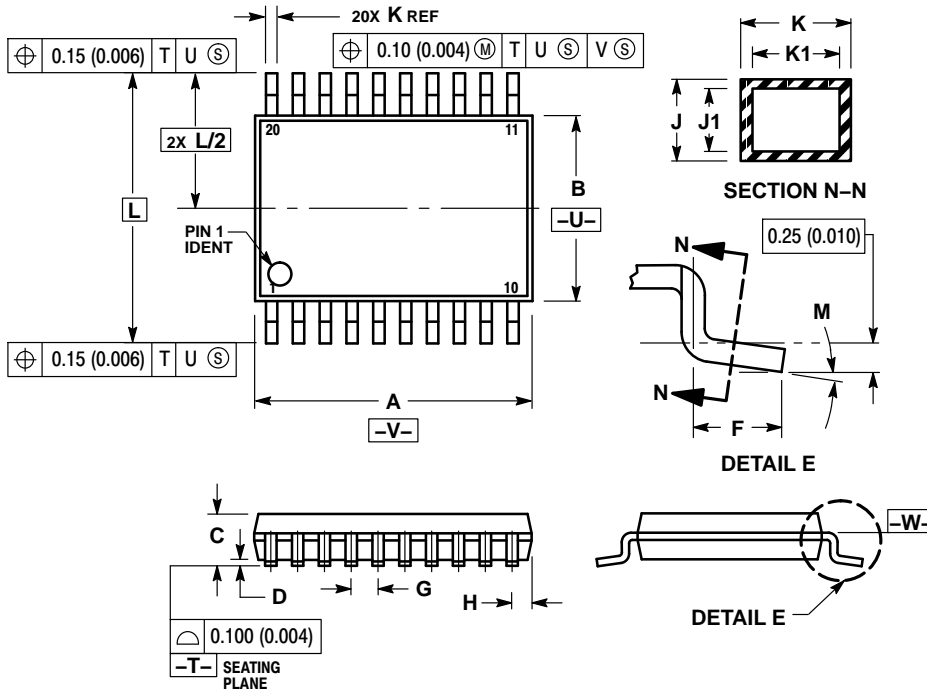
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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

MC74HC574A

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE C

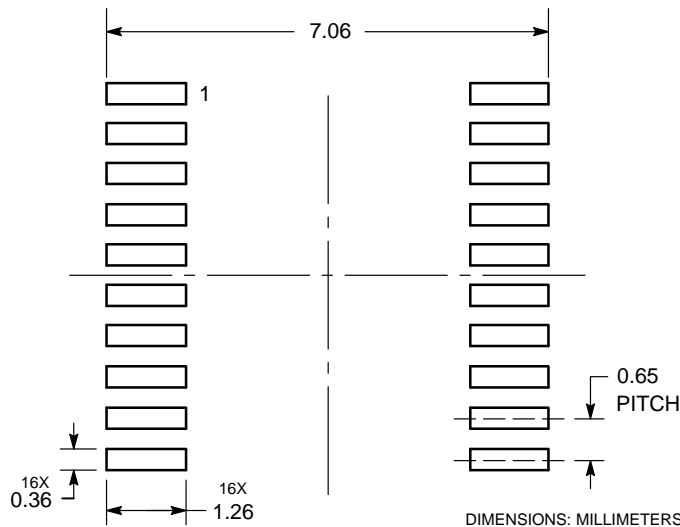


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

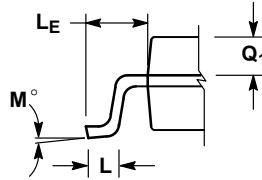
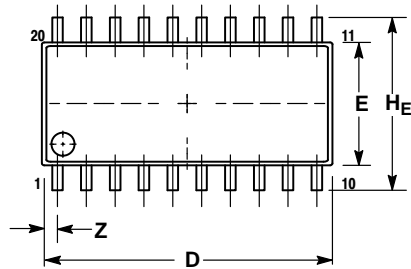


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

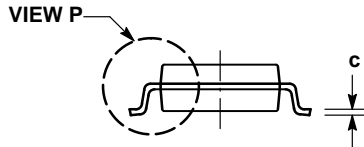
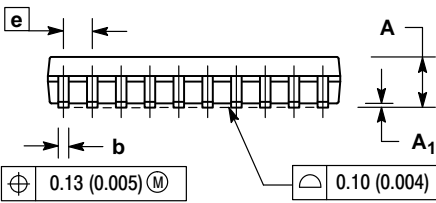
MC74HC574A

PACKAGE DIMENSIONS

SOEIAJ-20
F SUFFIX
CASE 967
ISSUE A




DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.15 | 0.25 | 0.006 | 0.010 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _F | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |

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