

# NB3M8304C

## 3.3 V 200 MHz 1:4 LVCMOS/LVTTL Low Skew Fanout Buffer

### Description

The NB3M8304C is 1:4 fanout buffer with LVCMOS/LVTTL input and output. The device supports the core supply voltage of 3.3 V ( $V_{DD}$  pin) and output supply voltage of 2.5 V or 3.3 V ( $V_{DDO}$  pin). The  $V_{DDO}$  pin powers the four single ended LVCMOS/LVTTL outputs.

The NB3M8304C is Form, Fit and Function (pin to pin) compatible to ICS8304 and ICS8304I. The NB3M8304C is qualified for industrial operating temperature range.

### Features

- Input Clock Frequency up to 200 MHz
- Low Output to Output Skew: 45 ps max
- Low Part to Part Skew: 500 ps max
- Low Additive RMS Phase Jitter
- Input Clock Accepts LVCMOS/ LVTTL Levels
- Operating Voltage:
  - ◆ Core Supply:  $V_{DD} = 3.3 \text{ V} \pm 5\%$
  - ◆ Output Supply:  $V_{DDO} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$
- Operating Temperature Range:
  - ◆ Industrial:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- These Devices are Pb-Free and are RoHS Compliant

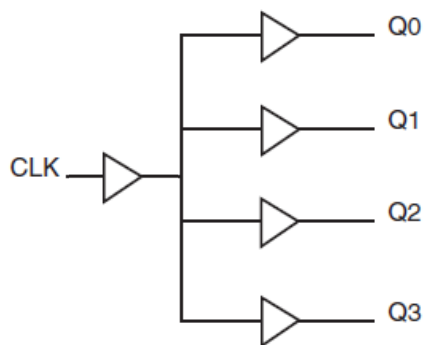


Figure 1. Block Diagram



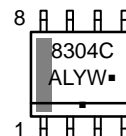
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### MARKING DIAGRAMS\*



SOIC-8  
D SUFFIX  
CASE 751



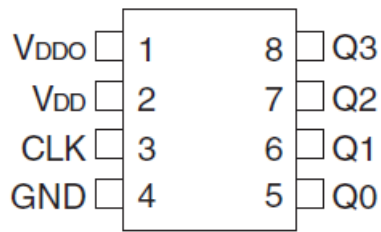
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

## NB3M8304C



**Figure 2. Pin Configuration** (Top View)

**Table 1. PIN DESCRIPTION**

Pin Number	Name	Type	Description
1	VDDO	Output Power	Clock output Supply pin.
2	VDD	Input and Core Power	Input and Core Supply pin.
3	CLK	LVC MOS/LVTTL Input	Clock Input. Internally pull-down.
4	GND	Ground	Supply Ground.
5, 6, 7, 8	Q[0:3]	LVC MOS/LVTTL Output	LVC MOS/LVTTL Clock output.

**Table 2. MAXIMUM RATINGS**

Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD}, V_{DDO}$	Power Supply		–	4.6	V
$V_I$	Input Voltage		–0.5	$V_{DD} + 0.5$	V
$T_{stg}$	Storage Temperature		–65	+150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) SOIC-8	0 lfpm 500 lfpm		80 55	°C/W
$\theta_{JC}$	Thermal Resistance (Junction to Case) (Note 1)			12–17	°C/W
$T_{sol}$	Wave Solder	3 sec		265	°C
MSL	Moisture Sensitivity SOIC-8	Indefinite Time Out of Drypack (Note 2)	Level 1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)
2. For additional information, see Application Note AND8003/D.

# NB3M8304C

**Table 3. DC OPERATING CHARACTERISTICS** ( $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{IN}$	Input Pull-down Resistor (CLK Pin)			51		$k\Omega$
$C_{IN}$	Input Capacitance			4		pF
$R_{OUT}$	Output Impedance (Note 3)		5	7	12	$\Omega$
$C_{PD}$	Power Dissipation Capacitance (per output)	$V_{DD} = V_{DDO} = 3.465\text{ V}$		15		pF
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$I_{IH}$	Input High Current	$V_{IN} = V_{DD} = 3.465\text{ V}$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = 3.465\text{ V}, V_{IN} = 0.0\text{ V}$	-0.5			$\mu\text{A}$

3. Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Figure 4 for supply considerations.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 4. DC OPERATING CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Symbol	Parameter	Condition	Min	Max	Unit
--------	-----------	-----------	-----	-----	------

$V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $V_{DDO} = 2.5\text{ V} \pm 5\%$

$V_{DDO}$	Output Supply Voltage		2.375	2.625	V
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -100\ \mu\text{A}$	2.2		V
		$I_{OH} = -16\ \text{mA}$	2.1		
		$50\ \Omega$ to $V_{DDO}/2$	2.1		
$V_{OL}$	Output LOW Voltage	$I_{OL} = 16\ \text{mA}$		0.25	
		$I_{OL} = 100\ \mu\text{A}$		0.2	V
		$50\ \Omega$ to $V_{DDO}/2$		0.5	

$V_{DD} = V_{DDO} = 3.3\text{ V} \pm 5\%$

$V_{DDO}$	Output Supply Voltage		3.135	3.465	V
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -16\ \text{mA}$	2.9		V
		$I_{OH} = -100\ \mu\text{A}$	3		
		$50\ \Omega$ to $V_{DDO}/2$	2.6		
$V_{OL}$	Output LOW Voltage	$I_{OL} = 16\ \text{mA}$		0.25	
		$I_{OL} = 100\ \mu\text{A}$		0.15	V
		$50\ \Omega$ to $V_{DDO}/2$		0.5	

**Table 5. DC OPERATING CHARACTERISTICS**

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{DD} = V_{DDO} = 3.3\text{ V} \pm 5\%$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $V_{DDO} = 2.5\text{ V} \pm 5\%$ )

Symbol	Parameter	Condition	Min	Max	Unit
$I_{DD}$	Quiescent Power Supply Current	No Load		15	mA
$I_{DDO}$	Quiescent Power Supply Current	No Load		8	mA
$V_{IH}$	Input HIGH Voltage		2	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage		-0.3	1.3	V

# NB3M8304C

**Table 6. AC CHARACTERISTICS** (Note 4)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b><math>T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}; V_{DD} = 3.3\text{ V } \pm 5\%, V_{DDO} = 3.3\text{ V } \pm 5\%</math></b>						
$F_{IN}$	Input Frequency				200	MHz
$t_{PLH}$	Propagation Delay (Note 5)	$F_{in} = 200\text{ MHz}$	1.9		3.3	ns
$t_{SKEW}$	Output to Output Skew(Note 6)			25	45	ps
	Part to Part Skew (Note 6)			250	800	ps
$t_{SKEWDC}$	Output Duty Cycle (see Figure 3)	$F_{in} = 200\text{ MHz}$	40		60	%
$t_r/t_f$	Output rise and fall times (Note 7)	30% to 70%, $R_S = 33\ \Omega$ , $CL = 10\text{ pF}$	250		500	ps

**$T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}; V_{DD} = 3.3\text{ V } \pm 5\%, V_{DDO} = 2.5\text{ V } \pm 5\%$**

$F_{IN}$	Input Frequency				200	MHz
$t_{PLH}$	Propagation Delay (Note 5)	$F_{in} = 200\text{ MHz}$	2.2		3.7	ns
$t_{SKEW}$	Output to Output Skew(Note 6)			25	45	ps
	Part to Part Skew (Note 6)			250	500	ps
$t_{SKEWDC}$	Output Duty Cycle (see Figure 3)	$F_{in} = 200\text{ MHz}$	40		60	%
$t_r/t_f$	Output rise and fall times (Note 7)	30% to 70%, $R_S = 33\ \Omega$ , $CL = 10\text{ pF}$	200		500	ps

4. Clock input with 50% duty cycle. Outputs terminated with  $50\ \Omega$  to  $V_{DDO}/2$ . See Figures 3 and 4.

5. Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

6. Similar input conditions and the same supply voltages. Measured at  $V_{DDO}/2$ . See Figures 3 and 4.

7.  $R_S$  is Series Resistance and  $CL$  is Load Capacitance at the clock outputs.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

# NB3M8304C

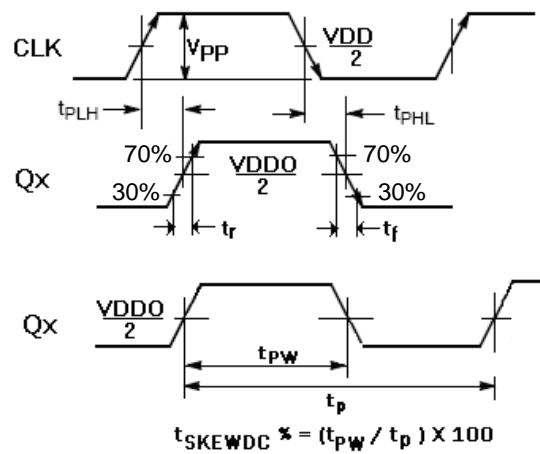
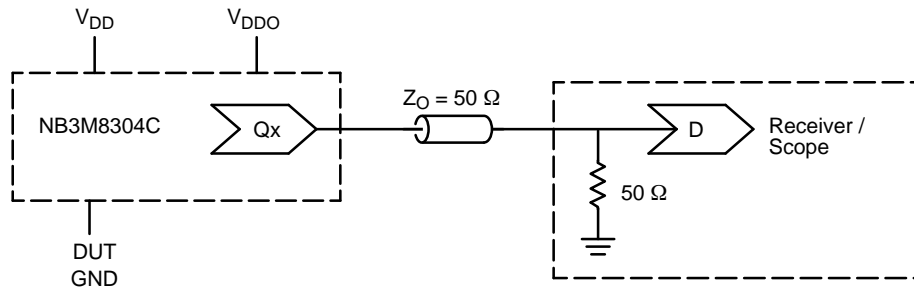


Figure 3. AC Reference Measurement



Spec Condition:	TEST SETUP V <sub>DD</sub> :	TEST SETUP V <sub>DDO</sub> :	TEST SETUP DUT GND:
V <sub>DD</sub> = V <sub>DDO</sub> = 3.3 V ±5%	1.65 V ±5%	1.65 V ±5%	-1.65 V ±5%
V <sub>DD</sub> = 3.3 V ±5%; V <sub>DDO</sub> = 2.5 V ±5%	2.05 V ±5%	1.25 V ±5%	-1.25 V ±5%

Figure 4. Output Driver Typical Device Evaluation and Termination Setup

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NB3M8304CDG	SOIC-8 (Pb-Free)	98 Units / Rail
NB3M8304CDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

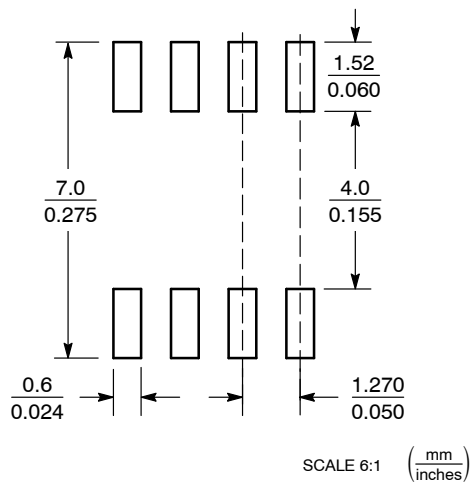


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*

### SOLDERING FOOTPRINT\*



XXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

### Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative