

74LVTH125

Low Voltage Quad Buffer with 3-STATE Outputs

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink $-32\text{mA}/+64\text{mA}$
- Functionally compatible with the 74 series 125
- Latch-up performance exceeds 500mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

General Description


The LVTH125 contains four independent non-inverting buffers with 3-STATE outputs.

These buffers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH125 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

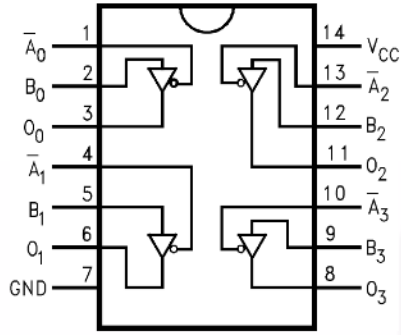
Ordering Information

Order Number	Package Number	Package Description
74LVTH125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVTH125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

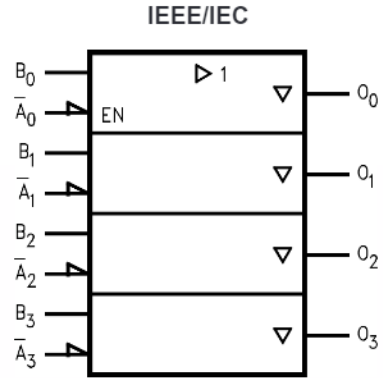
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
\bar{A}_n, B_n	Inputs
O_n	3-STATE Outputs

Truth Table

Inputs		Output
\bar{A}_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +4.6V
V_I	DC Input Voltage	-0.5V to +7.0V
V_O	DC Output Voltage Output in 3-STATE	-0.5V to +7.0V
	Output in HIGH or LOW State ⁽¹⁾	-0.5V to +7.0V
I_{IK}	DC Input Diode Current, $V_I < GND$	-50mA
I_{OK}	DC Output Diode Current, $V_O < GND$	-50mA
I_O	DC Output Current, $V_O > V_{CC}$ Output at HIGH State	64mA
	Output at LOW State	128mA
I_{CC}	DC Supply Current per Supply Pin	±64mA
I_{GND}	DC Ground Current per Ground Pin	±128mA
T_{STG}	Storage Temperature	-65°C to +150°C

Note:

- I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		-32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	-40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = -40°C to +85°C			Units	
				Min.	Typ. ⁽²⁾	Max.		
V _{IK}	Input Clamp Diode Voltage	2.7	I _I = -18mA			-1.2	V	
V _{IH}	Input HIGH Voltage	2.7-3.6	V _O ≤ 0.1V or	2.0			V	
V _{IL}	Input LOW Voltage	2.7-3.6	V _O ≥ V _{CC} - 0.1V			0.8	V	
V _{OH}	Output HIGH Voltage	2.7-3.6	I _{OH} = -100μA	V _{CC} - 0.2			V	
		2.7	I _{OH} = -8mA	2.4				
		3.0	I _{OH} = -32mA	2.0				
V _{OL}	Output LOW Voltage	2.7	I _{OL} = 100μA			0.2	V	
			I _{OL} = 24mA			0.5		
		3.0	I _{OL} = 16mA			0.4		
			I _{OL} = 32mA			0.5		
	I _{OL} = 64mA			0.55				
I _{I(HOLD)}	Bushold Input Minimum Drive	3.0	V _I = 0.8V	75			μA	
			V _I = 2.0V	-75				
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	3.0	⁽³⁾	500			μA	
			⁽⁴⁾	-500				
I _I	Input Current	3.6	V _I = 5.5V			10	μA	
		Control Pins	3.6	V _I = 0V or V _{CC}				±1
		Data Pins	3.6	V _I = 0V				-5
				V _I = V _{CC}				1
I _{OFF}	Power Off Leakage Current	0	0V ≤ V _I or V _O ≤ 5.5V			±100	μA	
I _{PU/PD}	Power up/down 3-STATE Output Current	0-1.5	V _O = 0.5V to 3.0V, V _I = GND or V _{CC}			±100	μA	
I _{OZL}	3-STATE Output Leakage Current	3.6	V _O = 0.5V			-5	μA	
I _{OZH}	3-STATE Output Leakage Current	3.6	V _O = 3.0V			5	μA	
I _{OZH+}	3-STATE Output Leakage Current	3.6	V _{CC} < V _O ≤ 5.5V			10	μA	
I _{CCH}	Power Supply Current	3.6	Outputs HIGH			0.19	mA	
I _{CCL}	Power Supply Current	3.6	Outputs LOW			5	mA	
I _{CCZ}	Power Supply Current	3.6	Outputs Disabled			0.19	mA	
I _{CCZ+}	Power Supply Current	3.6	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled			0.19	mA	
ΔI _{CC}	Increase in Power Supply Current ⁽⁵⁾	3.6	One Input at V _{CC} - 0.6V, Other Inputs at V _{CC} or GND			0.2	mA	

Notes:

- All typical values are at V_{CC} = 3.3V, T_A = 25°C.
- An external driver must source at least the specified current to switch from LOW-to-HIGH.
- An external driver must sink at least the specified current to switch from HIGH-to-LOW.
- This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics(6)

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			Units
			C _L = 50 pF, R _L = 500Ω	Min.	Typ.	Max.	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	(7)		0.8		V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	(7)		-0.8		V

Notes:

6. Characterized in SOIC package. Guaranteed parameter, but not tested.
 7. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, C _L = 50pF, R _L = 500Ω					Units
		V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V		
		Min.	Typ. ⁽⁸⁾	Max.	Min.	Max.	
t _{PLH}	Propagation Delay, Data to Output	1.0		3.5	1.0	4.5	ns
t _{PHL}		1.0		3.9	1.0	4.9	
t _{PZH}	Output Enable Time	1.0		4.0	1.0	5.5	ns
t _{PZL}		1.1		4.0	1.1	5.4	
t _{PHZ}	Output Disable Time	1.5		4.5	1.5	5.7	ns
t _{PLZ}		1.3		4.5	1.3	4.0	
t _{OSSL} , t _{OSSLH}	Output to Output Skew ⁽⁹⁾			1.0		1.0	ns

Notes:

8. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
 9. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSSLH}).

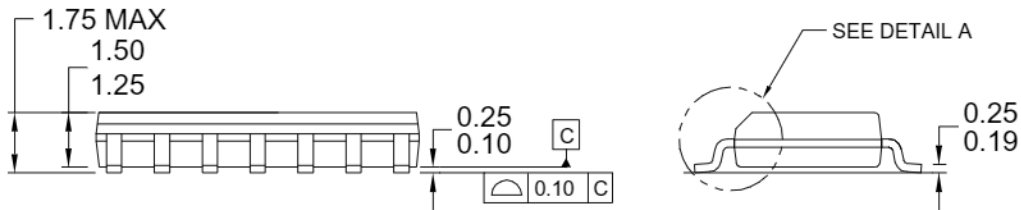
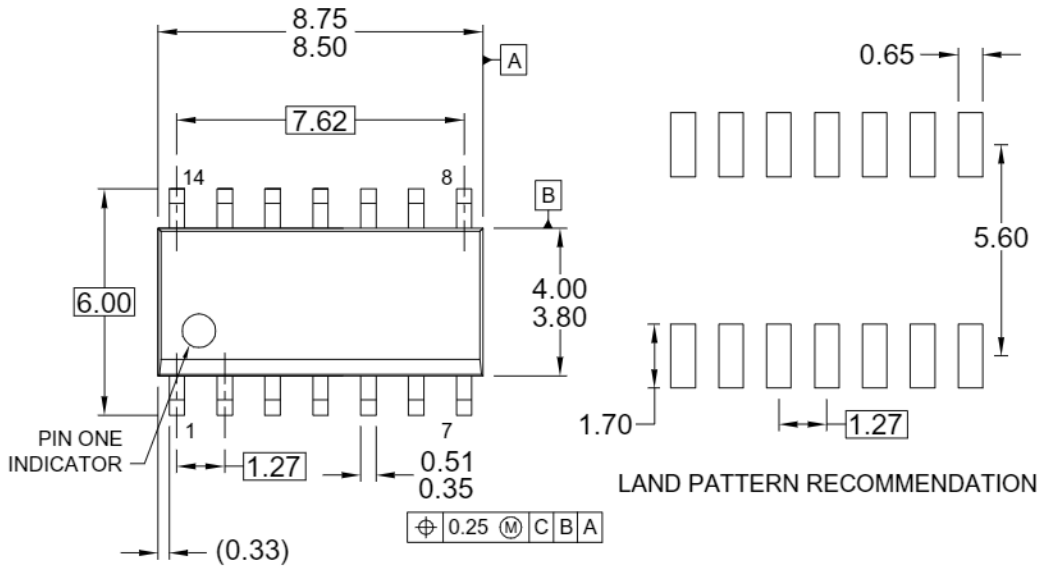
Capacitance⁽¹⁰⁾

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}	4	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

Note:

10. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

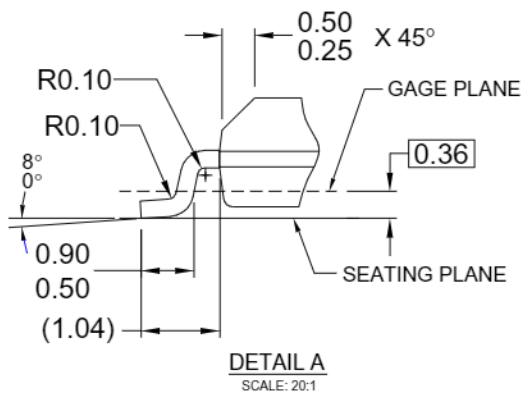


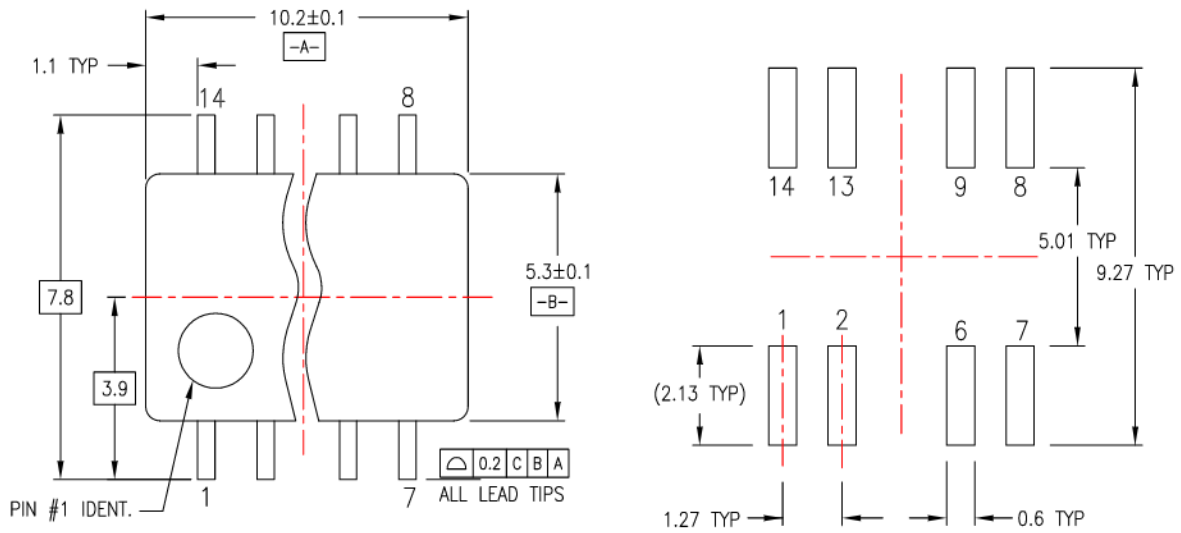
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

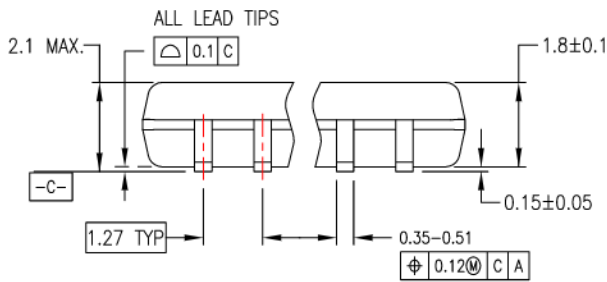
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



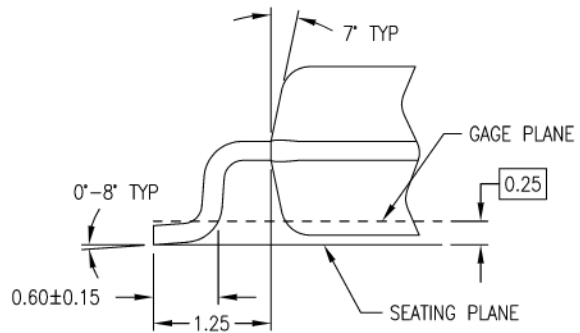
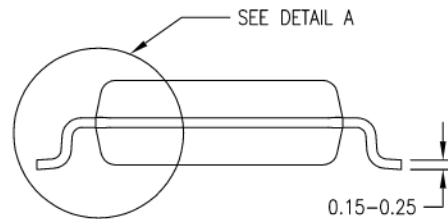
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DREVC

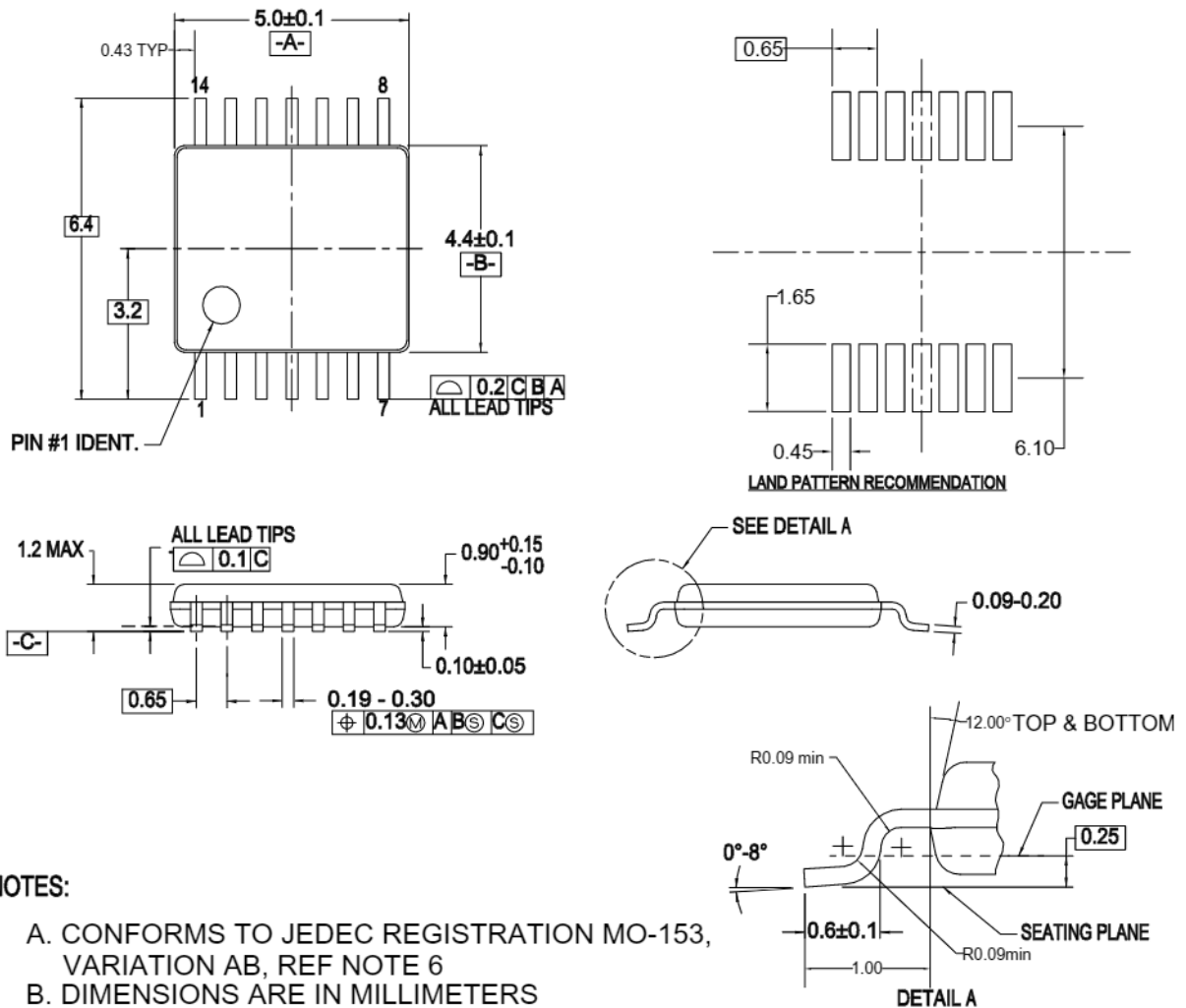
Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|---|--|--|----------------------------------|
| ACEx [®] | FPS [™] | PDP-SPM [™] | SupreMOS [™] |
| Build it Now [™] | FRFET [®] | Power220 [®] | SyncFET [™] |
| CorePLUS [™] | Global Power Resource SM | POWEREDGE [®] | SYSTEM GENERAL [®] |
| CROSSVOLT [™] | Green FPS [™] | Power-SPM [™] | The Power Franchise [®] |
| CTL [™] | Green FPS [™] e-Series [™] | PowerTrench [®] | power [®] |
| Current Transfer Logic [™] | GTO [™] | Programmable Active Droop [™] | the franchise |
| EcoSPARK [®] | i-Lo [™] | QFET [®] | TinyBoost [™] |
| EZSWITCH [™] * | IntelliMAX [™] | QS [™] | TinyBuck [™] |
|  ™ | ISOPLANAR [™] | QT Optoelectronics [™] | TinyLogic [®] |
|  ™ | MegaBuck [™] | Quiet Series [™] | TINYOPTO [™] |
| Fairchild [®] | MICROCOUPLER [™] | RapidConfigure [™] | TinyPower [™] |
| Fairchild Semiconductor [®] | MicroFET [™] | SMART START [™] | TinyPWM [™] |
| FACT Quiet Series [™] | MicroPak [™] | SPM [®] | TinyWire [™] |
| FACT [®] | MillerDrive [™] | STEALTH [™] | μSerDes [™] |
| FAST [®] | Motion-SPM [™] | SuperFET [™] | UHC [®] |
| FastvCore [™] * | OPTOLOGIC [®] | SuperSOT [™] 3 | Ultra FRFET [™] |
| FlashWriter [®] * | OPTOPLANAR [®] | SuperSOT [™] 6 | UniFET [™] |
| | | SuperSOT [™] 8 | VCX [™] |

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33