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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

SEMICONDUCTOR®

74AC86
Quad 2-Input Exclusive-OR Gate

General Description

The AC86 contains four, 2-input exclusive-OR gates.

Features

■ I_{CC} reduced by 50%

■ Outputs source/sink 24 mA

Ordering Code:

Order Number	Package Number	Package Description
74AC86SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC86SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC86MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC86PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram

Logic Symbol

IEEE/IEC
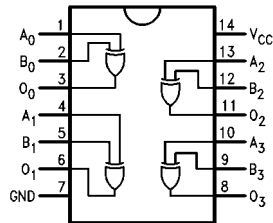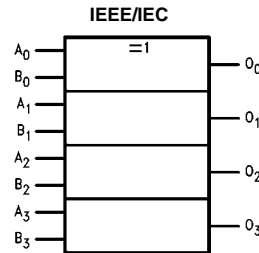
Pin Descriptions

Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = 0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
$V_O = −0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
Per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	$T_A = −40°C$ to +85°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} − 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} − 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = −50 \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = −12$ mA
		4.5		3.86	3.76		$I_{OH} = −24$ mA
		5.5		4.86	4.76		$I_{OH} = −24$ mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA
		4.5		0.36	0.44		$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 20 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
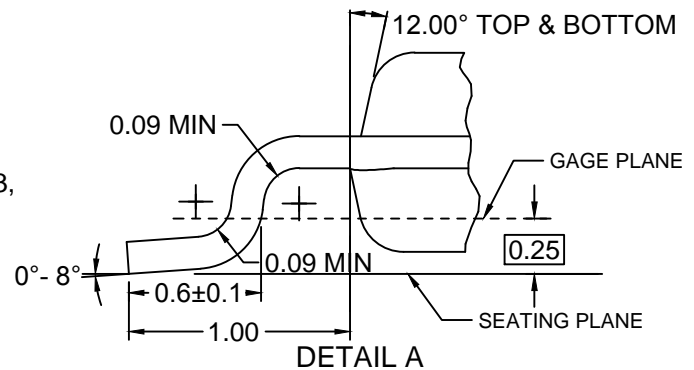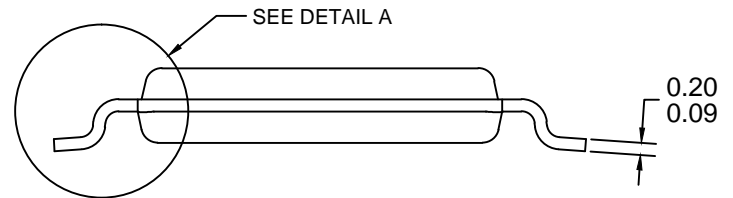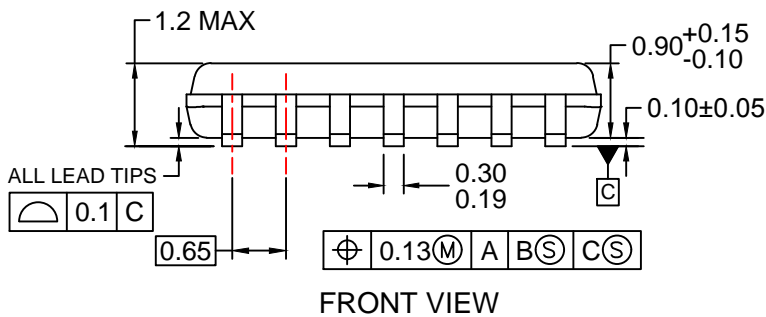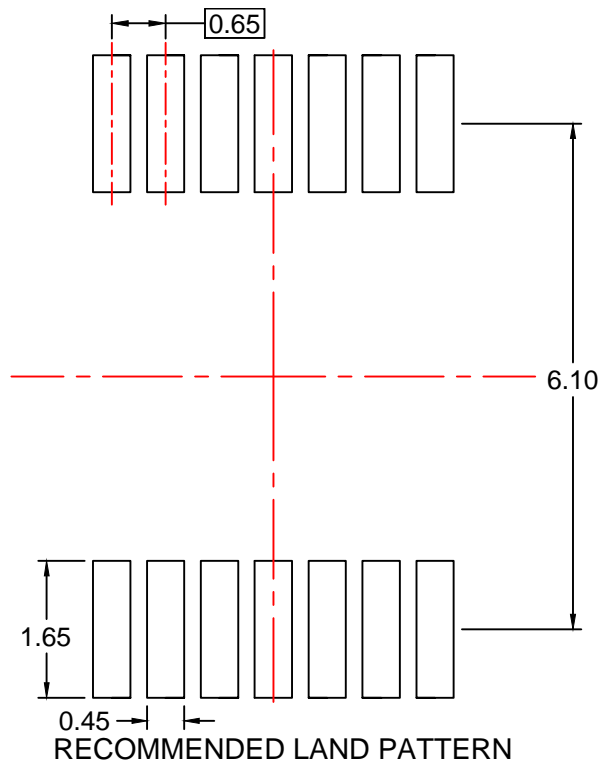
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$ $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$ C_L 40 pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	3.3	2.0	6.0	11.5	1.5	12.5	ns
	Inputs to Outputs	5.0	1.5	4.5	8.5	1.0	9.5	
t_{PLH}	Propagation Delay	3.3	2.0	6.5	11.5	1.5	12.5	ns
	Inputs to Outputs	5.0	1.5	4.5	8.5	1.0	9.0	

Note 5: Voltage Range 3.3V is 3.3V ± 0.3V
Voltage Range 5.0V is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0V

TOP VIEW

5.00±0.10   A

0.43TYP

14   8

6.4

4.40±0.10

3.2

PIN#1 IDENT

1   7

⌒ | 0.2 | C | B | A
ALL LEAD TIPS

RECOMMENDED LAND PATTERN

0.65

6.10

1.65

0.45

FRONT VIEW

1.2 MAX

$0.90^{+0.15}_{-0.10}$

0.10±0.05

ALL LEAD TIPS

⌒ | 0.1 | C

0.65

0.30
0.19

C

⊕ | 0.13 Ⓜ | A | B Ⓢ | C Ⓢ

DETAIL A

SEE DETAIL A

0.20
0.09

12.00° TOP & BOTTOM

0.09 MIN

GAGE PLANE

0.25

0°- 8°

0.09 MIN

0.6±0.1

1.00

SEATING PLANE
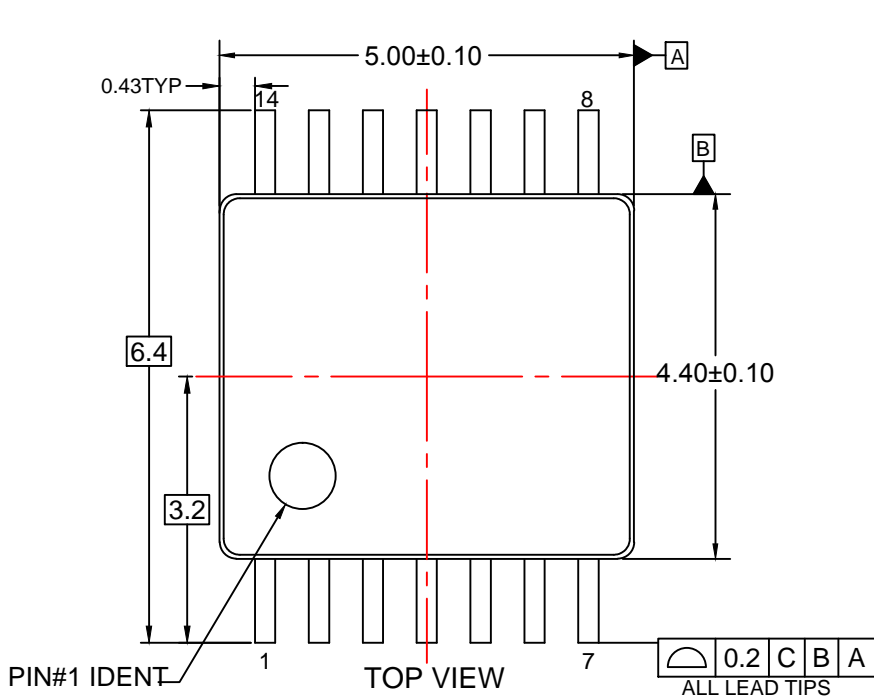
NOTES:
 A. CONFORMS TO JEDEC REGISTRATION MO-153,
    VARIATION AB, REF NOTE 6
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
    MOLD FLASH, AND TIE BAR EXTRUSIONS
 D. DIMENSIONING AND TOLERANCES PER ANSI
    Y14.5M, 2009.
 E. LANDPATTERN STANDARD: SOP65P640X110-14M.
 F. DRAWING FILE NAME: MKT-MTC14rev7.

FAIRCHILD.

TOP VIEW

8.75
8.50

7.62

14

8

| A |

| B |

6.00

4.00
3.80

PIN #1
IDENT.

1

7

1.27

0.51
0.35

(0.33)

⊕ | 0.25 Ⓜ | C | B | A |

LAND PATTERN RECOMMENDATION

14

0.65

8

5.60

1.70

1

7

1.27

FRONT VIEW

1.75 MAX

| C |

1.50
1.25

0.25
0.10

⌓ | 0.10 | C |

SIDE VIEW

A

0.25
0.19
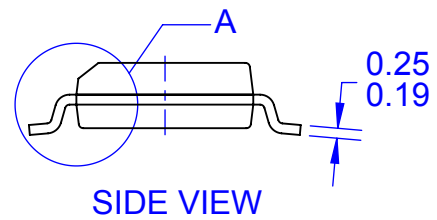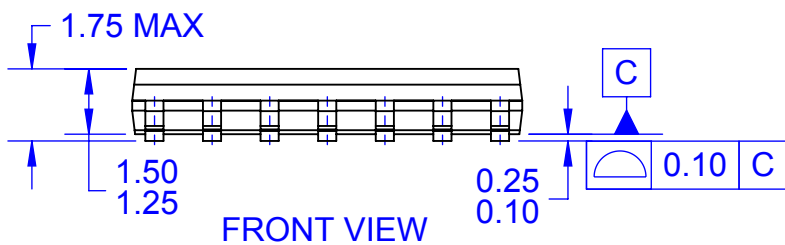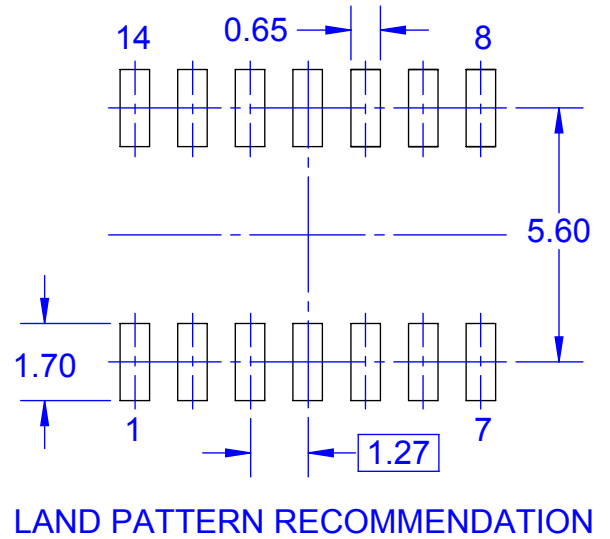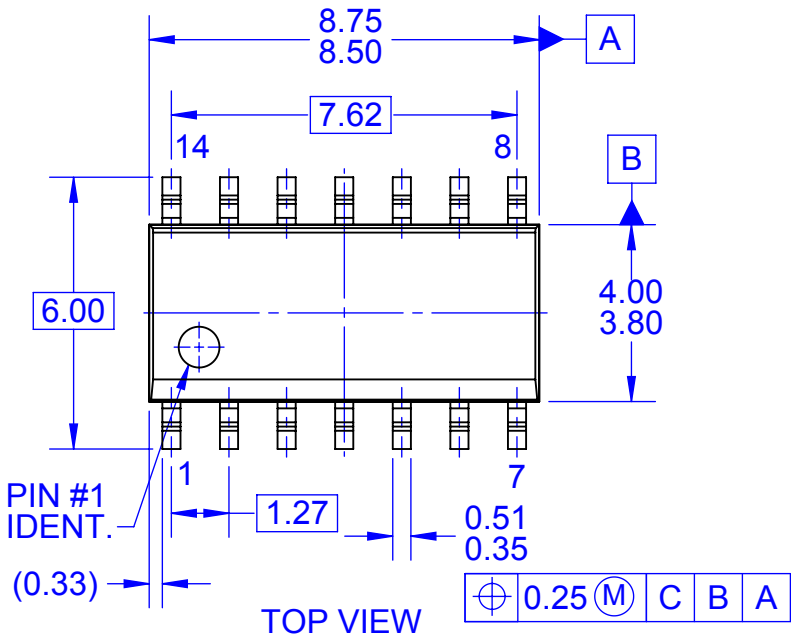
NOTES:
A. CONFORMS TO JEDEC MS-012,
   VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS
D. LAND PATTERN STANDARD:
   SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14

DETAIL A
SCALE 16 : 1

0.50
0.25 X 45°

R0.10

GAGE
PLANE

R0.10

0.36

8°
0°

0.90
0.50

(1.04)

SEATING PLANE

PUBLICATION ORDERING INFORMATION
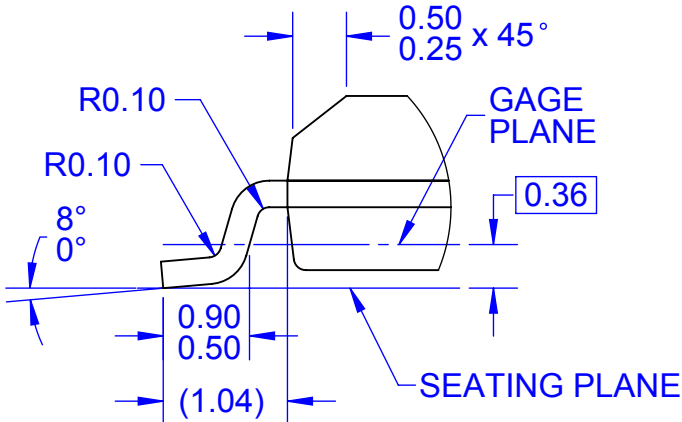
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