

# AR0147

## 1/4-Inch CMOS Digital Image Sensor

ON Semiconductor AR0147AT is a 1/4-inch CMOS digital image sensor with a 1344 H x 968 V active-pixel array. This advanced automotive sensor captures images in either linear, or high dynamic range, with rolling-shutter readout. AR0147AT is optimized for both low light and challenging high dynamic range scene performance, with a 3  $\mu\text{m}$  BSI pixel and on-sensor up to 140 dB (See Note 3 of Table 1) 4-exp HDR, and up to 120 dB with on-chip 3-exp HDR and Super-Exposure(SE) + T2 capture capability. The sensor includes flexible functions such as in-sensor binning, windowing, and both video and single frame modes. The sophisticated sensor real time safety mechanism and fault detection features on AR0147AT enable ASIL-B compliance. The device is programmable through a simple two-wire serial interface, and supports both MIPI CSI-2 and Parallel output interfaces.

**Table 1. KEY PARAMETERS**

| Parameter                  | Value  |
|----------------------------|--|
| Optical format             | 1/4 inch   |
| Maximum resolution         | 1344 x 968 (1.3 Mp)  |
| Shutter type               | Electronic Rolling Shutter (ERS)   |
| Pixel size                 | 3 $\mu\text{m}$  |
| Pixel output interfaces    | MIPI CSI-2<br>12-bit parallel  |
| Output formats             | 12-bit Uncompressed Linear<br>20-bit Uncompressed HDR<br>10-bit Companded Linear<br>16-bit, 14-bit, or 12-bit Companded HDR              |
| Control interface          | 2-wire, Serial Control 100 kHz/400 kHz/1 MHz   |
| Input clock range          | 12–50 MHz in PLL mode  |
| Frame Rate                 | 60 fps (legacy 3-exp) and 30 fps (SE+T2) (Note 1)  |
| Output pixel clock maximum | 89.1 MHz (legacy 3-exp) and 56 MHz (SE+T2) (Note 1)  |
| Responsivity               | 30.7 Ke-/lux-sec (Note 2)  |
| SNRmax                     | >43.1 dB (>50 dB in SE)  |
| Max Dynamic Range          | 120 dB (3-exp HDR and SE + T2) on chip and<br>140 dB 4-exp HDR off chip (Note 3)   |
| Packaging options          | 8 mm x 7 mm iBGA<br>9 mm x 9 mm iBGA<br>Recon Die  |
| Operating temp. range      | –40°C to 110°C Ambient<br>–40°C to 125°C Junction  |
| Supply voltage             | I/O 1.8 V or 2.8 V<br>Digital 1.2 V<br>Analog 2.8 V  |
| Power consumption          | <270 mW typical (1344x968, 3exp HDR, 30 fps)<br><380 mW typical (1344x968, 3exp HDR, 60 fps)<br><230 mW typical (SE+T2, 1344x968, 30fps) |

1. Maximum frame rates will depend on various sensor settings including resolution, output format, and output pixel clock.
2. Green pixel, D65 light, 670 nm IRCF
3. Assumes off-chip HDR linearization



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### Features

- Combined HDR RAW Output, up to 20-bit
- Support for full-resolution 120 dB to 140 dB (see Note 3 of Table 1) HDR
- New High-Performance 3  $\mu\text{m}$  BSI Pixel with Super-Exposure HDR Mode
- Advanced HDR Image Combination with Flexible Exposure Ratio Control
- 1344 x 968 at up to 60 fps (legacy 3-exp) and 30 fps (SE+T2)
- Real-time Functional Safety Mechanisms and Fault Detection
- ASIL-B and Safety Design
- 2x2 In-sensor Binning
- Data Interfaces: 4-lane MIPI CSI-2, Parallel
- Selectable Automatic or User Controlled Black Level Control
- Frame to Frame Context Switching to Enable Multi-function Systems
- Spread-spectrum Input Clock Support
- Multi-Camera Synchronization Support
- Pb-Free Devices

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## Applications

- Automotive ADAS
- Automotive Surround and Rear-View
- ADAS + Viewing Fusion
- Mirror Replacement (CMS)
- Digital Video Recorder (DVR)
- In-Cabin Monitoring

**Table 2. ORDERING INFORMATION**

| Part number             | Description      | Orderable Product Attribute Description   | Package                      |
|-------------------------|------------------|---|------------------------------|
| AR0147ATSC00XUEG0-DPBR  | RGB, 0°CRA, iBGA | Dry Pack with Protective Film, Double Side BBAR Glass                           | 8 mm x 7 mm iBGA89 (Pb-Free) |
| AR0147ATSC00XUEG0-DRBR  | RGB, 0°CRA, iBGA | Dry Pack without Protective Film, Double Side BBAR Glass                        |                              |
| AR0147ATSC00XUEG0-TPBR  | RGB, 0°CRA, iBGA | Tape & Reel with Protective Film, Double Side BBAR Glass                        |                              |
| AR0147ATSC00XUEG0-TRBR  | RGB, 0°CRA, iBGA | Tape & Reel without Protective Film, Double Side BBAR Glass                     |                              |
| AR0147ATSC00XUEGH3-GEVB | RGB, 0°CRA, iBGA | Demo3 Headboard   |                              |
| MARS1-AR0147ATS-GEVB    | RGB, 0°CRA, iBGA | MARS Sensor Board, Parallel   |                              |
| MARS1-AR0147ATSCS-GEVB  | RGB, 0°CRA, iBGA | MARS Sensor Board, MIPI   |                              |
| AR0147ATSC00XUEA0-DPBR  | RGB, 0°CRA, iBGA | Dry Pack with Protective Film, Double Side BBAR Glass, Engineering Sample       | 9 mm x 9 mm iBGA80 (Pb-Free) |
| AR0147ATSC00XUEA0-DRBR  | RGB, 0°CRA, iBGA | Dry Pack without Protective Film, Double Side BBAR Glass, Engineering Sample    |                              |
| AR0147ATSC00XUEA0-TPBR  | RGB, 0°CRA, iBGA | Tape & Reel with Protective Film, Double Side BBAR Glass, Engineering Sample    |                              |
| AR0147ATSC00XUEA0-TRBR  | RGB, 0°CRA, iBGA | Tape & Reel without Protective Film, Double Side BBAR Glass, Engineering Sample |                              |

NOTE: Contact the ON Semiconductor sales or marketing representative to discuss your specific requirements.

### General Description

The ON Semiconductor AR0147AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1344 x 968 resolution image at up to 60 fps (legacy 3-exp) and 30 fps (SE+T2). In linear mode, it outputs 12-bit raw data, using serial MIPI and parallel output ports. In high dynamic range mode, it outputs 12-bit, 14-bit or 16-bit compressed or 20-bit linearized data using the MIPI port. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME\_VALID, LINE\_VALID and pixel clock can be programmed to output by GPIO pins in serial mode.

The AR0147AT includes additional features to allow application-specific tuning: windowing and offset, auto black level correction, and on-board temperature sensor.

Optional register information and histogram statistic information can be embedded in first and last two or four lines of the image frame.

The sensor is designed to operate in a wide temperature range (-40°C to +125°C junction).

### Functional Overview

The AR0147AT is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 12 and 50 MHz. The maximum output pixel rate is 89.1 Mp/s (legacy 3-exp) and 56 Mp/s (SE+T2). Figure 1 shows a block diagram of the sensor.

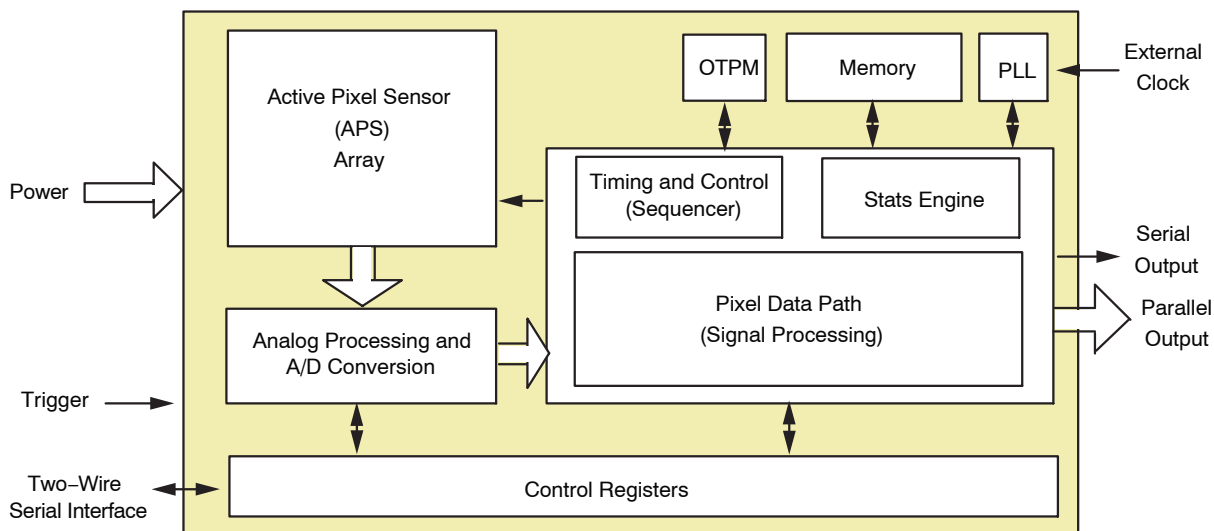


Figure 1. Block Diagram

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.3 Mp BSI Active-Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 13-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined onchip to produce a single image at 20-bit per pixel value. A compressing mode is further offered to allow this 20-bit

pixel value to be transmitted to the host system as a 12- or 14- or 16-bit value with close to zero loss in image quality. The pixel data are output at a rate of up to 89.1 Mp/s (legacy 3-exp) and 56 Mp/s (SE+T2).

### Features Overview

The AR0147AT has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0147AT Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- Operating Modes

The AR0147AT works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes.

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- **Window Control**  
Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations. Binning not supported.
- **Context Switching**  
Context switching may be used to rapidly switch between two sets of register values. Refer to the AR0147AT Developer Guide for a complete set of context switchable registers. RAM based context switching supported, Up to 16 contexts can be configured.
- **Gain**  
The AR0147AT can be configured for analog gain of up to 8x, and digital gain of up to 16x.
- **MIPI**  
The AR0147 image sensor supports 4-lane MIPI CSI-2 D-PHY
- **PLL**  
An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.
- **Reset**  
The AR0147AT may be reset by a register write, or by a dedicated input pin.

- **Output Enable**  
The AR0147AT output pins may be tri-stated using dedicated register bits.
- **Temperature Sensor**
- **Black Level Correction**
- **Row Noise Correction**
- **Digital Correlated Double Sampling (CDS)**
- **Test Patterns**  
Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to gray, and a walking 1s test pattern.

### ASIL / ISO26262 Support Features

The AR0147AT incorporates many features assisting the achievement of ASIL-B system compliance by a system that integrates it. Please refer to the AR0147AT Safety Manual for more information.

### Operating Modes:

The AR0147AT has versatile operating modes including multi-exposure HDR (regular modes), Super-Exposure HDR mode and in a combined HDR and line interleaved mode (LICM). It has the ability to output HDR frames combined on-chip, or as separate frames in Line Interleaved Mode (LIM). Below are a list of some of the operating modes supported and maximum possible frame rates in each mode.

**Table 3. OPERATING MODES**

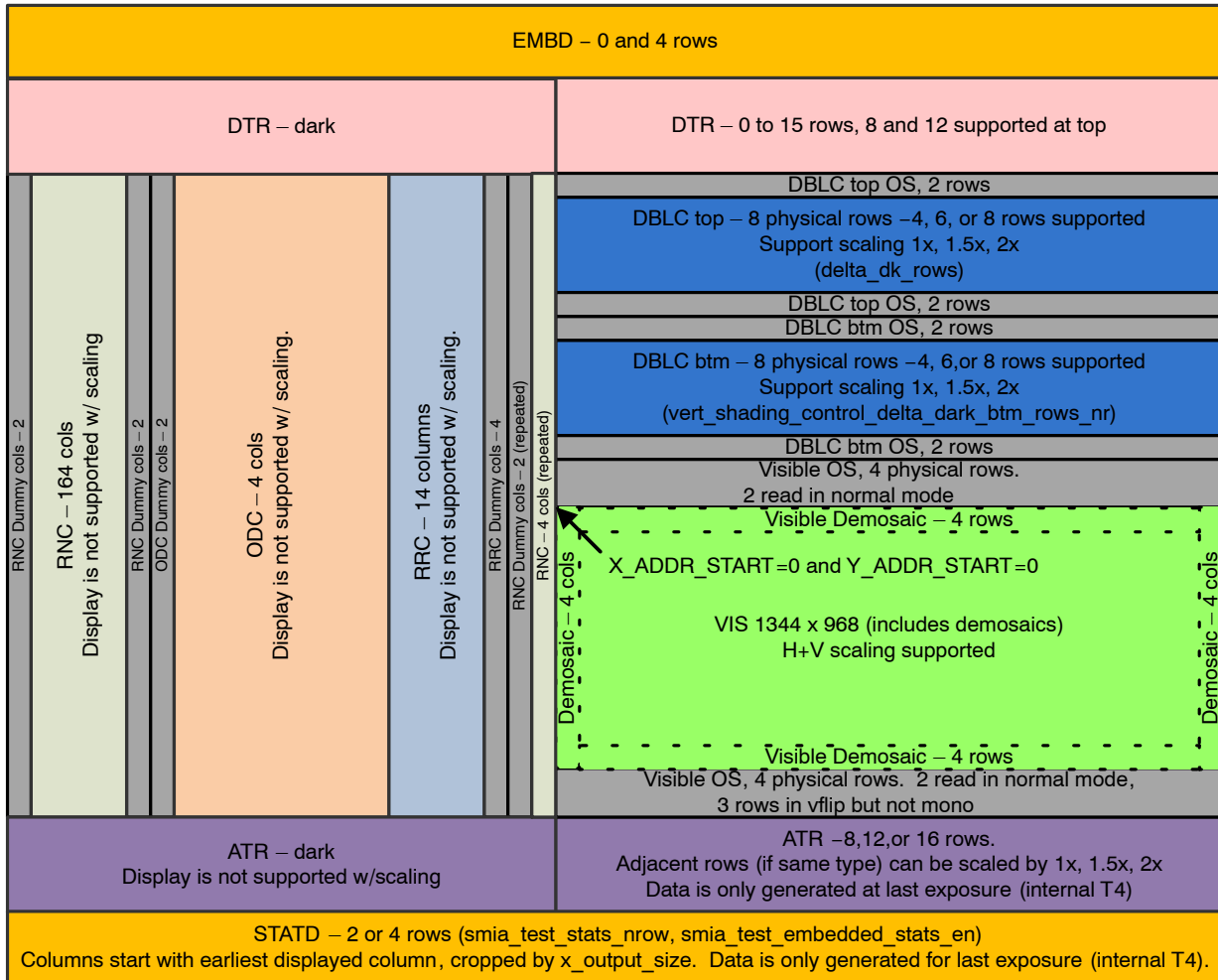
| No.                         | Modes                  | Number of Exposures | Output Description    | Resolution | Bit Width | Maximum Achievable Frame Rate (fps) |
|-----------------------------|------------------------|---------------------|-----------------------|------------|-----------|-------------------------------------|
| <b>REGULAR MODES</b>        |                        |                     |                       |            |           |                                     |
| 1                           | Linear                 | 1                   | Linear                | 1344x968   | 12 bit    | 60                                  |
| 2                           | T1 + T2 + T3 + T4      | 4                   | HDR                   | 1344x968   | 20 bit    | 45                                  |
| 3                           | T1, T2, T3, T4         | 4                   | LICM                  | 1344x968   | 12 bit    | 40                                  |
| 4                           | T1 + T2 + T3           | 3                   | HDR                   | 1344x968   | 20 bit    | 60                                  |
| 5                           | T1, T2, T3             | 3                   | LICM                  | 1344x968   | 12 bit    | 40                                  |
| <b>SUPER-EXPOSURE MODES</b> |                        |                     |                       |            |           |                                     |
| 6                           | Super-Exposure T1      | 1                   | Flicker Free 95dB HDR | 1344x968   | 16 bit    | 40                                  |
| 7                           | Super-Exposure T1 + T2 | 2                   | 120dB HDR             | 1344x968   | 20 bit    | 30                                  |

**Frame Readout:**

The following section provides figures that describe the **data types** that can be output in each frame. Each frame may contain different fields of embedded or statistics data. Please refer to details just below the image to see information on different data fields and their description including active image data.

- Each row readout happens from left to right (R0: T1→T2→T3→T4; R1: T1→T2→T3→T4; ... so on)
- Embedded data will be available only on the T1 Data frame.
- Stats data will be available only on the T4 data frame.
- RNC is available only for T4 and on the T4 data frame.
- ATR is available only on the T4 data frame.

**TYPICAL FRAME READOUT FORMAT**



**Figure 2. Typical Frame Readout Format**

- EMBD: Embedded Data Rows (Registers information)
- DTR: Digital Test Rows (Digital ASIL check)
- RNC: Row Noise Correction Columns
- ODC: Optically Dark Columns
- RRC: Row ROM Columns
- DBLC: Digital Black Level Correction Rows
- OS: OverScan Rows
- ATR: Analog Test Rows
- STATD: Statistics Data Rows

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## PIXEL DATA FORMAT

### Pixel Array Structure

The AR0147AT pixel array is configured as 1550 columns by 1052 rows (see Figure 3). The dark pixels are optically black and are used internally to monitor black level. There are 1344 columns by 968 rows of optically active pixels. While the sensor's format is 1344 x 968, the additional active columns and active rows are included for use when

horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out. The optical center of the readable active pixels can be found between Change to: X\_ADDR 671 and 672, and between Y\_ADDR 483 and 484.

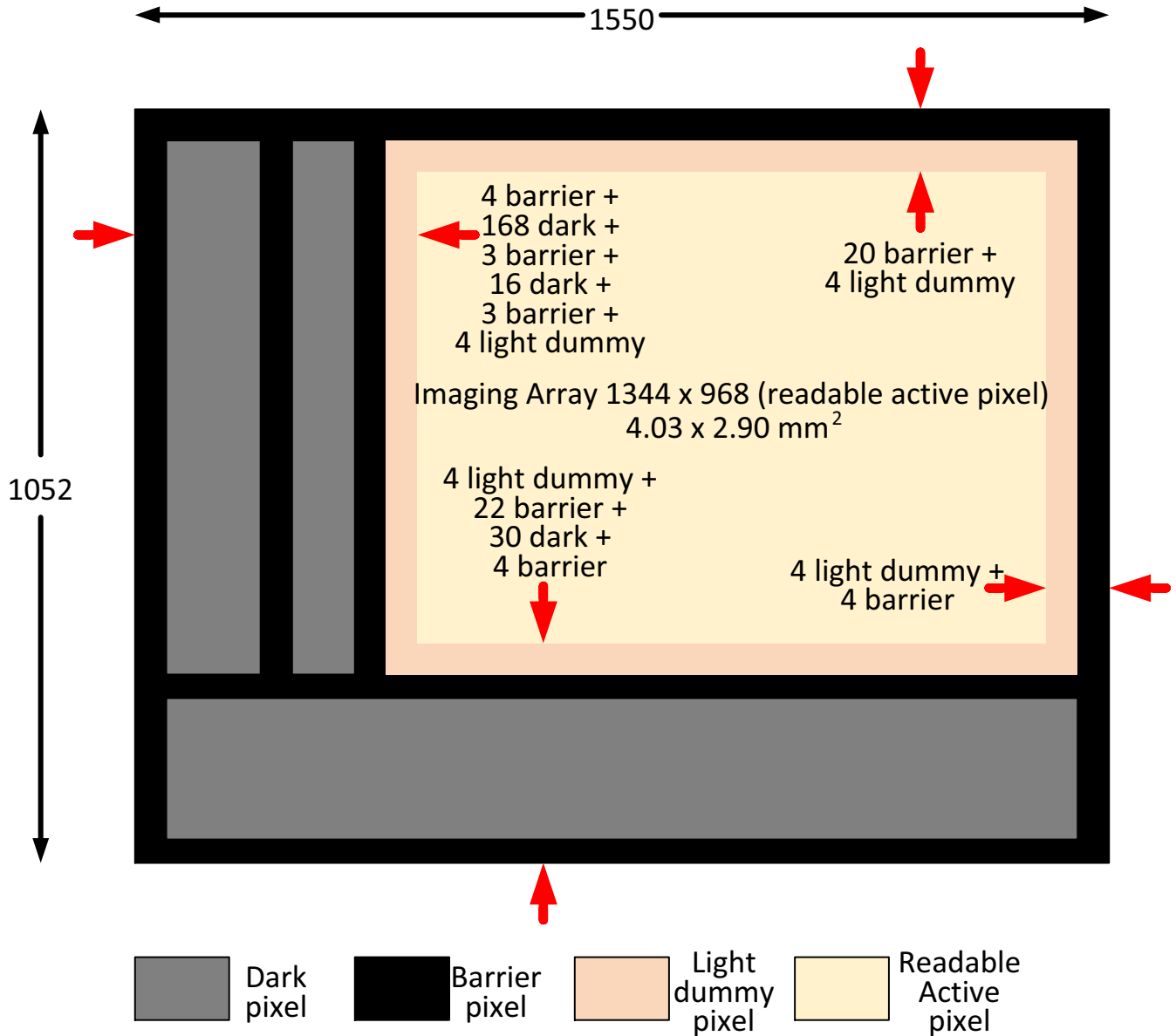


Figure 3. Pixel Array Description

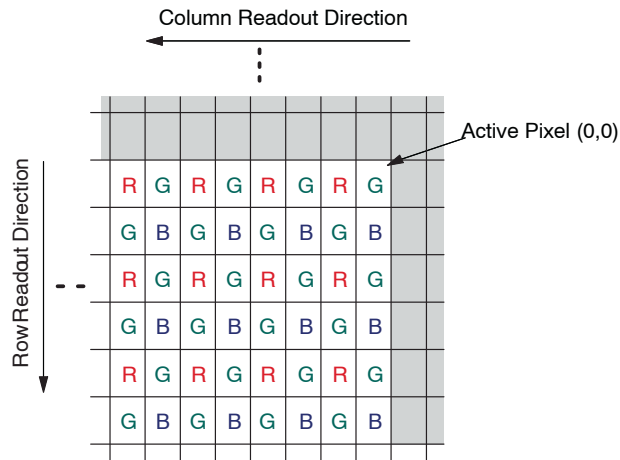


Figure 4. Pixel Color Pattern Detail (Top Right Corner) Bayer

**Default Readout Order**

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner. This reflects the actual layout of the array on the die.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 5. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 5.

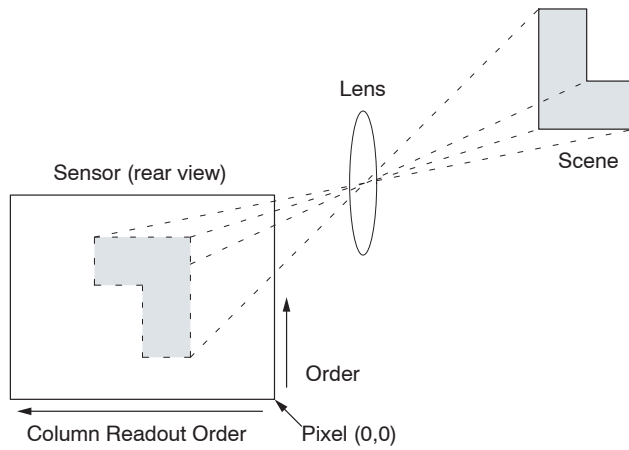
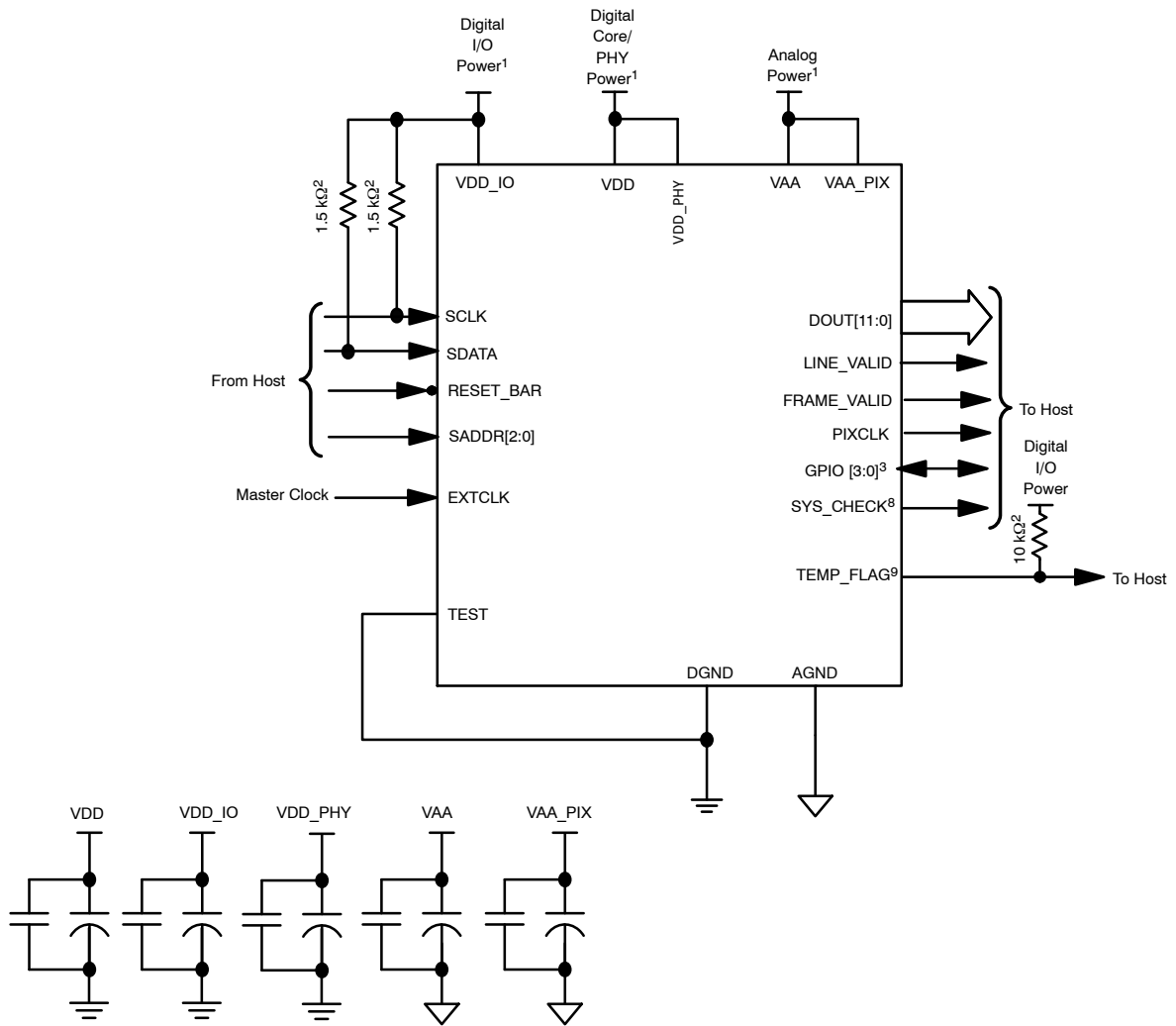


Figure 5. Imaging a Scene

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**Figure 6. Typical Configuration, Parallel**

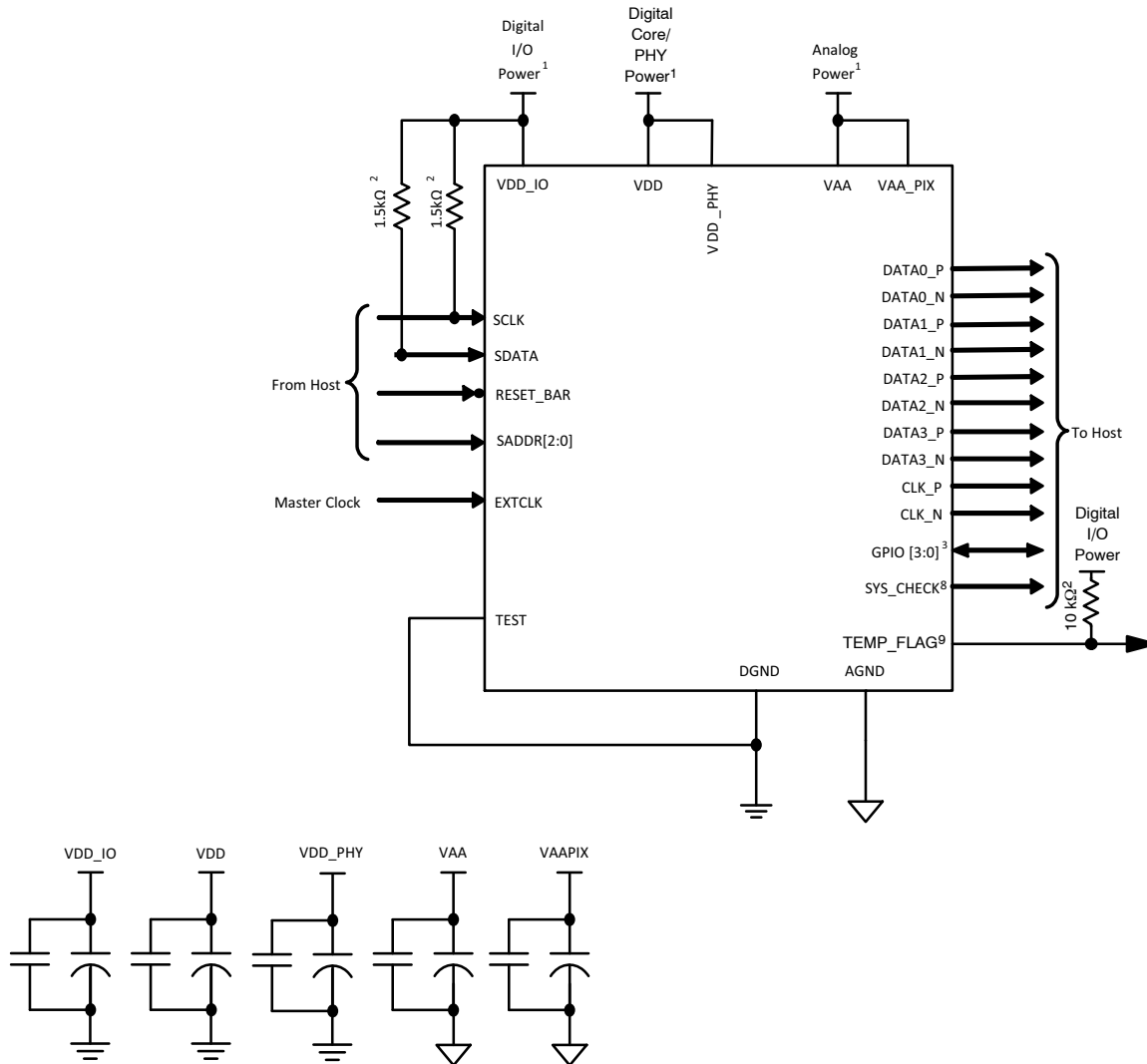
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The serial output data interface pads can be left unconnected when the parallel output interface is used. The serial output data supply pads should remain connected and powered appropriately.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0147AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD\_IO voltage to minimize any leakage currents.
8. Leave unconnected if not used.
9. Open drain. Leave unconnected if not used.



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## CONFIGURATION AND PINOUT

The figures and tables below show a typical configuration for the AR0147 image sensor and show the package pinout.



**Figure 7. Typical Configuration, 4-Lane MIPI**

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0147AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD\_10 voltage to minimize any leakage currents.
8. Leave unconnected if not used.
9. Open drain. Leave unconnected if not used.

Table 4. PIN DESCRIPTIONS, 8 X 7 MM, 89-BALL IBGA

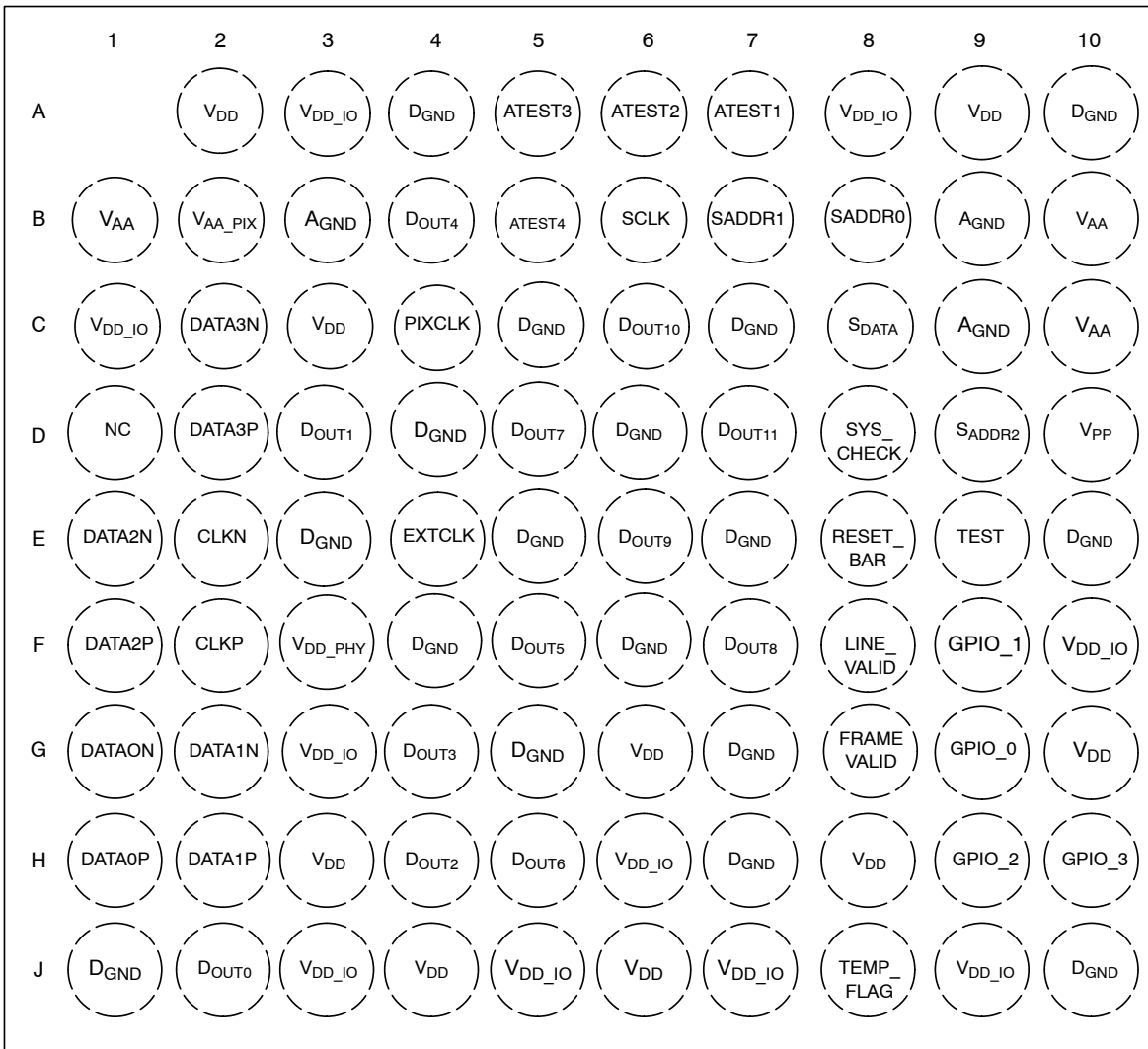
| Pin Name    | iBGA Pin | Type         | Description   | Comments  |
|-------------|----------|--------------|---|---|
| EXTCLK      | E4       | Input        | Master input clock. PLL input clock.  | Connect to clock source. Min and Max frequency depends upon output port and clocking method.  |
| RESET_BAR   | E8       | Input        | Asynchronous active-low reset.  | Connect to host.  |
| SCLK        | B6       | Input        | CCI clock for access to control and status registers  | Connect to host.  |
| SDATA       | C8       | Input/Output | CCI data for reads from and writes to control and status registers  | Connect to host.  |
| SADDR0      | B8       | Input        | CCI interface device address select bit 0.  | Selects CCI address. 000b sets the address to 0x20/0x21. 001b sets the address to 0x30/0x31. Connect to VDD_IO or DGND accordingly. |
| SADDR1      | B7       | Input        | CCI interface device address select bit 1.  |   |
| SADDR2      | D9       | Input        | CCI interface device address select bit 2.  |   |
| PIXCLK      | C4       | Output       | Parallel data output pixel clock. Used to qualify the LINE_VALID, FRAME_VALID, and DOUT11 to DOUT0 outputs. | Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12-bit parallel configuration.                     |
| FRAME_VALID | G8       | Output       | Parallel data output FRAME_VALID output. Qualified by PIXCLK.   |   |
| LINE_VALID  | F8       | Output       | Parallel data output LINE_VALID output. Qualified by PIXCLK.  |   |
| DOUT11      | D7       | Output       | Parallel data output pixel data bit 11. Qualified by PIXCLK.  | Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12-bit parallel configuration.                     |
| DOUT10      | C6       | Output       | Parallel data output pixel data bit 10. Qualified by PIXCLK.  |   |
| DOUT9       | E6       | Output       | Parallel data output pixel data bit 9. Qualified by PIXCLK.   |   |
| DOUT8       | F7       | Output       | Parallel data output pixel data bit 8. Qualified by PIXCLK.   |   |
| DOUT7       | D5       | Output       | Parallel data output pixel data bit 7. Qualified by PIXCLK.   |   |
| DOUT6       | H5       | Output       | Parallel data output pixel data bit 6. Qualified by PIXCLK.   |   |
| DOUT5       | F5       | Output       | Parallel data output pixel data bit 5. Qualified by PIXCLK.   |   |
| DOUT4       | B4       | Output       | Parallel data output pixel data bit 4. Qualified by PIXCLK.   |   |
| DOUT3       | G4       | Output       | Parallel data output pixel data bit 3. Qualified by PIXCLK.   |   |
| DOUT2       | H4       | Output       | Parallel data output pixel data bit 2. Qualified by PIXCLK.   |   |
| DOUT1       | D3       | Output       | Parallel data output pixel data bit 1. Qualified by PIXCLK.   |   |
| DOUT0       | J2       | Output       | Parallel data output pixel data bit 0. Qualified by PIXCLK.   |   |

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**Table 4. PIN DESCRIPTIONS, 8 X 7 MM, 89–BALL IBGA**

| Pin Name  | iBGA Pin  | Type         | Description                               | Comments  |
|-----------|---|--------------|---|---|
| CLKP      | F2  | Output       | Differential Mipi serial clock            | Connect to host/receiver or can be left floating if not used. Use DATA0 for 1 lane configuration or DATA0 and DATA1 for 2 lane configuration. |
| CLKN      | E2  | Output       | Differential Mipi serial clock            |   |
| DATA3P    | D2  | Output       | Differential Mipi serial data lane 3.     |   |
| DATA3N    | C2  | Output       | Differential Mipi serial data lane 3.     |   |
| DATA2P    | F1  | Output       | Differential Mipi serial data lane 2.     |   |
| DATA2N    | E1  | Output       | Differential Mipi serial data lane 2.     |   |
| DATA1P    | H2  | Output       | Differential Mipi serial data lane 1.     |   |
| DATA1N    | G2  | Output       | Differential Mipi serial data lane 1.     |   |
| DATA0P    | H1  | Output       | Differential Mipi serial data lane 0.     |   |
| DATA0N    | G1  | Output       | Differential Mipi serial data lane 0.     |   |
| TEST      | E9  | Input        | Enable manufacturing test modes.          | Tie to DGND.  |
| ATEST1    | A7  | Input/Output | Analog manufacturing test access          | Leave unconnected.  |
| ATEST2    | A6  | Input/Output | Analog manufacturing test access          |   |
| ATEST3    | A5  | Input/Output | Analog manufacturing test access          |   |
| ATEST4    | B5  | Input/Output | Analog manufacturing test access          |   |
| GPIO_0    | G9  | Input/Output | GPIO Pin 0                                | GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.  |
| GPIO_1    | F9  | Input/Output | GPIO Pin 1                                |   |
| GPIO_2    | H9  | Input/Output | GPIO Pin 2                                |   |
| GPIO_3    | H10   | Input/Output | GPIO Pin 3                                |   |
| SYS_CHECK | D8  | Output       | Combined OR of error flags.               | Leave unconnected if not used.  |
| TEMP_FLAG | J8  | Output       | Temperature monitoring flag.              | Open–drain. Leave unconnected if not used.  |
| DGND      | A4, A10, C5, C7, D4, D6, E10, E3, E5, E7, F4, F6, G5, G7, H7, J1, J10 | Power        | Digital ground.                           |   |
| VDD       | A2, A9, C3, G6, G10, H3, H8, J4, J6                                   | Power        | Core digital power.                       |   |
| VDD_PHY   | F3  | Power        | PHY digital power.                        | Connect to VDD.   |
| VDD_IO    | A3, A8, C1, F10, G3, H6, J3, J5, J7, J9                               | Power        | Digital I/O power.                        |   |
| AGND      | B3, B9, C9  | Power        | Analog ground.                            |   |
| VAA       | B1, B10, C10  | Power        | Analog power.                             |   |
| VAA_PIX   | B2  | Power        | Analog pixel array power.                 | Connect to VAA.   |
| VPP       | D10   | Power        | High voltage supply for programming OTPM. | Leave unconnected.  |
| NC        | A1, D1  |              | No connect.                               |   |

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Top View  
(Ball Down)

**Figure 8. 8 x 7 mm, 89-Ball iBGA Package**

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**Table 5. PIN DESCRIPTIONS, 9 x 9 mm, 80-BALL iBGA**

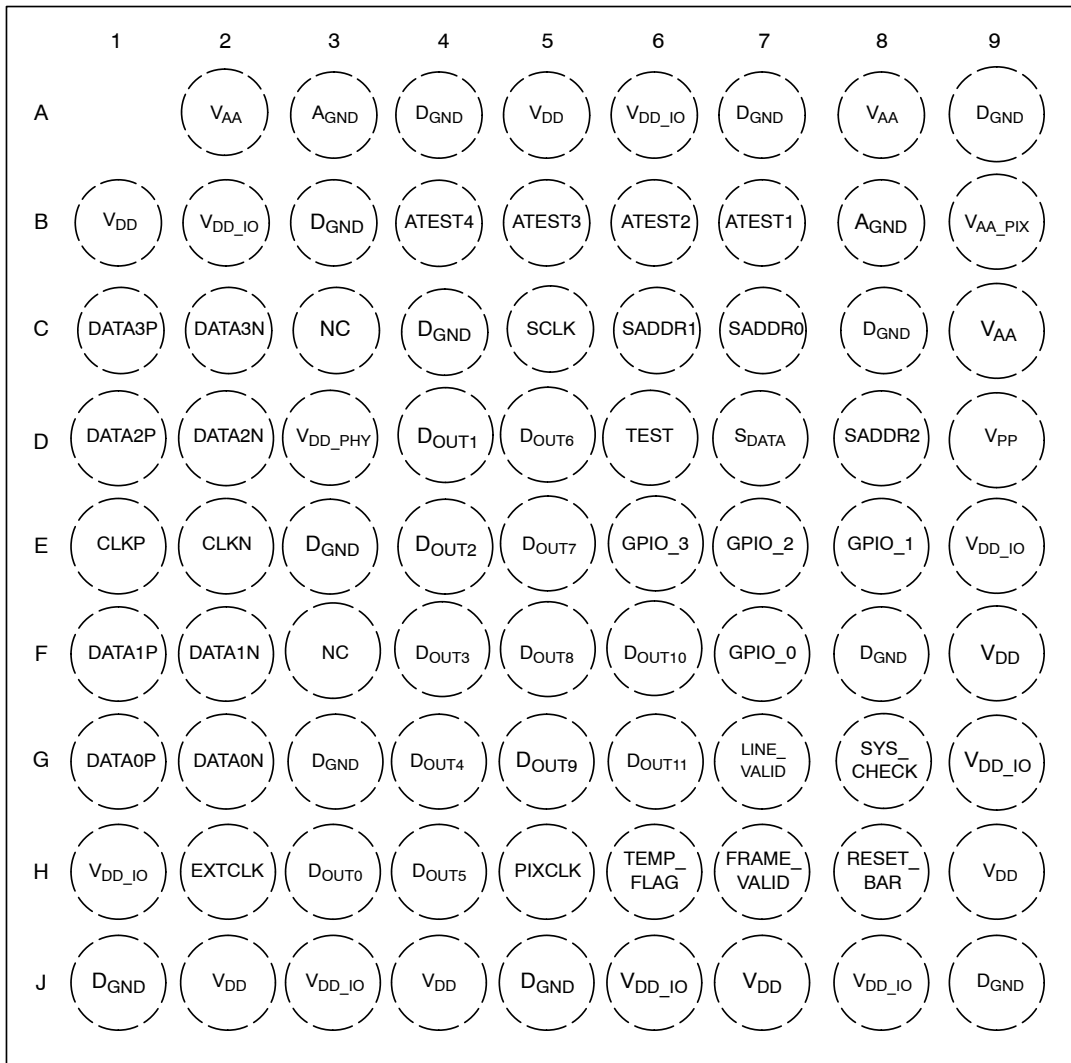
| Pin Name    | iBGA Pin | Type         | Description   | Comments  |
|-------------|----------|--------------|---|---|
| EXTCLK      | H2       | Input        | Master input clock. PLL input clock.  | Connect to clock source. Min and Max frequency depends upon output port and clocking method.  |
| RESET_BAR   | H8       | Input        | Asynchronous active-low reset.  | Connect to host.  |
| SCLK        | C5       | Input        | CCI clock for access to control and status registers  | Connect to host.  |
| SDATA       | D7       | Input/Output | CCI data for reads from and writes to control and status registers  | Connect to host.  |
| SADDR0      | C7       | Input        | CCI interface device address select bit 0.  | Selects CCI address. 000b sets the address to 0x20/0x21. 001b sets the address to 0x30/0x31. Connect to VDD_IO or DGND accordingly. |
| SADDR1      | C6       | Input        | CCI interface device address select bit 1.  |   |
| SADDR2      | D8       | Input        | CCI interface device address select bit 2.  |   |
| PIXCLK      | H5       | Output       | Parallel data output pixel clock. Used to qualify the LINE_VALID, FRAME_VALID, and DOUT11 to DOUT0 outputs. | Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12-bit parallel configuration.                     |
| FRAME_VALID | H7       | Output       | Parallel data output FRAME_VALID output. Qualified by PIXCLK.   |   |
| LINE_VALID  | G7       | Output       | Parallel data output LINE_VALID output. Qualified by PIXCLK.  |   |
| DOUT11      | G6       | Output       | Parallel data output pixel data bit 11. Qualified by PIXCLK.  | Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12-bit parallel configuration.                     |
| DOUT10      | F6       | Output       | Parallel data output pixel data bit 10. Qualified by PIXCLK.  |   |
| DOUT9       | G5       | Output       | Parallel data output pixel data bit 9. Qualified by PIXCLK.   |   |
| DOUT8       | F5       | Output       | Parallel data output pixel data bit 8. Qualified by PIXCLK.   |   |
| DOUT7       | E5       | Output       | Parallel data output pixel data bit 7. Qualified by PIXCLK.   |   |
| DOUT6       | D5       | Output       | Parallel data output pixel data bit 6. Qualified by PIXCLK.   |   |
| DOUT5       | H4       | Output       | Parallel data output pixel data bit 5. Qualified by PIXCLK.   |   |
| DOUT4       | G4       | Output       | Parallel data output pixel data bit 4. Qualified by PIXCLK.   |   |
| DOUT3       | F4       | Output       | Parallel data output pixel data bit 3. Qualified by PIXCLK.   |   |
| DOUT2       | E4       | Output       | Parallel data output pixel data bit 2. Qualified by PIXCLK.   |   |
| DOUT1       | D4       | Output       | Parallel data output pixel data bit 1. Qualified by PIXCLK.   |   |
| DOUT0       | H3       | Output       | Parallel data output pixel data bit 0. Qualified by PIXCLK.   |   |

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**Table 5. PIN DESCRIPTIONS, 9 x 9 mm, 80-BALL iBGA**

| Pin Name  | iBGA Pin                                       | Type             | Description                               | Comments  |
|-----------|--|------------------|---|---|
| CLKP      | E1   | Output           | Differential Mipi serial clock            | Connect to host/receiver or can be left floating if not used. Use DATA0 for 1 lane configuration or DATA0 and DATA1 for 2 lane configuration. |
| CLKN      | E2   | Output           | Differential Mipi serial clock            |   |
| DATA3P    | C1   | Output           | Differential Mipi serial data lane 3.     |   |
| DATA3N    | C2   | Output           | Differential Mipi serial data lane 3.     |   |
| DATA2P    | D1   | Output           | Differential Mipi serial data lane 2.     |   |
| DATA2N    | D2   | Output           | Differential Mipi serial data lane 2.     |   |
| DATA1P    | F1   | Output           | Differential Mipi serial data lane 1.     |   |
| DATA1N    | F2   | Output           | Differential Mipi serial data lane 1.     |   |
| DATA0P    | G1   | Output           | Differential Mipi serial data lane 0.     |   |
| DATA0N    | G2   | Output           | Differential Mipi serial data lane 0.     |   |
| TEST      | D6   | Input            | Enable manufacturing test modes.          | Tie to DGND.  |
| ATEST1    | B7   | Input/<br>Output | Analog manufacturing test access          | Leave unconnected.  |
| ATEST2    | B6   | Input/<br>Output | Analog manufacturing test access          |   |
| ATEST3    | B5   | Input/<br>Output | Analog manufacturing test access          |   |
| ATEST4    | B4   | Input/<br>Output | Analog manufacturing test access          |   |
| GPIO_0    | F7   | Input/<br>Output | GPIO Pin 0                                | GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.  |
| GPIO_1    | E8   | Input/<br>Output | GPIO Pin 1                                |   |
| GPIO_2    | E7   | Input/<br>Output | GPIO Pin 2                                |   |
| GPIO_3    | E6   | Input/<br>Output | GPIO Pin 3                                |   |
| SYS_CHECK | G8   | Output           | Combined OR of error flags.               | Leave unconnected if not used.  |
| TEMP_FLAG | H6   | Output           | Temperature monitoring flag.              | Open-drain. Leave unconnected if not used.  |
| DGND      | J1, B3, E3, G3, A4, C4, J5, A7, C8, F8, A9, J9 | Power            | Digital ground.                           |   |
| VDD       | B1, J2, J4, A5, J7, F9, H9                     | Power            | Core digital power.                       |   |
| VDD_PHY   | D3   | Power            | PHY digital power.                        | Connect to VDD.   |
| VDD_IO    | H1, B2, J3, A6, J6, J8, E9, G9                 | Power            | Digital I/O power.                        |   |
| AGND      | A3, B8   | Power            | Analog ground.                            |   |
| VAA       | A2, A8, C9                                     | Power            | Analog power.                             |   |
| VAA_PIX   | B9   | Power            | Analog pixel array power.                 | Connect to VAA.   |
| VPP       | D9   | Power            | High voltage supply for programming OTPM. | Leave unconnected.  |
| NC        | A1, C3, F3                                     |                  | No connect.                               |   |

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Top View  
(Ball Down)

**Figure 9. 9 x 9 mm 80-Ball iBGA Package**

## TWO-WIRE SERIAL REGISTER INTERFACE

The two-wire serial interface bus enables read/write access to control and status registers within the AR0147AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD\_IO off-chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR0147AT uses SCLK as an input only and therefore never drives it LOW.

### Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

10. A (repeated) start condition
11. A slave address/data direction byte
12. An (a no) acknowledge bit
13. A message byte
14. A stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

### Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

### Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

### Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

### Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit

[0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0147AT are 0x20(write address) and 0x21 (read address) in accordance with the specification. An additional 7 alternate slave address can be selected by enabling and asserting the SADDR [2:0] inputs.

### Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

### Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

### No Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

### Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

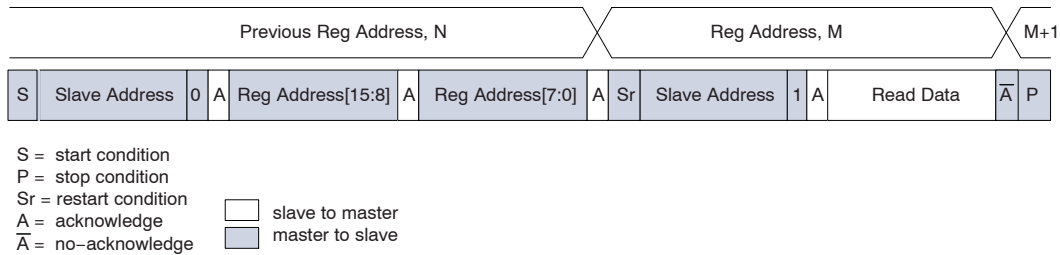
If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.



**Single READ from Random Location**

This sequence (Figure 10) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of

register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 10 shows how the internal register address maintained by the AR0147AT is loaded and incremented as the sequence proceeds.

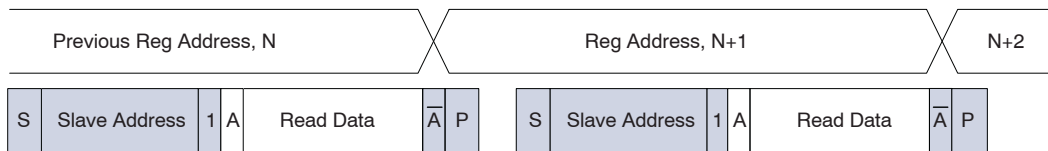


**Figure 10. Single READ from Random Location**

**Single READ from Current Location**

This sequence (Figure 11) performs a read using the current value of the AR0147AT internal register address.

The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

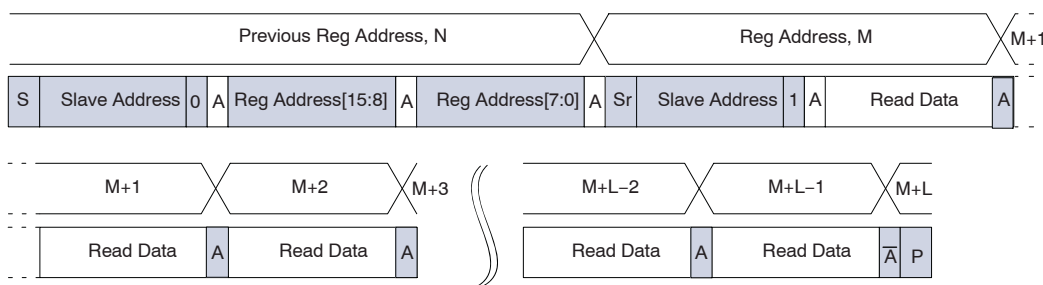


**Figure 11. Single READ from Current Location**

**Sequential READ, Start from Random Location**

This sequence (Figure 12) starts in the same way as the single READ from random location (Figure 10). Instead of generating a no-acknowledge bit after the first byte of data

has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

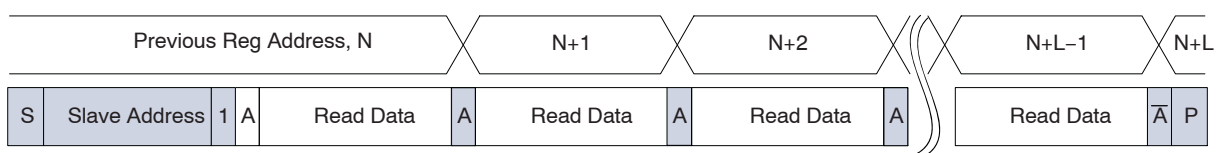


**Figure 12. Sequential READ, Start from Random Location**

**Sequential READ, Start from Current Location**

This sequence (Figure 13) starts in the same way as the single READ from current location (Figure 11). Instead of generating a no-acknowledge bit after the first byte of data

has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

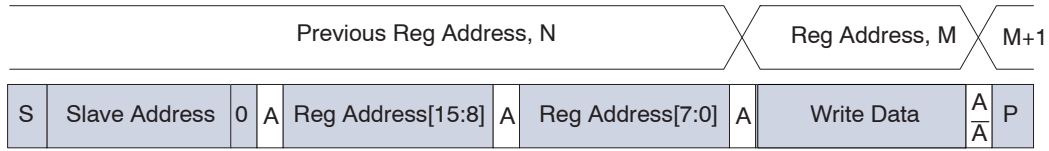


**Figure 13. Sequential READ, Start from Current Location**

**Single WRITE to Random Location**

This sequence (Figure 14) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH

then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

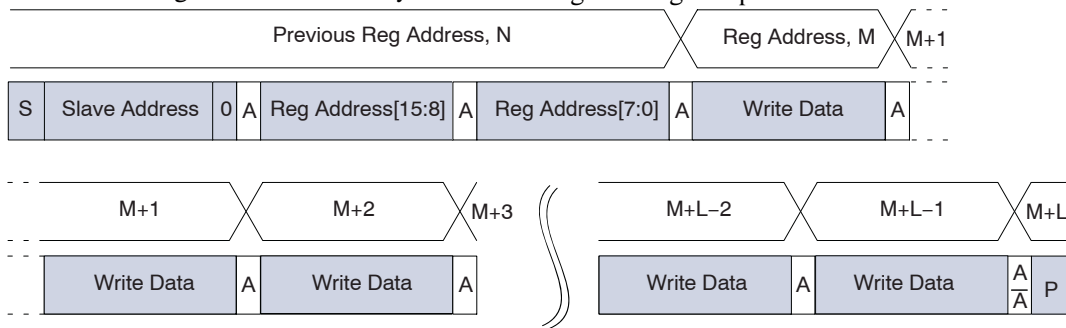


**Figure 14. Single WRITE to Random Location**

**Sequential WRITE, Start at Random Location**

This sequence (Figure 15) starts in the same way as the single WRITE to random location (Figure 14). Instead of generating a no-acknowledge bit after the first byte of data

has been transferred, the master generates an acknowledge bit and continues to perform byte WRITES until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.



**Figure 15. Sequential WRITE, Start at Random Location**

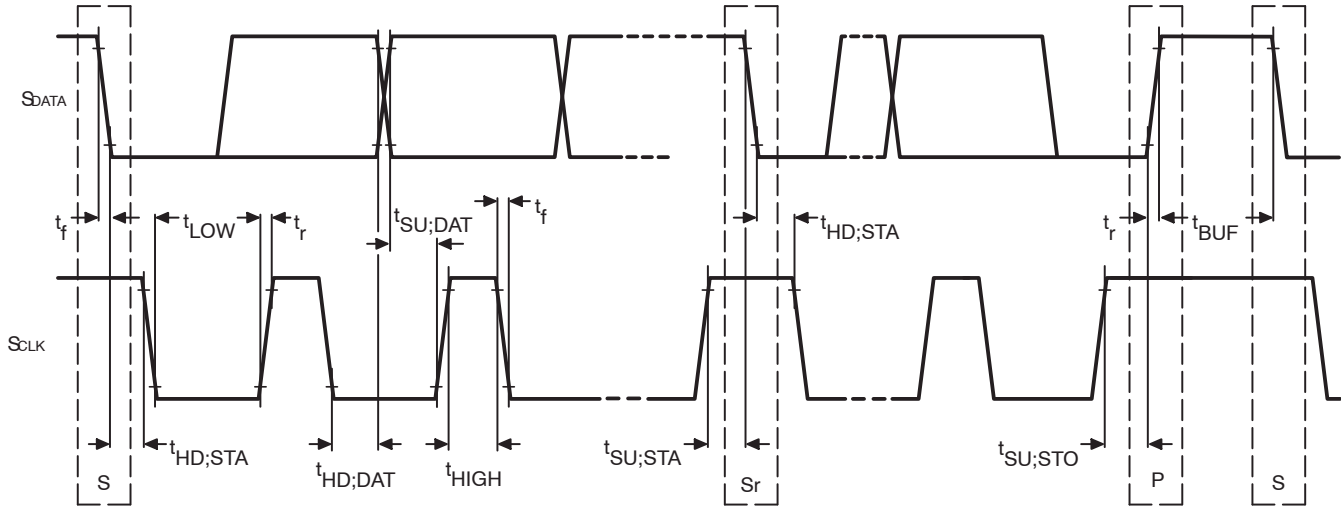
## ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply to the following conditions:

EXTCLK = 27 MHz;  $V_{AA} = 2.8$  V;  $V_{AA\_PIX} = 2.8$  V;  
 $V_{DD\_IO} = 1.8$  V;  $V_{DD}$  (digital core) = 1.2 V;  $V_{DD\_PHY} = 1.2$  V; Output load = 68.5 pF;  $T_J = 60^\circ\text{C}$ .

### Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 16 and Table 6.



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

**Figure 16. Two-Wire Serial Bus Timing Parameters**

**Table 6. TWO-WIRE SERIAL BUS CHARACTERISTICS**
 $f_{EXTCLK} = 27 \text{ MHz}$ ;  $V_{DD} = V_{DD\_PHY} = 1.2 \text{ V}$ ;  $V_{DD\_IO} = V_{AA} = V_{AA\_PIX} = 2.8 \text{ V}$ ;  $T_A = 25^\circ\text{C}$ 

| Parameter   | Symbol         | Standard Mode             |       | Fast Mode                   |      | Fast Mode Plus       |      | Unit          |
|---|----------------|---------------------------|-------|-----------------------------|------|----------------------|------|---------------|
|   |                | Min                       | Max   | Min                         | Max  | Min                  | Max  |               |
| M_SCLK Clock Frequency  | $f_{SCL}$      | 0                         | 100   | 0                           | 400  | 0                    | 1000 | KHz           |
| SCLK High   |                | 8*EXTCLK + SCLK rise time |       | 8*EXTCLK + EXTCLK rise time |      |                      |      | $\mu\text{s}$ |
| SCLK Low  |                | 6*EXTCLK + SCLK rise time |       | 6*EXTCLK + SCLK rise time   |      |                      |      | $\mu\text{s}$ |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD;STA}$   | 4                         | -     | 0.6                         | -    | 0.26                 | -    | $\mu\text{s}$ |
| LOW period of the M_SCLK clock  | $t_{LOW}$      | 4.7                       | -     | 1.2                         | -    | 0.5                  | -    | $\mu\text{s}$ |
| HIGH period of the M_SCLK clock   | $t_{HIGH}$     | 4                         | -     | 0.6                         | -    | 0.26                 | -    | $\mu\text{s}$ |
| Set-up time for a repeated START condition  | $t_{SU;STA}$   | 4.7                       | -     | 0.6                         | -    | 0.26                 | -    | $\mu\text{s}$ |
| Data hold time  | $t_{HD;DAT}$   | 0                         | 3.453 | 0                           | 0.93 | 0                    | -    | $\mu\text{s}$ |
| Data set-up time  | $t_{SU;DAT}$   | 250                       | -     | 100                         | -    | 50                   | -    | ns            |
| Rise time of both M_SDATA and M_SCLK time (10–90%)  | $t_r$          | -                         | 1000  | 20 + 0.1 Cb (Note 4)        | 300  | 20 + 0.1 Cb (Note 4) | 120  | ns            |
| Fall time of both M_SDATA and M_SCLK time (10–90%)  | $t_f$          | -                         | 300   | 20 + 0.1 Cb (Note 4)        | 300  | 20 + 0.1 Cb (Note 4) | 120  | ns            |
| Set-up time for STOP condition  | $t_{SU;STO}$   | 4                         | -     | 0.6                         | -    | 0.26                 | -    | $\mu\text{s}$ |
| Bus free time between a STOP and START condition  | $t_{BUF}$      | 4.7                       | -     | 1.3                         | -    | 0.5                  | -    | $\mu\text{s}$ |
| Capacitive load for each bus line   | Cb             | -                         | 400   | -                           | 400  | -                    | 500  | pF            |
| Serial interface input pin capacitance  | $C_{IN\_SI}$   | -                         | 3.3   | -                           | 3.3  | -                    | 3.3  | pF            |
| M_SDATA max load capacitance  | $C_{LOAD\_SD}$ | -                         | 30    | -                           | 30   | -                    | 30   | pF            |
| M_SDATA pull-up resistor  | $R_{SD}$       | 1.5                       | 4.7   | 1.5                         | 4.7  | 1.5                  | 4.7  | k $\Omega$    |

4. This table is based on I<sup>2</sup>C standard (v2.1 January 2000). Philips Semiconductor.

5. Two-wire control is I<sup>2</sup>C compatible.

6. All values referred to  $V_{IHmin} = 0.9 V_{DD\_IO}$  and  $V_{ILmax} = 0.1 V_{DD\_IO}$  levels. Sensor EXCLK = 27 MHz.

7. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK. The two-wire standard specifies a minimum rise and fall time for Fast-Mode and Fast-Mode Plus modes of operation. This specification is not a timing requirement that is enforced on ON Semiconductor sensor's as a receiver, because our receivers are designed to work in mixed systems with std-mode where no such minimum rise and fall times are required/specified. However, it's the host's responsibility when using fast edge rates, especially when two-wire slew-rate driver control isn't available, to manage the generated EMI, and the potential voltage undershoot on the sensor receiver circuitry, to avoid activating sensor ESD diodes and current-clamping circuits. This is typically not an issue in most applications, but should be checked if below minimum fall times and rise times are required.

8. The maximum  $t_{HD;DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCLK signal.

9. A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT}$  250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line  $t_r \text{ max} + t_{SU;DAT} = 1000 + 250 = 1250 \text{ ns}$  (according to the Standard-mode I<sup>2</sup>C-bus specification) before the SCLK line is released.

10. Cb = total capacitance of one bus line in pF.

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**Table 7. TWO-WIRE SERIAL REGISTER INTERFACE ELECTRICAL CHARACTERISTICS**

$f_{EXTCLK} = 27\text{MHz}$ ;  $V_{DD} = V_{DD\_PHY} = 1.2\text{V}$ ;  $V_{DD\_IO} = V_{AA} = V_{AA\_PIX} = 2.8\text{V}$ ;  $T_A = 25^\circ\text{C}$

| Parameter          | Symbol   | Condition                                   | Standard Mode    |                  | Fast Mode        |                  | Fast Mode Plus   |                  | Unit |
|--------------------|----------|---|------------------|------------------|------------------|------------------|------------------|------------------|------|
|                    |          |   | Min              | Max              | Min              | Max              | Min              | Max              |      |
| Input HIGH voltage | $V_{IH}$ |   | $0.7 * V_{DDIO}$ | –                | $0.7 * V_{DDIO}$ | –                | $0.7 * V_{DDIO}$ | –                | V    |
| Input LOW voltage  | $V_{IL}$ |   | –                | $0.3 * V_{DDIO}$ | –                | $0.3 * V_{DDIO}$ | –                | $0.3 * V_{DDIO}$ | V    |
| Output LOW voltage | $V_{OL}$ | $V_{DDIO} = (1.7\text{ V} - 1.9\text{ V})$  | –                | 0.4              | –                | 0.4              | –                | 0.4              | V    |
|                    |          | $I_{OL} = 3\text{ mA}$                      |                  |                  |                  |                  |                  |                  |      |
| Output LOW voltage | $V_{OL}$ | $V_{DDIO} = (2.6\text{ V} - 2.94\text{ V})$ | –                | $0.2 * V_{DDIO}$ | –                | $0.2 * V_{DDIO}$ | –                | $0.2 * V_{DDIO}$ | V    |
|                    |          | $I_{OL} = 3\text{ mA}$                      |                  |                  |                  |                  |                  |                  |      |

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## I/O Timing

By default, the AR0147AT launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising

edge of PIXCLK. This can be changed using register R0x3028.

See Figure 17 and Table 8 for I/O timing (AC) characteristics.

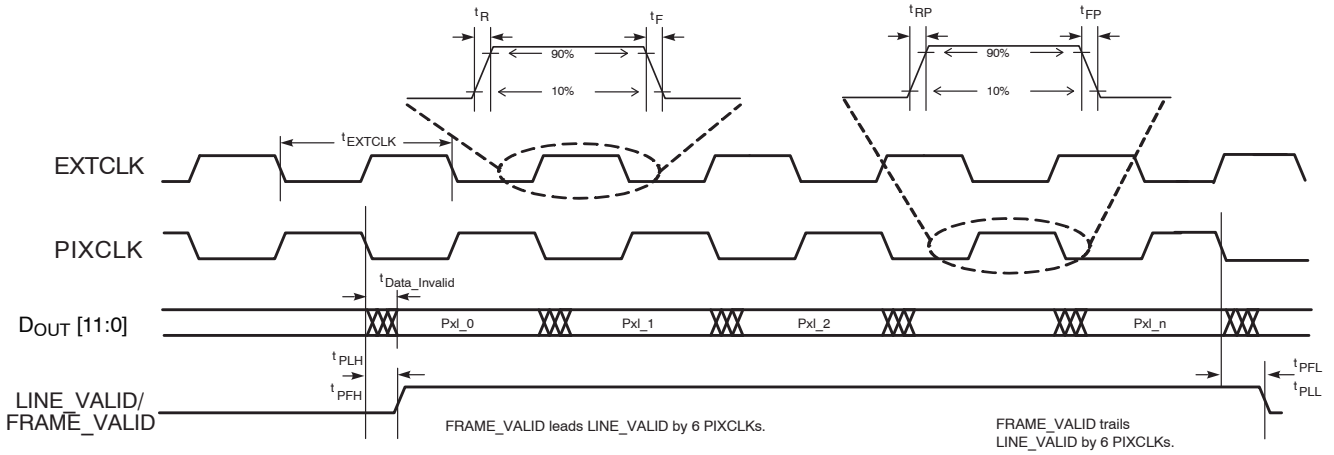


Figure 17. I/O Timing Diagram

The following I/O timing diagram has PIXCLK configured as data valid on rising edge through register R0x3028

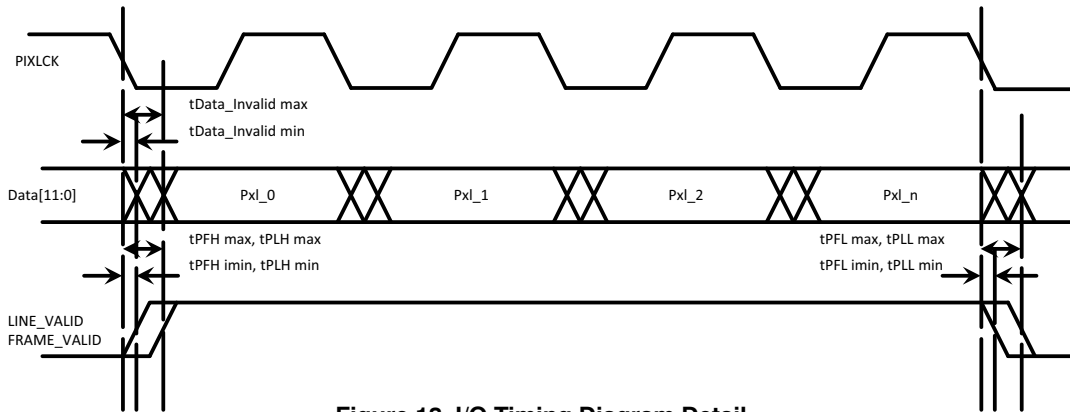


Figure 18. I/O Timing Diagram Detail

Table 8. I/O Timing Characteristics (1.8 V VDD\_IO) (Note 11)

| Symbol        | Definition                   | Condition                                  | Min | Typical | Max              | Unit |
|---------------|------------------------------|--|-----|---------|------------------|------|
| fEXTCLK       | Input clock frequency        | PLL Enabled                                | 12  | --      | 50               | MHz  |
| tEXTCLK       | Input clock period           | PLL Enabled                                | 20  | --      | 83.3             | ns   |
| tR            | Input clock rise time        | PLL Enabled                                | 0.2 | --      | 0.3 *<br>tEXTCLK | ns   |
| tF            | Input clock fall time        | PLL Enabled                                | 0.2 | --      | 0.3 *<br>tEXTCLK | ns   |
| tJITTER       | Input clock jitter           | PLL Enabled                                | --  | --      | 600              | ps   |
| fPIXCLK       | PIXCLK frequency             | Default, Nominal Voltages                  | 12  | --      | 89.2             | MHz  |
|               | Clock duty cycle             | PLL Enabled                                | 40  | 50      | 60               | %    |
| tPIX JITTER   | Jitter on PIXCLK             |  | --  | 1       |                  | ns   |
| tData_Invalid | PIXCLK to data not valid     | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3                | ns   |
| tPFH          | PIXCLK to FV HIGH Transition | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3                | ns   |
| tPLH          | PIXCLK to LV HIGH Transition | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3                | ns   |
| tPFL          | PIXCLK to FV LOW Transition  | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3                | ns   |
| tPLL          | PIXCLK to LV LOW Transition  | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3                | ns   |
| CLOAD         | Output load capacitance      |  | --  | 20      | --               | pF   |
| CIN           | Input pin capacitance        |  | --  | 2.5     | --               | pF   |

11. I/O timing characteristics are measured under the following conditions:

- Minimum and maximum values are taken at 105°C, 1.7 V and -40°C, 1.9 V. All values are taken at the 50% transition point. The loading used is 20 pF.
- Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

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**Table 9. I/O Timing Characteristics (2.8 V VDD\_IO) (Note 12)**

| Symbol        | Definition                   | Condition                                  | Min | Typical | Max         | Unit |
|---------------|------------------------------|--|-----|---------|-------------|------|
| fEXTCLK       | Input clock frequency        | PLL Enabled                                | 12  | --      | 50          | MHz  |
| tEXTCLK       | Input clock period           | PLL Enabled                                | 20  | --      | 83.3        | ns   |
| tR            | Input clock rise time        | PLL Enabled                                | 0.2 | --      | 0.3*tEXTCLK | ns   |
| tF            | Input clock fall time        | PLL Enabled                                | 0.2 | --      | 0.3*tEXTCLK | ns   |
| tJITTER       | Input clock jitter           | PLL Enabled                                | --  | --      | 600         | ps   |
| fPIXCLK       | PIXCLK frequency             | Default, Nominal Voltages                  | 12  | --      | 89.2        | MHz  |
|               | Clock duty cycle             | PLL Enabled                                | 40  | 50      | 60          | %    |
| tPIX JITTER   | Jitter on PIXCLK             |  | --  | 1       |             | ns   |
| tData_Invalid | PIXCLK to data not valid     | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3           | ns   |
| tPFH          | PIXCLK to FV HIGH Transition | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3           | ns   |
| tPLH          | PIXCLK to LV HIGH Transition | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3           | ns   |
| tPFL          | PIXCLK to FV LOW Transition  | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3           | ns   |
| tPLL          | PIXCLK to LV LOW Transition  | PIXCLK slew rate = 7<br>Data slew rate = 7 | 0.1 | --      | 3           | ns   |
| CLOAD         | Output load capacitance      |  | --  | 20 pF   | --          | pF   |
| CIN           | Input pin capacitance        |  | --  | 2.5 pF  | --          | pF   |

12. I/O timing characteristics are measured under the following conditions

- a. Minimum and maximum values are taken at 105°C, 2.6 V and -40°C, 2.94 V. All values are taken at the 50% transition point. The loading used is 20 pF.
- b. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.



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**Table 10. I/O RISE SLEW RATE (2.8 V  $V_{DD\_IO}$ ) (Note 13)**

| Parallel Slew Rate (R0x306E[15:13]) | Conditions | Min  | Typ  | Max  | Unit |
|-------------------------------------|------------|------|------|------|------|
| 7                                   | Default    | 1.19 | 2.46 | 3.79 | V/ns |
| 6                                   | Default    | 1.17 | 2.44 | 3.75 | V/ns |
| 5                                   | Default    | 1.15 | 2.43 | 3.7  | V/ns |
| 4                                   | Default    | 1.14 | 2.42 | 3.67 | V/ns |
| 3                                   | Default    | 1.12 | 2.40 | 3.62 | V/ns |
| 2                                   | Default    | 0.93 | 2.03 | 3.08 | V/ns |
| 1                                   | Default    | 0.72 | 1.60 | 2.43 | V/ns |
| 0                                   | Default    | 0.46 | 1.07 | 1.64 | V/ns |

13.20 pF loads at nominal voltages.

**Table 11. I/O FALL SLEW RATE (2.8 V  $V_{DD\_IO}$ ) (Note 14)**

| Parallel Slew Rate (R0x306E[15:13]) | Conditions | Min  | Typ  | Max  | Unit |
|-------------------------------------|------------|------|------|------|------|
| 7                                   | Default    | 1.40 | 2.85 | 4.33 | V/ns |
| 6                                   | Default    | 1.32 | 2.72 | 4.12 | V/ns |
| 5                                   | Default    | 1.25 | 2.59 | 3.89 | V/ns |
| 4                                   | Default    | 1.16 | 2.44 | 3.63 | V/ns |
| 3                                   | Default    | 1.07 | 2.28 | 3.35 | V/ns |
| 2                                   | Default    | 0.87 | 1.88 | 2.75 | V/ns |
| 1                                   | Default    | 0.66 | 1.44 | 2.08 | V/ns |
| 0                                   | Default    | 0.41 | 0.91 | 1.32 | V/ns |

14.20 pF loads at nominal voltages.

**Table 12. I/O RISE SLEW RATE (1.8 V  $V_{DD\_IO}$ ) (Note 15)**

| Parallel Slew Rate (R0x306E[15:13]) | Conditions | Min  | Typ  | Max  | Unit |
|-------------------------------------|------------|------|------|------|------|
| 7                                   | Default    | 0.6  | 1.06 | 1.73 | V/ns |
| 6                                   | Default    | 0.59 | 1.05 | 1.71 | V/ns |
| 5                                   | Default    | 0.58 | 1.04 | 1.7  | V/ns |
| 4                                   | Default    | 0.58 | 1.03 | 1.68 | V/ns |
| 3                                   | Default    | 0.56 | 1.02 | 1.66 | V/ns |
| 2                                   | Default    | 0.47 | 0.85 | 1.39 | V/ns |
| 1                                   | Default    | 0.36 | 0.67 | 1.09 | V/ns |
| 0                                   | Default    | 0.26 | 0.44 | 0.66 | V/ns |

15.20 pF loads at nominal voltages.

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**Table 13. I/O FALL SLEW RATE (1.8 V  $V_{DD\_IO}$ ) (Note 16)**

| Parallel Slew Rate (R0x306E[15:13]) | Conditions | Min  | Typ  | Max  | Unit |
|-------------------------------------|------------|------|------|------|------|
| 7                                   | Default    | 0.71 | 1.27 | 2.04 | V/ns |
| 6                                   | Default    | 0.67 | 1.20 | 1.93 | V/ns |
| 5                                   | Default    | 0.64 | 1.14 | 1.83 | V/ns |
| 4                                   | Default    | 0.60 | 1.08 | 1.72 | V/ns |
| 3                                   | Default    | 0.55 | 0.99 | 1.58 | V/ns |
| 2                                   | Default    | 0.46 | 0.83 | 1.32 | V/ns |
| 1                                   | Default    | 0.35 | 0.65 | 1.02 | V/ns |
| 0                                   | Default    | 0.27 | 0.41 | 0.72 | V/ns |

16.20 pF loads at nominal voltages.

The DC electrical characteristics are shown in the tables below.

**Table 14. DC ELECTRICAL CHARACTERISTICS**

| Symbol          | Definition            | Condition                                    | Min         | Typ     | Max         | Unit |
|-----------------|-----------------------|--|-------------|---------|-------------|------|
| VDD             | Core digital voltage  |  | 1.14        | 1.2     | 1.26        | V    |
| VDD_IO          | I/O digital voltage   |  | 1.7/2.60    | 1.8/2.8 | 1.9/2.94    | V    |
| VAA             | Analog voltage        |  | 2.60        | 2.8     | 2.94        | V    |
| VAA_PIX         | Pixel supply voltage  |  | 2.60        | 2.8     | 2.94        | V    |
| VDD_PHY         | PHY supply voltage    |  | 1.14        | 1.2     | 1.26        | V    |
| V <sub>IH</sub> | Input HIGH voltage    |  | 0.7 x VDDIO | –       | VDDIO + 0.3 | V    |
| V <sub>IL</sub> | Input LOW voltage     |  | –0.3        | –       | 0.3 x VDDIO | V    |
| I <sub>IN</sub> | Input leakage current | No pull-up resistor:<br>VIN = VDD_IO or DGND | –           | –       | 20          | μA   |
| V <sub>OH</sub> | Output HIGH voltage   |  | 0.8 x VDDIO | –       | –           | V    |
| V <sub>OL</sub> | Output LOW voltage    |  | –           | –       | 0.2 x VDDIO | V    |
| I <sub>OH</sub> | Output HIGH current   | At specified VDDIO=1.8 V;<br>Vpadd=VDDIO–0.4 | 20          | –       | –           | mA   |
| I <sub>OL</sub> | Output LOW current    | At specified VDDIO=1.8 V;<br>Vpadd=VDDIO–0.4 | –           | –       | 45          | mA   |

17. VAA\_PIX must always be equal to VAA.

18. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 15. ABSOLUTE MAXIMUM RATINGS**

| Symbol      | Parameter                | Min  | Max         | Unit |
|-------------|--------------------------|------|-------------|------|
| Vsupply_2V8 | Power supply voltage 2V8 | –0.3 | 3.6         | V    |
| Vsupply_1V8 | Power supply voltage 1V8 | –0.3 | 2.7         | V    |
| Vsupply_1V2 | Power supply voltage 1V2 | –0.3 | 1.6         | V    |
| Isupply_2V8 | Power supply current 2V8 | –0.3 | 167         | mA   |
| Isupply_1V8 | Power supply current 1V8 | –    | 167         | mA   |
| Isupply_1V2 | Power supply current 1V2 | –    | 374         | mA   |
| Ignd        | Total ground current     | –    | 540         | mA   |
| Vin         | DC input voltage         | –0.3 | VDD_IO +0.3 | V    |
| Vout        | DC output voltage        | –0.3 | VDD_IO +0.3 | V    |
| Tstg        | Storage temperature      | –40  | 150         | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

19. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

20. 125°C is applied for reliability testing as maximum storage temperature.

21. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

**Table 16. OPERATING CURRENT CONSUMPTION IN PARALLEL 12-BIT LINEAR 30FPS**

| Current Type                  | Condition                 | Symbol              | Voltage | Min | Typ<br>(Note 24) | Max<br>(Note 25) | Unit |
|-------------------------------|---------------------------|---------------------|---------|-----|------------------|------------------|------|
| Analog Operating Current      | Streaming Full Res, 30fps | I <sub>AA</sub>     | 2.8     | --  | 39               | 50               | mA   |
| Pixel Supply Current          | Streaming Full Res, 30fps | I <sub>AA_PIX</sub> | 2.8     | --  | 3                | 10               | mA   |
| PHY Supply Current            | Streaming Full Res, 30fps | I <sub>DD_PHY</sub> | 1.2     | --  | 0                | 10               | mA   |
| Digital Operating Current     | Streaming Full Res, 30fps | I <sub>DD</sub>     | 1.2     | --  | 25               | 30               | mA   |
| I/O Digital Operating Current | Streaming Full Res, 30fps | I <sub>DD_IO</sub>  | 1.8     | --  | 8                | 10               | mA   |

22. VAA and VAA\_PIX are tied together

23. PLL enabled and PIXCLK set to 50 MHz

24. T<sub>J</sub> = 55°C25. T<sub>J</sub> = 125°C26. C<sub>LOAD</sub> = 20 pF**Table 17. OPERATING CURRENT CONSUMPTION IN PARALLEL 12-BIT 3-EXPOSURE HDR 30FPS**

| Current Type                  | Condition                 | Symbol              | Voltage | Min | Typ<br>(Note 28) | Max<br>(Note 29) | Unit |
|-------------------------------|---------------------------|---------------------|---------|-----|------------------|------------------|------|
| Analog Operating Current      | Streaming Full Res, 30fps | I <sub>AA</sub>     | 2.8     | --  | 60               | 70               | mA   |
| Pixel Supply Current          | Streaming Full Res, 30fps | I <sub>AA_PIX</sub> | 2.8     | --  | 8                | 10               | mA   |
| PHY Supply Current            | Streaming Full Res, 30fps | I <sub>DD_PHY</sub> | 1.2     | --  | 0                | 10               | mA   |
| Digital Operating Current     | Streaming Full Res, 30fps | I <sub>DD</sub>     | 1.2     | --  | 44               | 50               | mA   |
| I/O Digital Operating Current | Streaming Full Res, 30fps | I <sub>DD_IO</sub>  | 1.8     | --  | 8                | 10               | mA   |

27. VAA and VAA\_PIX are tied together

28. PLL enabled and PIXCLK set to 50 MHz

29. T<sub>J</sub> = 55°C30. T<sub>J</sub> = 125°C31. C<sub>LOAD</sub> = 20 pF**Table 18. OPERATING CURRENT CONSUMPTION IN MIPI 4-LANE 12-BIT 3-EXPOSURE HDR 30FPS**

| Current Type                  | Condition                 | Symbol              | Voltage | Min | Typ<br>(Note 34) | Max<br>(Note 35) | Unit |
|-------------------------------|---------------------------|---------------------|---------|-----|------------------|------------------|------|
| Analog Operating Current      | Streaming Full Res, 30fps | I <sub>AA</sub>     | 2.8     | --  | 60               | 70               | mA   |
| Pixel Supply Current          | Streaming Full Res, 30fps | I <sub>AA_PIX</sub> | 2.8     | --  | 8                | 10               | mA   |
| PHY Supply Current            | Streaming Full Res, 30fps | I <sub>DD_PHY</sub> | 1.2     | --  | 7                | 10               | mA   |
| Digital Operating Current     | Streaming Full Res, 30fps | I <sub>DD</sub>     | 1.2     | --  | 44               | 50               | mA   |
| I/O Digital Operating Current | Streaming Full Res, 30fps | I <sub>DD_IO</sub>  | 1.8     | --  | 1                | 5                | mA   |

32. VAA and VAA\_PIX are tied together

33. PLL enabled and PIXCLK set to 50 MHz

34. T<sub>J</sub> = 55°C35. T<sub>J</sub> = 125°C36. C<sub>LOAD</sub> = 20 pF

**Table 19. OPERATING CURRENT CONSUMPTION IN PARALLEL 12-BIT SUPER-EXPOSURE+T2 30FPS**

| Current Type                  | Condition                 | Symbol              | Voltage | Min | Typ<br>(Note 39) | Max<br>(Note 40) | Unit |
|-------------------------------|---------------------------|---------------------|---------|-----|------------------|------------------|------|
| Analog Operating Current      | Streaming Full Res, 30fps | I <sub>AA</sub>     | 2.8     | --  | 56               | 70               | mA   |
| Pixel Supply Current          | Streaming Full Res, 30fps | I <sub>AA_PIX</sub> | 2.8     | --  | 9                | 10               | mA   |
| PHY Supply Current            | Streaming Full Res, 30fps | I <sub>DD_PHY</sub> | 1.2     | --  | 0                | 10               | mA   |
| Digital Operating Current     | Streaming Full Res, 30fps | I <sub>DD</sub>     | 1.2     | --  | 31               | 40               | mA   |
| I/O Digital Operating Current | Streaming Full Res, 30fps | I <sub>DD_IO</sub>  | 1.8     | --  | 4                | 10               | mA   |

37. VAA and VAA\_PIX are tied together

38. PLL enabled and PIXCLK set to 56 MHz

39. T<sub>J</sub> = 55°C40. T<sub>J</sub> = 125°C41. C<sub>LOAD</sub> = 20 pF**Table 20. OPERATING CURRENT CONSUMPTION IN MIPI 4-LANE 12-bit SUPER-EXPOSURE+T2 30FPS**

| Current Type                  | Condition                 | Symbol              | Voltage | Min | Typ<br>(Note 44) | Max<br>(Note 45) | Unit |
|-------------------------------|---------------------------|---------------------|---------|-----|------------------|------------------|------|
| Analog Operating Current      | Streaming Full Res, 30fps | I <sub>AA</sub>     | 2.8     | --  | 56               | 70               | mA   |
| Pixel Supply Current          | Streaming Full Res, 30fps | I <sub>AA_PIX</sub> | 2.8     | --  | 9                | 10               | mA   |
| PHY Supply Current            | Streaming Full Res, 30fps | I <sub>DD_PHY</sub> | 1.2     | --  | 3                | 10               | mA   |
| Digital Operating Current     | Streaming Full Res, 30fps | I <sub>DD</sub>     | 1.2     | --  | 31               | 40               | mA   |
| I/O Digital Operating Current | Streaming Full Res, 30fps | I <sub>DD_IO</sub>  | 1.8     | --  | 1                | 5                | mA   |

42. VAA and VAA\_PIX are tied together

43. PLL enabled and PIXCLK set to 56 MHz

44. T<sub>J</sub> = 55°C45. T<sub>J</sub> = 125°C46. C<sub>LOAD</sub> = 20 pF**Table 21. OPERATING CURRENT CONSUMPTION IN MIPI 4-LANE 12-BIT 3-EXPOSURE HDR 60FPS**

| Current Type                  | Condition                 | Symbol              | Voltage | Min | Typ<br>(Note 49) | Max<br>(Note 50) | Unit |
|-------------------------------|---------------------------|---------------------|---------|-----|------------------|------------------|------|
| Analog Operating Current      | Streaming Full Res, 60fps | I <sub>AA</sub>     | 2.8     | --  | 70               | 78               | mA   |
| Pixel Supply Current          | Streaming Full Res, 60fps | I <sub>AA_PIX</sub> | 2.8     | --  | 9                | 10               | mA   |
| PHY Supply Current            | Streaming Full Res, 60fps | I <sub>DD_PHY</sub> | 1.2     | --  | 11               | 12               | mA   |
| Digital Operating Current     | Streaming Full Res, 60fps | I <sub>DD</sub>     | 1.2     | --  | 66               | 80               | mA   |
| I/O Digital Operating Current | Streaming Full Res, 60fps | I <sub>DD_IO</sub>  | 1.8     | --  | 0                | 1                | mA   |

47. VAA and VAA\_PIX are tied together

48. PLL enabled and PIXCLK set to 50 MHz

49. T<sub>J</sub> = 55°C50. T<sub>J</sub> = 125°C51. C<sub>LOAD</sub> = 20 pF**Table 22. OPERATING CURRENT CONSUMPTION IN PARALLEL 12-BIT SUPER EXPOSURE 30FPS**

| Current Type             | Condition                 | Symbol              | Voltage | Min | Typ<br>(Note 52) | Max<br>(Note 53) | Unit |
|--------------------------|---------------------------|---------------------|---------|-----|------------------|------------------|------|
| Analog Operating Current | Streaming Full Res, 30fps | I <sub>AA</sub>     | 2.8     | --  | 54               | 63               | mA   |
| Pixel Supply Current     | Streaming Full Res, 30fps | I <sub>AA_PIX</sub> | 2.8     | --  | 17               | 20               | mA   |

52. VAA and VAA\_PIX are tied together

53. PLL enabled and PIXCLK set to 50 MHz

54. T<sub>J</sub> = 55°C55. T<sub>J</sub> = 125°C56. C<sub>LOAD</sub> = 20 pF

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**Table 22. OPERATING CURRENT CONSUMPTION IN PARALLEL 12-BIT SUPER EXPOSURE 30FPS**

| Current Type                  | Condition                 | Symbol              | Voltage | Min | Typ (Note 52) | Max (Note 53) | Unit |
|-------------------------------|---------------------------|---------------------|---------|-----|---------------|---------------|------|
| PHY Supply Current            | Streaming Full Res, 30fps | I <sub>DD_PHY</sub> | 1.2     | --  | 0             | 1             | mA   |
| Digital Operating Current     | Streaming Full Res, 30fps | I <sub>DD</sub>     | 1.2     | --  | 46            | 55            | mA   |
| I/O Digital Operating Current | Streaming Full Res, 30fps | I <sub>DD_IO</sub>  | 1.8     | --  | 7             | 11            | mA   |

52. VAA and VAA\_PIX are tied together

53. PLL enabled and PIXCLK set to 50 MHz

54. T<sub>J</sub> = 55°C

55. T<sub>J</sub> = 125°C

56. C<sub>LOAD</sub> = 20 pF

**Table 23. STANDBY CURRENT CONSUMPTION**

| Definition                            | Condition               | Symbol          | Min | Typ  | Max | Unit |
|---------------------------------------|-------------------------|-----------------|-----|------|-----|------|
| Hard standby (clock off)<br>(Note 57) | Analog, 2.8V (Note 58)  | I <sub>AA</sub> |     | 275  |     | μA   |
|                                       | Digital, 1.2V (Note 59) | I <sub>DD</sub> |     | 0.55 |     | mA   |
| Hard standby (clock on)<br>(Note 57)  | Analog, 2.8V (Note 58)  | I <sub>AA</sub> |     | 300  |     | μA   |
|                                       | Digital, 1.2V (Note 59) | I <sub>DD</sub> |     | 0.7  |     | mA   |
| Soft standby (clock off)              | Analog, 2.8V (Note 58)  | I <sub>AA</sub> |     | 275  |     | μA   |
|                                       | Digital, 1.2V (Note 59) | I <sub>DD</sub> |     | 0.55 |     | mA   |
| Soft standby (clock on)               | Analog, 2.8V (Note 58)  | I <sub>AA</sub> |     | 500  |     | μA   |
|                                       | Digital, 1.2V (Note 59) | I <sub>DD</sub> |     | 2    |     | mA   |

57. Hard standby is set when RESET\_BAR = 0.

58. Analog = VAA + VAA\_PIX.

59. Digital = VDD + VDD\_PHY

60. T<sub>A</sub> = 55°C.

## MIPI Electrical Specifications

The ON Semiconductor AR0147AT sensor supports four lanes of MIPI data.

Compliant to MIPI standards:

- MIPI Alliance Standard for CSI-2 version 1.0
- MIPI Alliance Standard for D-PHY version 1.1

**Table 24. MIPI HIGH-SPEED TRANSMITTER DC CHARACTERISTICS**

| Symbol                   | Parameter  | Min | Typ | Max  | Unit |
|--------------------------|--|-----|-----|------|------|
| V <sub>OD</sub>          | HS transmit differential voltage   | 140 | –   | 270  | mV   |
| V <sub>CMTX</sub>        | HS transmit static common mode voltage                                     | 150 | –   | 250  | mV   |
| ΔV <sub>OD</sub>         | V <sub>OD</sub> mismatch when output is Differential-1 or Differential-0   | –   | –   | 14   | mV   |
| ΔV <sub>CMTX</sub> (1,0) | V <sub>CMTX</sub> mismatch when output is Differential-1 or Differential-0 | –   | –   | 5    | mV   |
| V <sub>OHHS</sub>        | HS output HIGH voltage   | –   | –   | 360  | mV   |
| Z <sub>OS</sub>          | Single-ended output impedance  | 40  | –   | 62.5 | Ω    |
| ΔZ <sub>OS</sub>         | Single-ended output impedance mismatch                                     | –   | –   | 10   | %    |

**Table 25. MIPI HIGH-SPEED TRANSMITTER AC CHARACTERISTICS**

| Symbol            | Parameter        | Min | Typ | Max | Unit |
|-------------------|------------------|-----|-----|-----|------|
|                   | Data bit rate    | –   | –   | 600 | Mb/s |
| t <sub>rise</sub> | 20–80% rise time | 150 | –   | 500 | ps   |
| t <sub>fall</sub> | 20–80% fall time | 150 | –   | 500 | ps   |

**Table 26. MIPI LOW-POWER TRANSMITTER DC CHARACTERISTICS**

| Symbol          | Parameter                 | Min | Typ | Max | Unit |
|-----------------|---------------------------|-----|-----|-----|------|
| V <sub>OL</sub> | Thevenin output low level | –   | –   | 50  | mV   |

**Table 26. MIPI LOW-POWER TRANSMITTER DC CHARACTERISTICS**

|      |                                    |     |      |     |   |
|------|------------------------------------|-----|------|-----|---|
| VOH  | Thevenin output high level         | 1.1 | 1.15 | 1.3 | V |
| ZOLP | Output impedance of LP transmitter | 110 | –    | –   | Ω |

**Table 27. MIPI LOW-POWER TRANSMITTER AC CHARACTERISTICS**

| Symbol            | Parameter                  | Min | Typ | Max | Unit  |
|-------------------|----------------------------|-----|-----|-----|-------|
| t <sub>rise</sub> | 15–85% rise time           | –   | –   | 25  | ns    |
| t <sub>fall</sub> | 15–85% fall time           | –   | –   | 25  | ns    |
| Slew              | Slew rate (CLOAD 5–20 pf)  | –   | –   | 250 | mV/ns |
| Slew              | Slew rate (CLOAD 20–70 pf) | –   | –   | 150 | mV/ns |

### Power Up/Down Timing

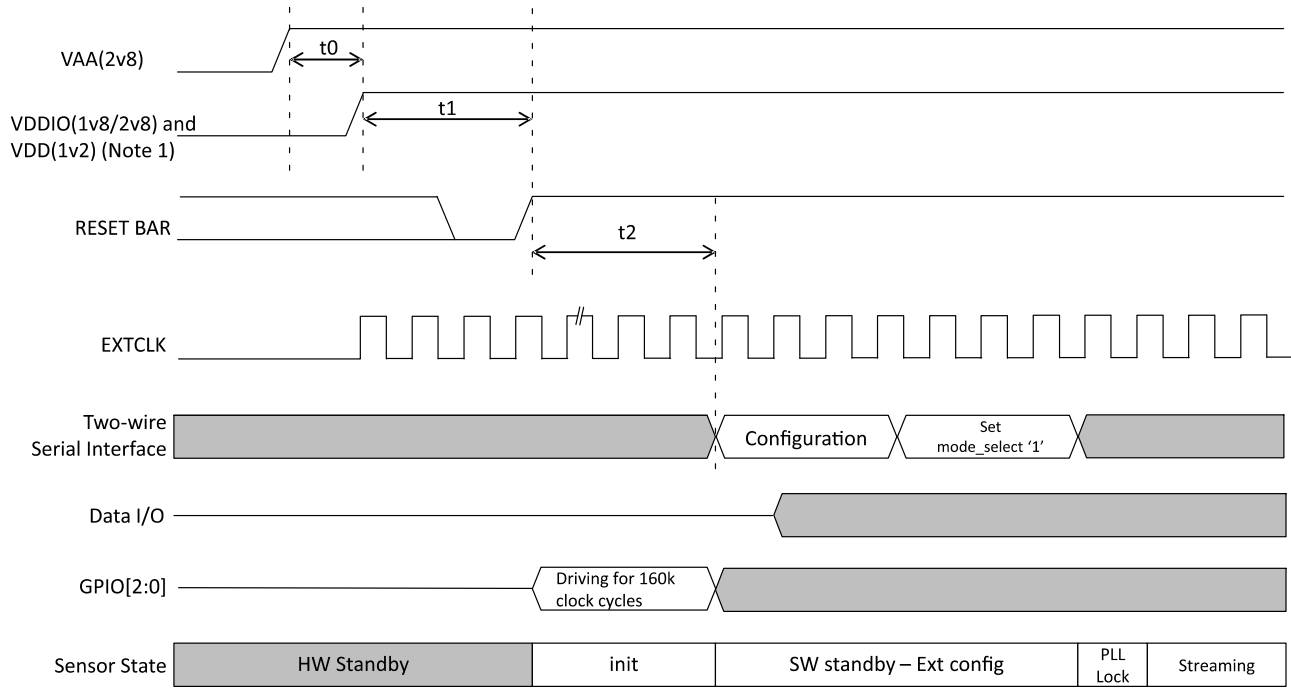
#### Power Up

For controlled power up, RESET\_BAR pin must be asserted (low) before supplies can be sequenced up. Once all supplies are valid, RESET\_BAR is de-asserted (high), the part will begin boot-up on EXTCLK.

Typical Power Up Sequence:

1. Set RESET\_BAR low. The EXTCLK may be applied at any time in the sequence.
2. Power on supplies in the prescribed order: VAA first, followed by VDDIO or VDD. VDDIO and VDD can be powered up in any order as long as VAA is powered up first.
3. After 1.0 ms, set RESET\_BAR high.
4. Wait 160000 EXTCLKs for a full OTPM loading.
5. Set STREAMING bit.
6. Wait 1.0 ms for PLL lock.
7. AR0147 enters streaming mode.

Should the VAA and VDDIO/VDD sequence be brought up differently from the recommended sequence, there may be a potential current leakage of around 10 mA from one power rail to the other power rail in the sensor. For example, should VDDIO and VDD both powered up first before VAA supply reaches 1.5 V, then there exist a resistive path such that a leakage current of around 10 mA would exist between VDD and VAA. Also note that in the event that VDDIO supply is up first and before VAA reaches 1.5 V, the existence of the leakage current depends on whether if VDD supply is already up or not. If VDD supply is still low, then, there is no leakage current observed. In summary, if VDDIO/VDD powered up first while VAA remain low, then there exist a resistive path between VDD and VAA such that approximately 10 mA of leakage current will persists until VAA gets to 1.5 V. The leakage current will not pose any reliability concern to the sensor as long as the duration of the leakage current is not more than 250 ms.



1. VDDIO and VDD can be powered up in any order, as long as VAA is powered up first.

**Figure 19. Power Up Sequence**

**Table 28. POWER UP SEQUENCE**

| Definition   | Symbol   | Min    | Max | Unit    |
|--|----------|--------|-----|---------|
| VAA to VDDIO or VDD (Note 61)                                      | t0       | 0      |     | $\mu$ s |
| VDDIO and VDD Supplies Stable to RESET_N                           | t1       | 1.0    |     | ms      |
| Minimum number of EXTCLK cycles prior to the first CCI transaction | t2       | 160000 |     | cycles  |
| PLL lock time  | PLL lock |        | 1.0 | ms      |

61. VDDIO and VDD can be powered up in any order as long as VAA is powered up first.

**Power Down**

For controlled power down, streaming must be first disabled. The RESET\_BAR pin must be asserted (low) before any external supplies are removed. Then the supplies are allowed to be sequenced off in any order.

Typical Power Down Sequence:

1. De-assert Streaming: Set software standby mode (mode\_select = 0) register.
2. Wait till the end of the current frame (or end-of-line if so configured).

3. Set RESET\_BAR = 0. (Hard Standby, low-leakage state)
4. Wait to power-down delay.
5. Power down supplies in the prescribed order: VDDIO and VDD first, followed by VAA. VDDIO and VDD can be powered down in any order as long as VAA is powered down last.



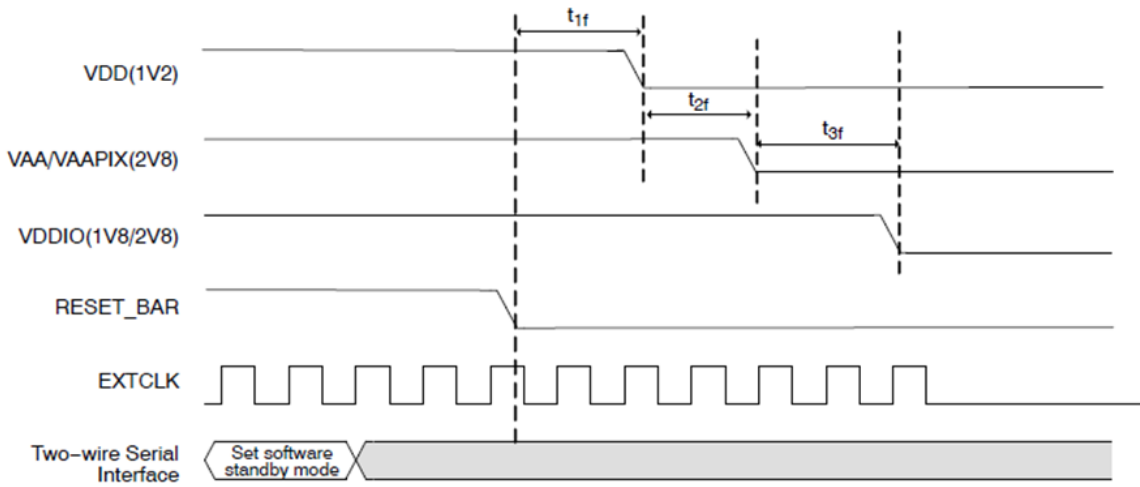


Figure 23. Power Down Sequence

Table 25. POWER DOWN SEQUENCE

| Definition                                      | Symbol | Min | Typ | Max | Unit |
|---|--------|-----|-----|-----|------|
| RESET_BAR falling to any VDD removal [optional] | T1f    | 0   | -   | -   | ms   |
| VDD removal to VAA/VAAPIX removal               | T2f    | 0   | -   | -   | ms   |
| VAA/VAAPIX removal to VDDIO removal             | T3f    | 0   | -   | -   | ms   |

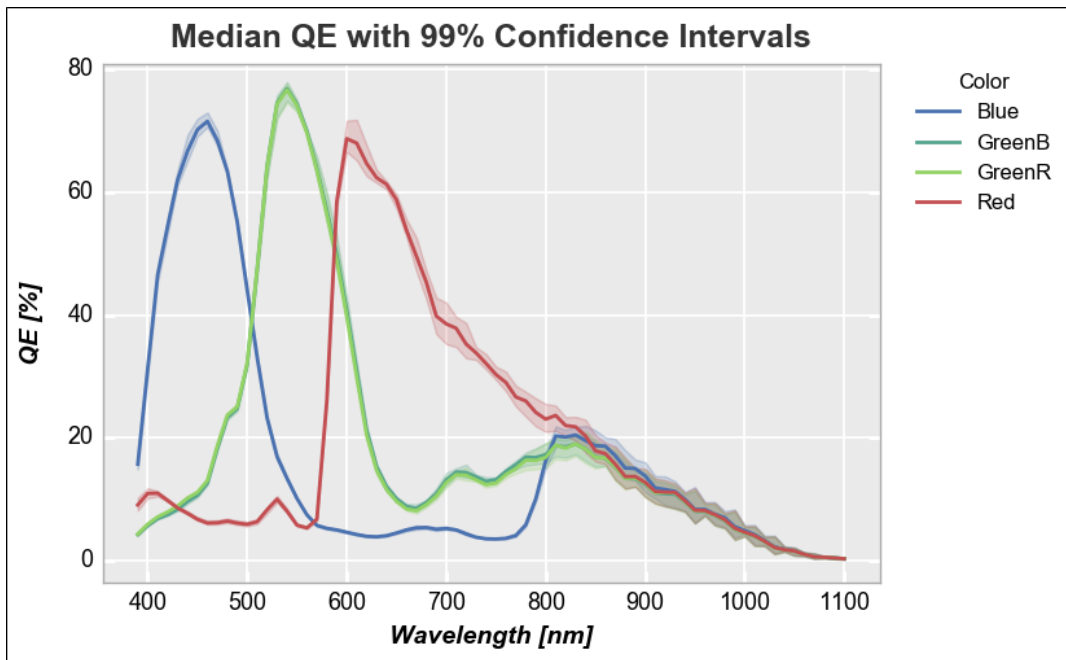


Figure 20. Quantum Efficiency – RGB Bayer Sensor

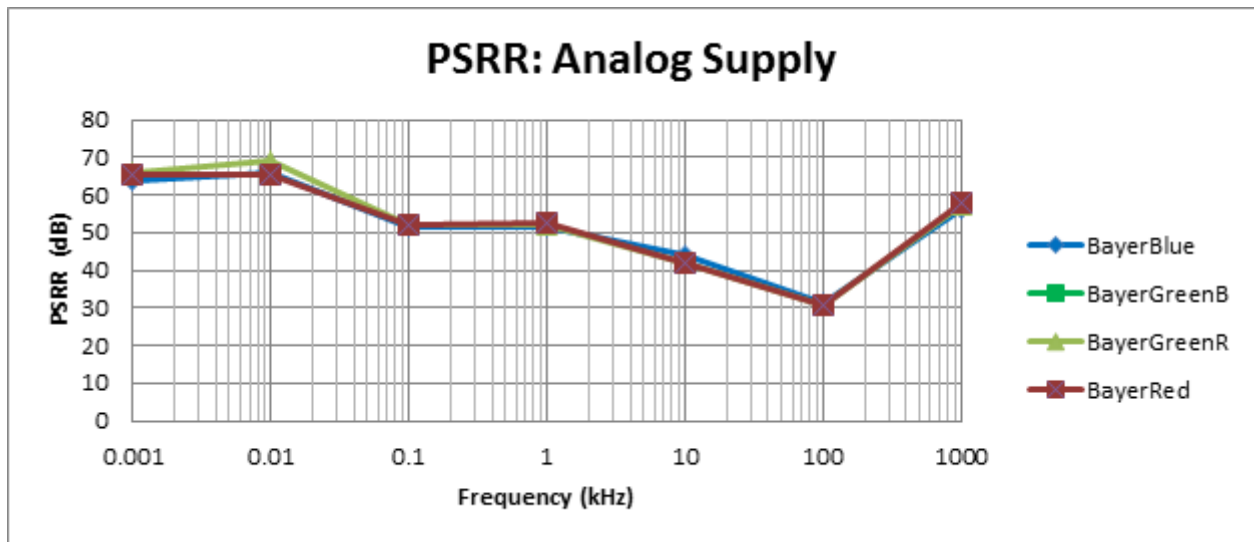


Figure 21. Power Supply Rejection Ratio

**Package Material Information:**

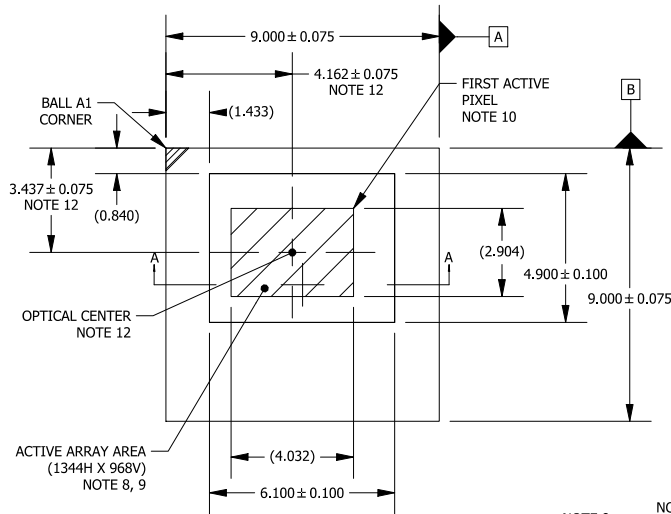
For the listed packages, the following material information applies:

- ENCAPSULANT: EPOXY
- SUBSTRATE MATERIAL: EPOXY LAMINANTE 0.25 THICKNESS
- GLASS MATERIAL: 0.4 THICKNESS; REFRACTIVE INDEX = 1.5; AR COATING R < 1% 420–850nm (EACH SIDE)
- SOLDER BALL MATERIAL: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu) SOLDER BALL PAD:  $\phi$ 0.4 SMD



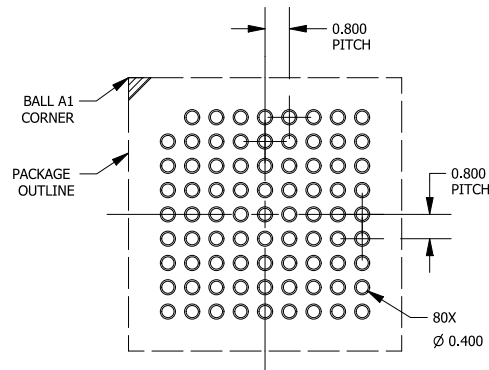
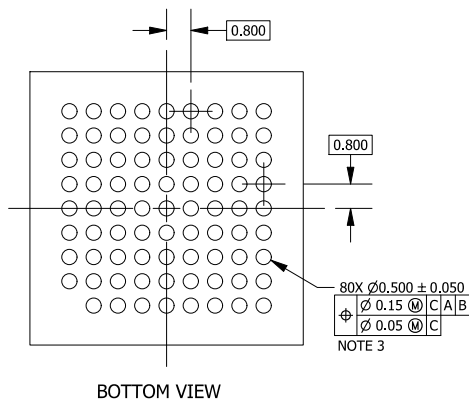
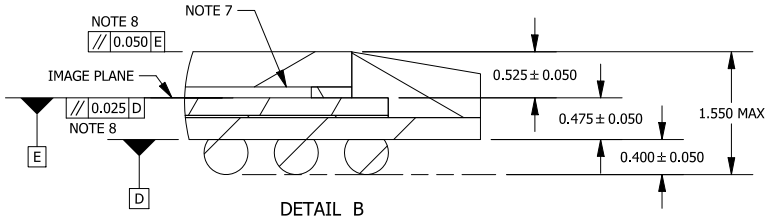
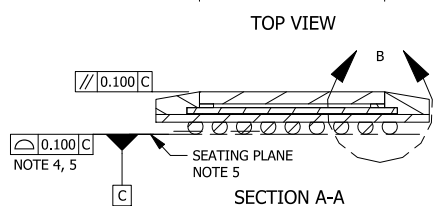
### IBGA80 9x9 CASE 503CB ISSUE A

DATE 05 FEB 2020



NOTES:

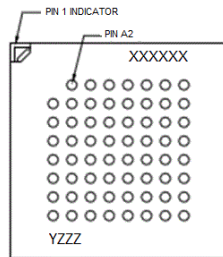
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.400 THICKNESS; REFRACTIVE INDEX = 1.52; AR COATING R<1% 420-850nm (EACH SIDE).
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.125 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 0.5°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. PACKAGE CENTER (X, Y) = (0.000, 0.000).
12. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (-0.338, 1.063).



RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
Y = Year  
ZZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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| <b>DESCRIPTION:</b>     | <b>IBGA80 9X9</b>  | <b>PAGE 1 OF 1</b>  |

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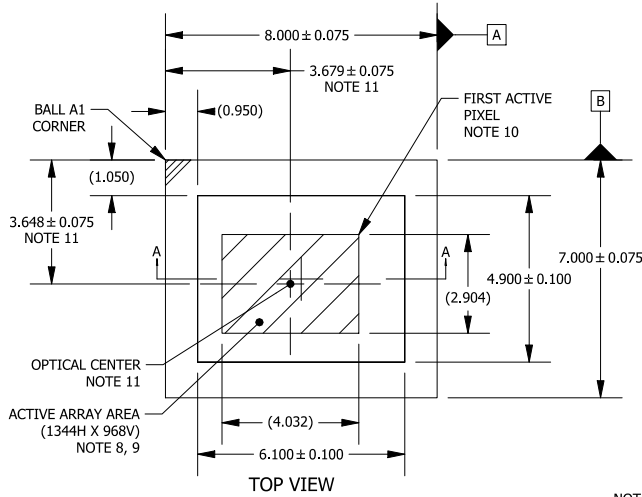
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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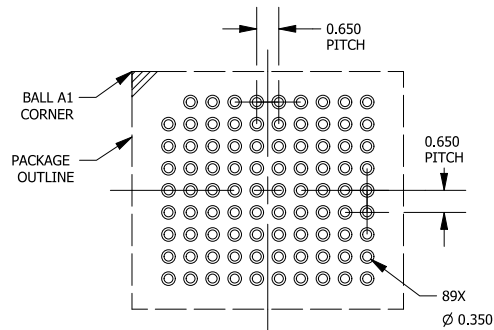
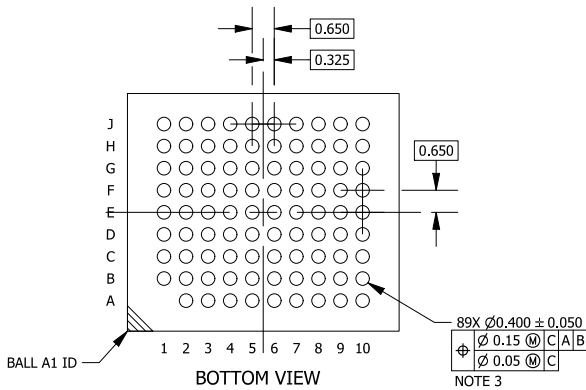
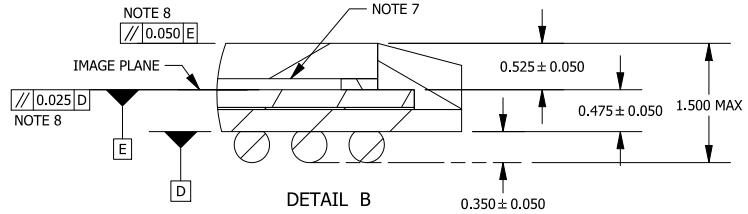
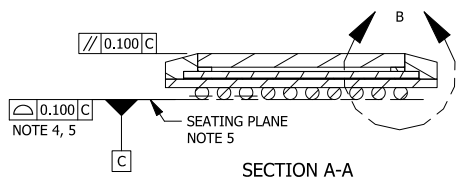
## IBGA89 8x7 CASE 503CC ISSUE A

DATE 05 FEB 2020

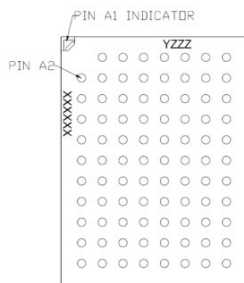


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.400 THICKNESS; REFRACTIVE INDEX = 1.52; AR COATING R<1% 420-850nm (EACH SIDE).
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.125 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 0.5°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (-0.321, -0.148).
12. PACKAGE CENTER (X, Y) = (0.000, 0.000).



### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
Y = Year  
ZZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

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| DESCRIPTION:     | IBGA89 8x7  | PAGE 1 OF 1  |

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