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LV5239TA

Linear LED Driver, 24-Channel, Bus Controlled

Overview

The LV5239TA is a serial bus controlled linear low side driver for LEDs (or other loads). The 24 channels are grouped in 3 color blocks (RGB) of 8 channels each. The ON-time for each channel can be programmed by an 8 bit register. The reference current is programmed by a single resistor, a 3 bit register defines the current for each color block as a fraction (20 to 100%) of the reference current to adjust for color temperature.

Systems parameters can be programmed via 2 wire serial bus, or 3 wire SPI bus with EN.

Features

- LED supply from 3 V to TBDV with transient tolerance up to 42 V.
- System supply from 3 V to 12 V with transient tolerance up to 13.6 V.
- Up to 100 mA resistor defined maximum current for all channels.
- 3 bit individually adjustable current for each color group RGB.
- 8 bit luminance dimming for each channel.
- 2 or 3 wire bus interface with up to 32 slave addresses.
- Thermal and undervoltage lock-out protection.
- Thermally efficient exposed die 48 pin TQFP package for operation up to 85°C ambient.

Typical Applications

- Gaming (slot machine) and entertainment equipment.
- LED displays.
- Digital information signs.

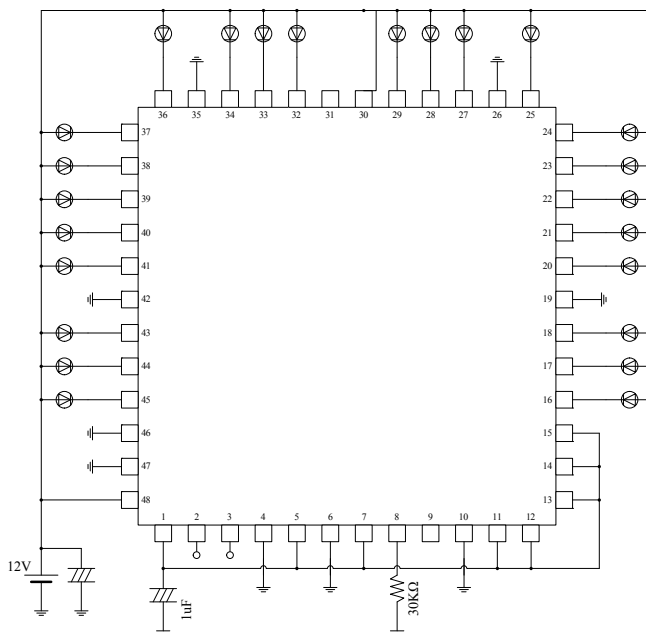
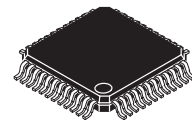


Figure 1: Typical Application Diagram



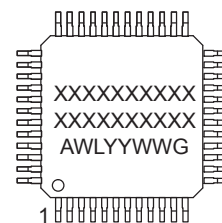
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TQFP48 EP 7x7mm

GENERIC MARKING DIAGRAM



XXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

Ordering Code:
 LV5239TAZ-NH

Package
 TQFP48 EP
 (Pb-Free / Halogen Free)

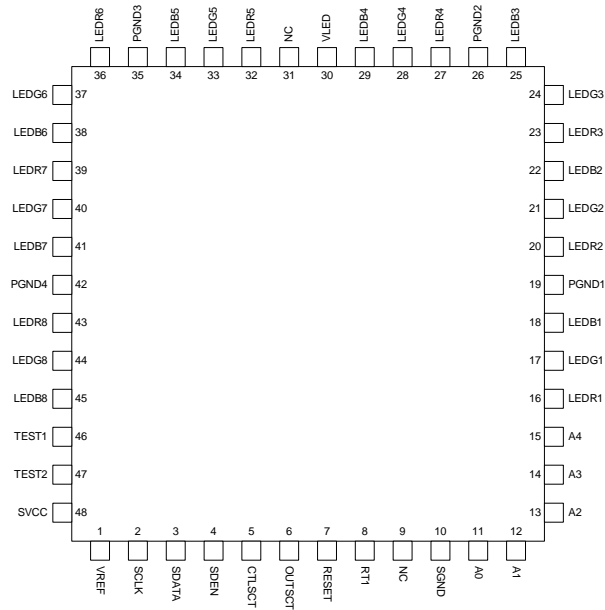
Shipping (Qty / packing)
 1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
<http://www.onsemi.com/pub/link/Collateral/BRD8011-D.PDF>

LV5239TA

PINOUT

Pin Assignment



Pin Descriptions

| Pin No. | Pin name | I/O | Description | Pin Circuit |
|---------|----------|-----|---|-------------|
| 1 | VREF | O | Internal supply output pin. Regulates to 5 V if SVCC is higher than 5 V. Bypass with a TBD capacitor. | |
| 2 | SCLK | I | Serial interface clock signal input pin. Data is latched at the rising clock edge. | TYPE1 |
| 3 | SDATA | I | Serial interface input pin. Data frame consists of: Slave_Address[7:0] – Register_Address[7:0] – Data1[7:0] ... DataN[7:0] | TYPE1 |
| 4 | SDEN | I | Active high, SPI Mode enable signal. Must go low after each SPI frame. Not used for 2 wire interface. | TYPE1 |
| 5 | CTLSCT | I | Select pin for 2-wire or 3-wire interface. Tie to GND for 3-wire, tie to VREF for 2wire bus. | TYPE2 |
| 6 | OUTSCT | I | Analog three level selection pin to set current characteristics for the output channels. See "OUTSCT Setting" on page 8 for details. | TYPE3 |
| 7 | RESET | I | Active high reset input pin. Clears all register settings. | TYPE4 |
| 8 | RT1 | O | Maximum reference current programming pin. Connect a resistor >10 kΩ from this pin to GND to define maximum LED current according to the following formula: IREF = 1.22 x 800 / RT. | TYPE5 |
| 9 | NC | | No connection. | |
| 10 | SGND | - | Analog circuit GND pin. | |
| 11 - 15 | A0-4 | I | Slave address setting pin. Refer to "Slave address setting" on page 9 for details. | TYPE6 |
| 16 | LEDR1 | I | LED red 1 current input pin. | TYPE7 |
| 17 | LEDG1 | I | LED green 1 current input pin. | TYPE7 |
| 18 | LEDB1 | I | LED blue 1 current input pin. | TYPE7 |
| 19 | PGND1 | - | GND pin dedicated for LED driver. Connect directly to ground plane. | |
| 20 | LEDR2 | I | LED red 2 current input pin. | TYPE7 |
| 21 | LEDG2 | I | LED green 2 current input pin. | TYPE7 |
| 22 | LEDB2 | I | LED blue 2 current input pin. | TYPE7 |
| 23 | LEDR3 | I | LED red 3 current input pin. | TYPE7 |
| 24 | LEDG3 | I | LED green 3 current input pin. | TYPE7 |
| 25 | LEDB3 | I | LED blue 3 current input pin. | TYPE7 |
| 26 | PGND2 | - | GND pin dedicated for LED driver. Connect directly to ground plane. | |
| 27 | LEDR4 | I | LED red 4 current input pin. | TYPE7 |
| 28 | LEDG4 | I | LED green 4 current input pin. | TYPE7 |
| 29 | LEDB4 | I | LED blue 4 current input pin | TYPE7 |
| 30 | VLED | | Protection for LED drivers. For higher LED voltages. VLED must be limited to 42.0 V (max). | |
| 31 | NC | | No connection | |
| 32 | LEDR5 | I | LED red 5 current input pin. | TYPE7 |

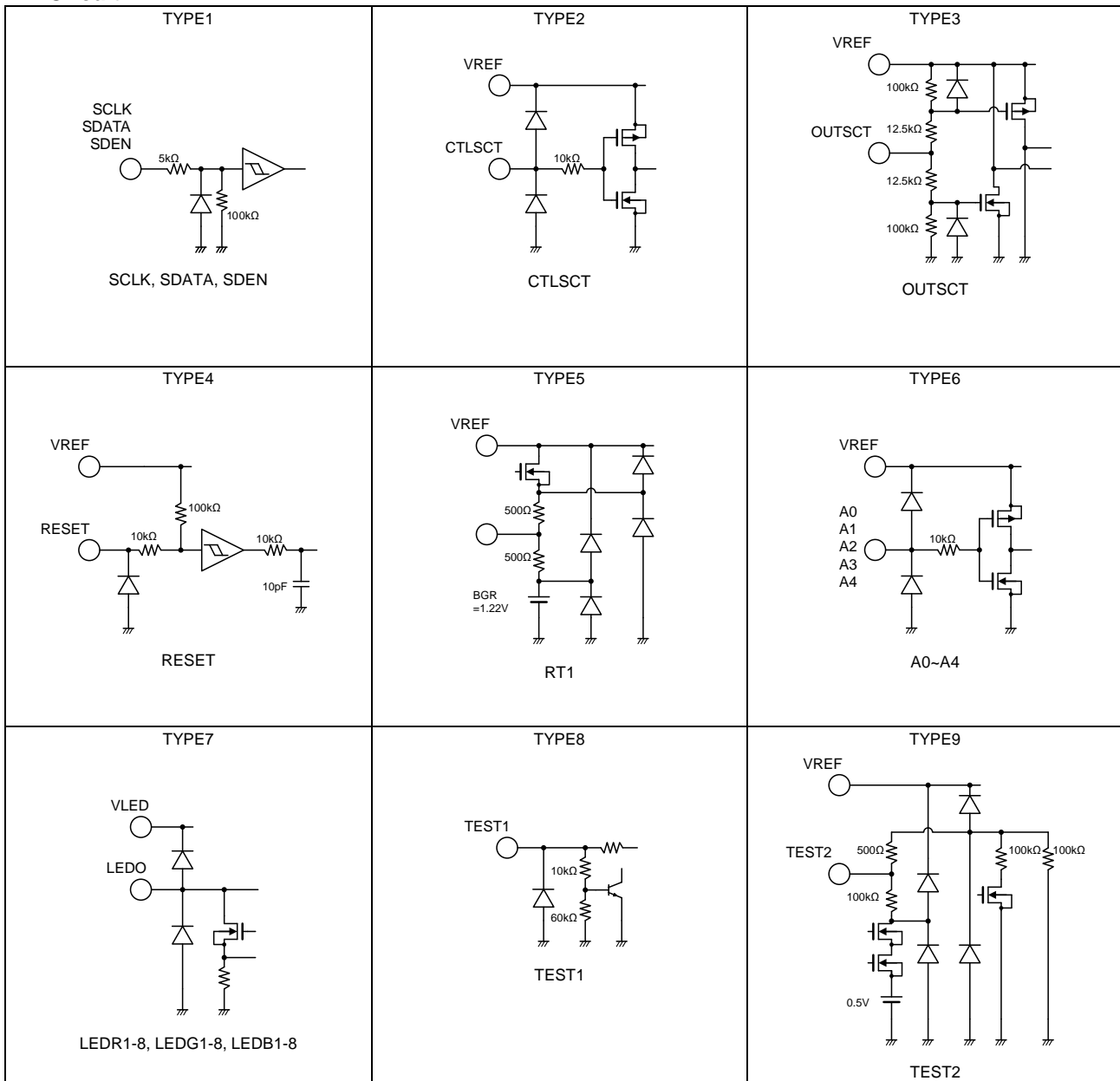
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| Pin No. | Pin name | I/O | Description | Pin Circuit |
|---------|----------|-----|---|-------------|
| 33 | LEDG5 | I | LED green 5 current input pin. | TYPE7 |
| 34 | LEDB5 | I | LED blue 5 current input pin. | TYPE7 |
| 35 | PGND3 | - | GND pin dedicated for LED drivers 4 and 5. Connect directly to ground plane. | |
| 36 | LEDR6 | I | LED red 6 current input pin. | TYPE7 |
| 37 | LEDG6 | I | LED green 6 current input pin. | TYPE7 |
| 38 | LEDB6 | I | LED blue 6 current input pin. | TYPE7 |
| 39 | LEDR7 | I | LED red 7 current input pin. | TYPE7 |
| 40 | LEDG7 | I | LED green 7 current input pin. | TYPE7 |
| 41 | LEDB7 | I | LED blue 7 current input pin. | TYPE7 |
| 42 | PGND4 | - | GND pin dedicated for LED drivers 6 and 7. Connect directly to ground plane. | |
| 43 | LEDR8 | I | LED red 8 current input pin. | TYPE7 |
| 44 | LEDG8 | I | LED green 8 current input pin. | TYPE7 |
| 45 | LEDB8 | I | LED blue 8 current input pin. | TYPE7 |
| 46 | TEST1 | I | Test1 pin (connected to GND) | TYPE8 |
| 47 | TEST2 | I | Test2 pin (connected to GND) | TYPE9 |
| 48 | SVCC | - | System power supply input. For LED supply voltages from 3 to 12 V connect directly to LED supply. For higher LED voltages SVCC must be limited to 13.6 V (max). | |

Pin Circuit



LV5239TA

SPECIFICATIONS

Absolute Maximum Ratings (Note 1,3)

| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------------|---------|--------------------|-------------|------|
| Maximum supply voltage | VCC max | | 13.6 | V |
| | VLED | | 42 | V |
| | VREF | | 5.8 | V |
| Output voltage | VO max | LED off | 42 | V |
| Output current | IO max | Open drain | 100 | mA |
| Allowable power dissipation | Pd max | Ta ≤ 25°C (Note 2) | 1.25 | W |
| Operating temperature | Topr | | -25 to +85 | °C |
| Operating Junction Temperature | Tj | | -25 to +150 | °C |
| Storage temperature | Tstg | | -40 to +150 | °C |

- Stresses exceeding those listed in the Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
- Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board. Exposed Die-pad area is not a substrate mounting.
- If you should intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for a confirmation.

Recommended Operating Conditions (Note 4)

| Parameter | Symbol | Pin | Ratings | Unit |
|--------------------------------|---------------------|------------------|-------------|------|
| Operating supply voltage range | V _{CC OP} | SV _{CC} | 3.0 to 12.8 | V |
| | V _{LED OP} | VLED | 3.0 to 42 | V |
| | V _{REF OP} | VREF | 3.0 to 5.5 | V |

- Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, 3.3 V < VCC < 5 V (Note 5)

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------|------------------|---|---------|------|------|------|
| | | | min | typ | max | |
| Supply current | I _{CC1} | All LEDs off | 1.8 | 2.3 | 2.9 | mA |
| Reference current pin voltage | VRT | RT1 = 30 kΩ | 1.14 | 1.22 | 1.30 | V |
| Line regulation | ΔIL | V _O = 0.7 to 4.0 V (Same channel line regulation) | -10 | | | % |
| Output current accuracy | ΔI _{OL} | I _O = 32.40 mA (Between bits pairing characteristics) | | | 5 | % |
| LED driver output current 1 | IMAX1 | RT1 = 30 kΩ LED OUTSCT = L | 30.0 | 32.4 | 34.8 | mA |
| LED output on resistance 1 | Ron1 | I _O = 10 mA | | 10 | 20 | Ω |
| OFF leak current | Ileak | LED OFF | | | 10 | μA |
| VCC Power on RESET voltage | VPOR | POR release voltage threshold | | 2.5 | | V |
| | VRST | Undervoltage lockout threshold | | 2.3 | | V |
| VREF voltage | VREF | VREF = open | | 4.9 | | V |
| VREF voltage | VREF1 | V _{CC} = 6.0 V, I _O = 10 mA | 4.7 | 5.1 | 5.4 | V |

- Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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Control Circuit at Ta = 25°C, V_{CC} = VREF = 5.0 V (Note 5)

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------|--------|---------------------------------|---------|-----|-----|------|
| | | | min | typ | max | |
| H level 1 | VH1 | Input H level OUTSCT | 4.5 | | 5.0 | V |
| M level 1 | VM1 | Input M level OUTSCT | 1.8 | | 3.0 | V |
| L level 1 | VL1 | Input L level OUTSCT | -0.2 | | 0.5 | V |
| H level 2 | VH2 | Input H level CTLST | 3.5 | | 5.0 | V |
| L level 2 | VL2 | Input L level CTLST | -0.2 | | 0.5 | V |
| H level 3 | VH3 | Input H level RESET | 4.0 | | 5.0 | V |
| L level 3 | VL3 | Input L level RESET | -0.2 | | 1.0 | V |
| H level 4 | VH4 | Input H level SCLK, SDATA, SDEN | 4.0 | | 5.0 | V |
| L level 4 | VL4 | Input L level SCLK, SDATA, SDEN | -0.2 | | 1.0 | V |
| H level 5 | VH5 | Input H level A0 to A4 | 3.5 | | 5.0 | V |
| L level 5 | VL5 | Input L level A0 to A4 | -0.2 | | 0.5 | V |

Control Circuit at Ta = 25°C, V_{CC} = VREF = 3.3 V (Note 5)

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------|--------|---------------------------------|---------|-----|-----|------|
| | | | min | typ | max | |
| H level 1 | VH1 | Input H level OUTSCT | 2.8 | | 3.3 | V |
| M level 1 | VM1 | Input M level OUTSCT | 1.2 | | 1.7 | V |
| L level 1 | VL1 | Input L level OUTSCT | -0.2 | | 0.5 | V |
| H level 2 | VH2 | Input H level CTLST | 2.3 | | 3.3 | V |
| L level 2 | VL2 | Input L level CTLST | -0.2 | | 0.5 | V |
| H level 3 | VH3 | Input H level RESET | 2.7 | | 3.3 | V |
| L level 3 | VL3 | Input L level RESET | -0.2 | | 0.6 | V |
| H level 4 | VH4 | Input H level SCLK, SDATA, SDEN | 2.7 | | 3.3 | V |
| L level 4 | VL4 | Input L level SCLK, SDATA, SDEN | -0.2 | | 0.6 | V |
| H level 5 | VH5 | Input H level A0 to A4 | 2.3 | | 3.3 | V |
| L level 5 | VL5 | Input L level A0 to A4 | -0.2 | | 0.5 | V |

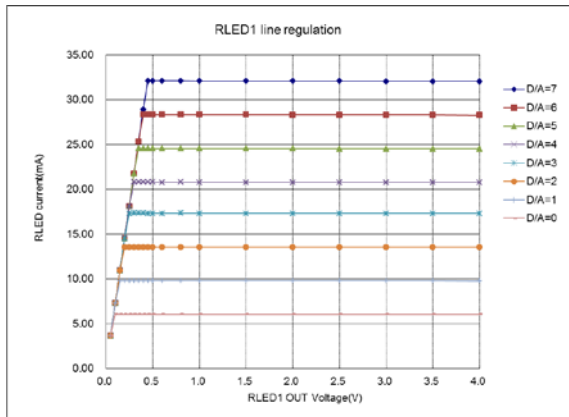
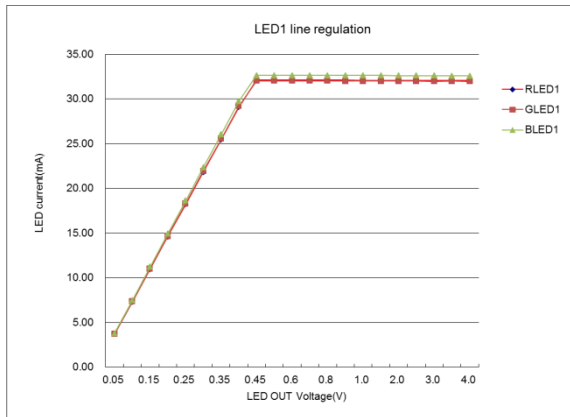
Serial bus timing conditions

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|--------|---|------|------|------|------|
| Cycle time | tcy1 | SCLK clock period | 200 | - | - | ns |
| Data setup time | ts0 | SDEN setup time relative to the rise of SCLK | 90 | - | - | ns |
| | ts1 | SDATA setup time relative to the rise of SCLK | 60 | - | - | ns |
| Data hold time | th0 | SDEN hold time relative to the fall of SCLK | 200 | - | - | ns |
| | th1 | SDATA hold time relative to the fall of SCLK | 60 | - | - | ns |
| Pulse width | tw1L | Low period pulse width of SCLK | 90 | - | - | ns |
| | tw1H | High period pulse width of SCLK | 90 | - | - | ns |
| | tw2L | Low period pulse width of SDEN | 1 | - | - | μs |

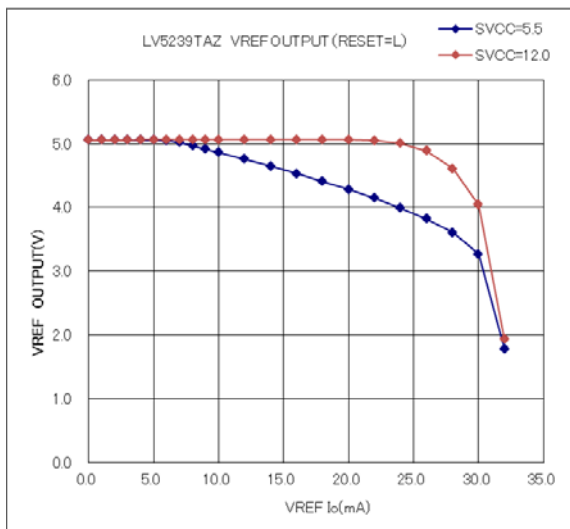
LV5239TA

Typical Operating Characteristics (SVCC = 5.0 V, VREF = 5.0 V)

LEDOUT Line regulation



VREF OUT Load regulation



LV5239TA

Detailed Functional Description

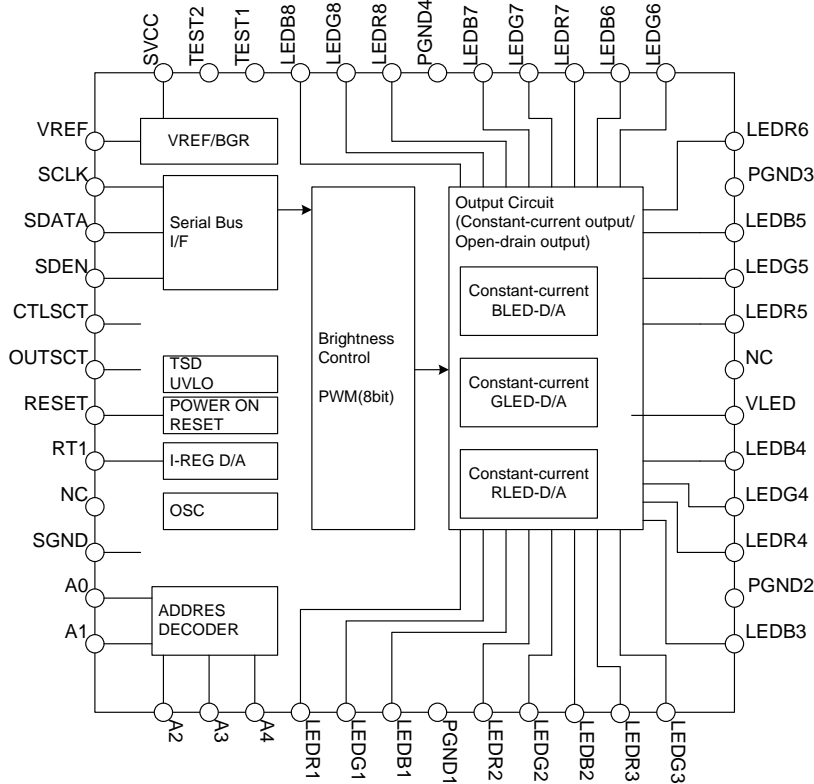


Figure 2: Block Diagram

System Startup and Shutdown (SVCC, RESET)

The LV5239TA is supplied via SVCC. If the voltage on SVCC rises above the POR level of 2.5 V (typ) the

system setup registers are being reset to their default state, and the reference internal reference circuit at VREF starts up.

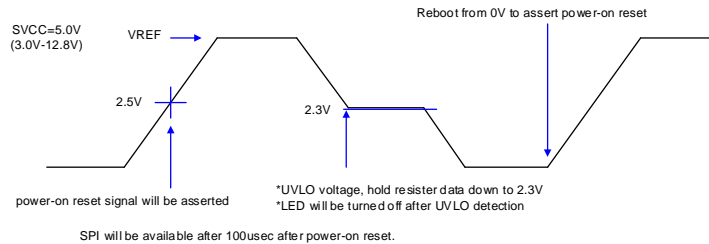


Figure 3: SVCC startup and shutdown

SVCC can be connected to the LED supply of the application as long as that supply is between 3 and 12 V. If the LED supply is higher than 12 V, SVCC must be supplied from a separate source.

An LED reference current is defined by connecting a resistor R_{RT} between RT1 and GND according to the formula: $I_{MAX} = 1.22 \times 800 / R_{RT}$. A fraction of this current (20% - 100%) is applied to each LED channel.

If SVCC drops below the undervoltage lockout level of 2.3 V (typ) the system shuts down.

Internal References (SVCC, VREF, RT1)

An internal voltage reference of 5 V (typ) is generated at VREF from SVCC. Do not connect external loads.

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LED Driver Configuration (LEDR1-8, LEDG1-8, LEDB1-8, OUTSCT)

The LEDs are connected between the system LED supply and IC channels LEDR1-8, LEDG1-8, LEDB1-8 such that the LED current flows into the IC. Depending on the LED drive voltage, it is possible to connect a single LED or a chain of LEDs.

For details on the relationship between chain length, LED supply voltage and power dissipation see section “Thermal considerations” below.

The LV5239TA can adjust color temperature and brightness for up to 24 LEDs. Color temperature is adjusted by varying the LED current, and brightness (luminance) is adjusted by varying the on-time of the LED a fixed time period (duty-cycle).

Color temperature control

The 24 LED channels are organized into 3 color groups (Red, Green, Blue) of 8 channels each. The currents for each color group are programmed by a 3 bit register as a

percentage of the LED reference current I_{MAX} . Percentages of 20, 31, 43, 54, 66, 77 and 100 of are possible.

Luminance control

The brightness of each LED channel is defined by the duty cycle Duty(%): the time t_{ON} the channel is active during a time window t_{CYCLE} . The duty cycle is defined by the following formula. $Duty(\%) = 100 \cdot t_{ON} / t_{CYCLE}$. Each LED channel has an 8-bit register to vary the duty cycle between OFF (0.0%) and 99.6% in steps of 0.39% each.

The PWM period is defined by the 3 most significant bits at address 00h starting with 0.5msec, doubling with each bit up to 8ms.

OUTSCT Settings

In addition to the settings mentioned above, it is also possible to subdivide the 8 LED channels within the color groups into 6 and 2 LED channels grouped in the following way:

| OUTSCT Level | LED Driver Output Pin | |
|----------------|---|--|
| | LED1, LED2, LED3, LED4, LED5, LED6 | LED7, LED8 |
| L=-0.2 to 0.3V | Constant current output Set maximum current by built-in D/A (3 bits) 6.40 mA to 32.40 mA, RT1 = 30 kΩ (f = 1 MHz) | Same as the other LEDs |
| H=4.7 to 5.0V | Open drain output Set current by external resistor. $R_{ON} = 10 \Omega$ | Same as the other LEDs |
| M=1.8 to 3.0V | Constant current output Set maximum current by built-in D/A (3 bits) 6.40 mA to 32.40 mA, RT1 = 30 kΩ (f = 1 MHz) | Open drain output Set current by external resistor. $R_{ON} = 10 \Omega$ |

Thermal Considerations

Supplying a large number of LEDs from the LV5239TA leads to a rise in chip temperature. The self-heating depends on:

- the drive current I_O flowing into the LED channel
- the voltage at the output V_{OUT} of the LED channel
- and the duty cycle D they are driven with

leading to the following formula for dissipated power in each channel:

$$P_{CH} = I_O \times V_{OUT} \times D$$

The only architecture sensitive value is V_{OUT} . It must be greater than 0.5 V (min) to allow for regulation, but also as small as possible. It is therefore advisable to connect the maximum possible number of LEDs in series to one channel.

The total power dissipation P_{TOT} of the IC is then the sum of all P_{CH} together. P_{TOT} must not exceed the power allowed by the safe operating area shown in Figure 4.

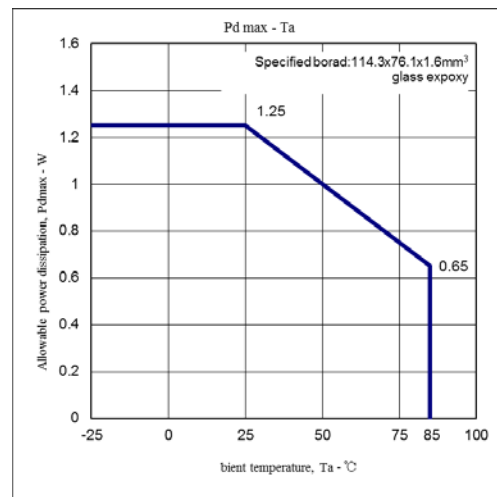


Figure 4: Safe Operating Area

To make evaluation of the actual drive capability easier, a number of plots are included after page 13. These plots show the safe operating area for LED string current I_O on the vertical axis, the number of active RGB Channels on the horizontal axis (times 3 for each color group) along with individual duty cycle curves at a given V_{OUT} and temperature.

LV5239TA

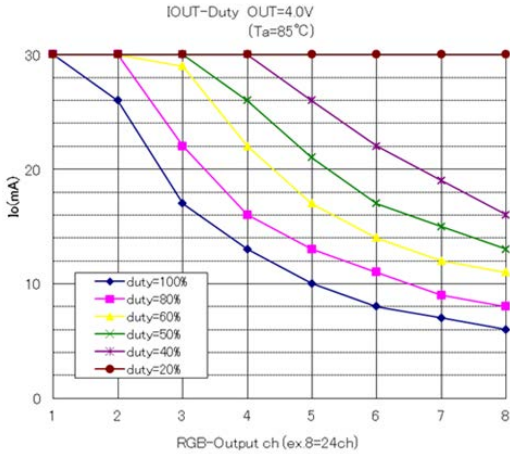


Figure 5: Thermally Safe Operation Example

The example in Figure 5 shows operation of up to 8 RGB channels (24LEDs) at 85°C and a channel voltage of 4 V. Operation below the curve is safe! It is therefore possible to drive 2 RGB LEDs (6 channels) at 20 mA or 8 RGB LEDs (24 channels) at 4 mA with 100% duty cycle. If only 20% duty cycle is required, all 8 RGBLEDs can be driven with 20 mA.

See more examples in section “LEDOUT Duty Cycle De-rating” starting on page 13.

Overtemperature shutoff

To protect the circuit from permanent damage or fire, overtemperature shutoff is implemented. If the junction temperature of the IC reaches 175°C, all LED outputs are turned OFF. The thermal shut down is not latched, so when the temperature falls below 130°C activity resumes.

Serial Bus Communication (SCLK, SDATA, SDEN, CTLST)

All parameters described above are written to the LV5239TA via a single directional 2-wire or 3-wire serial bus with a clock frequency of up to 5 MHz. The bus type is defined by the state of pin CTLST (VREF = 2-wire, GND = 3-wire).

Each bus message consists of an 8bit slave (IC) address, followed by an 8bit register address, followed by one or more 8bit data words. The register address will self-increment for consecutive data words as long as the communication is valid. After the last address was written, the next data word will be written to address 00h again. For detailed information on addresses and register contents see section “Register Map” on page 12.

Slave Address (A4-A0)

Each IC is identified by its unique slave address. The most significant two bits of the 8bit slave (IC) address are fixed to 10b. 32 Slave addresses are hardware defined by pins A0-A4 as described below.

| | SA7 | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| ADDRESS | 1 | 0 | A4 | A3 | A2 | A1 | A0 | 0 |

| Terminal PIN (Input) | | | | | SLAVE ADDRESS | | | | | | | |
|----------------------|----|----|----|----|---------------|-----|-----|-----|-----|-----|-----|-----|
| A4 | A3 | A2 | A1 | A0 | SA7 | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 |
| L | L | L | L | L | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ... | | | | | 1 | 0 | A4 | A3 | A2 | A1 | A0 | 0 |
| H | H | H | H | H | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |

3-wire Serial Bus Communication (SCLK, SDATA, and SDEN)

In 3-wire communication a frame is started with a rising edge of SDEN and terminated with a falling edge of

SDEN. SCLK latches data at the rising edge. The smallest data word is 24bits long consisting of:

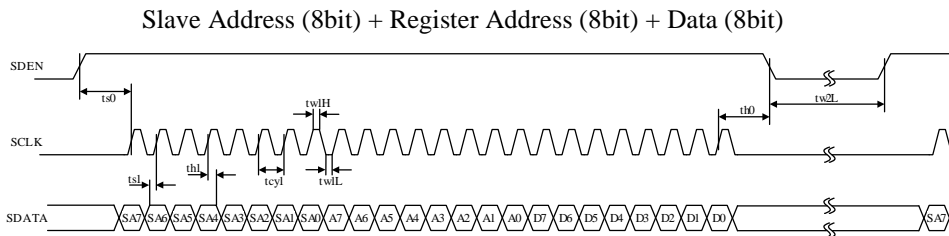
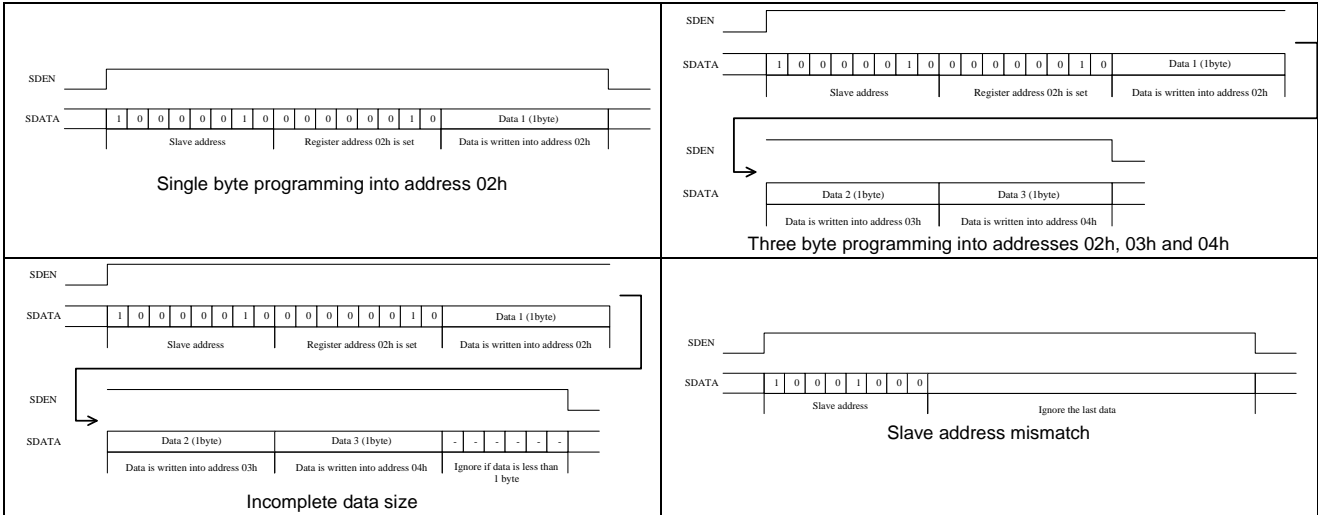


Figure 6: 3 Wire Serial Data Frame

If the number of SCLK transitions is less than 23, Data is not latched. If it is 25 or more, the register address is automatically incremented and the next data word will be latched after eight clock cycles.

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Data write examples into slave 82h



2-wire Serial Bus Communication (SCLK, SDATA)

In 2-wire communication the LV5239TA watches SDATA at every rising SCLK edge. A data frame begins after START condition: nine consecutive detections of a “1” (high) followed by a “0” (BLANK). This is true even during an ongoing data transfer: serial communication will be restarted by a START condition (“11111111”) + BLANK (“0”).

After start detection, the eight bit slave address will be latched after receiving a BLANK (0h) with the ninth bit. The register address will be latched after receiving a BLANK “0” after eight address bits. The third byte is the

data byte which was addressed by the register address received before. The data byte will be latched after receiving a BLANK “0” in position nine after eight data bits.

When data bytes continue after this, the register address will be automatically incremented after each byte transfer is completed after receiving BLANK “0”.

If the BLANK after a data transfer is “1”, including slave address and register address, the single byte data just before it will not be written, and subsequent data is ignored until another START condition is detected.

| bit | ST8 | ST7 | ST6 | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | BL | SA7 | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | BL | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | BL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | BL |
|-----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-------|---------------|-----|-----|-----|-----|-----|-----|-----|-------|------------------|----|----|----|----|----|----|----|-------|------|----|----|----|----|----|----|----|-------|
| SDATA | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | | | | | | | 0 | 0 | | | | | | | | 0 | | | | | | | | 0 | |
| Parameter | Start condition | | | | | | | | | BLANK | Slave address | | | | | | | | BLANK | Register address | | | | | | | | BLANK | Data | | | | | | | | BLANK |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

▲ Fix slave address

▲ Fix register address

▲ Fix Data

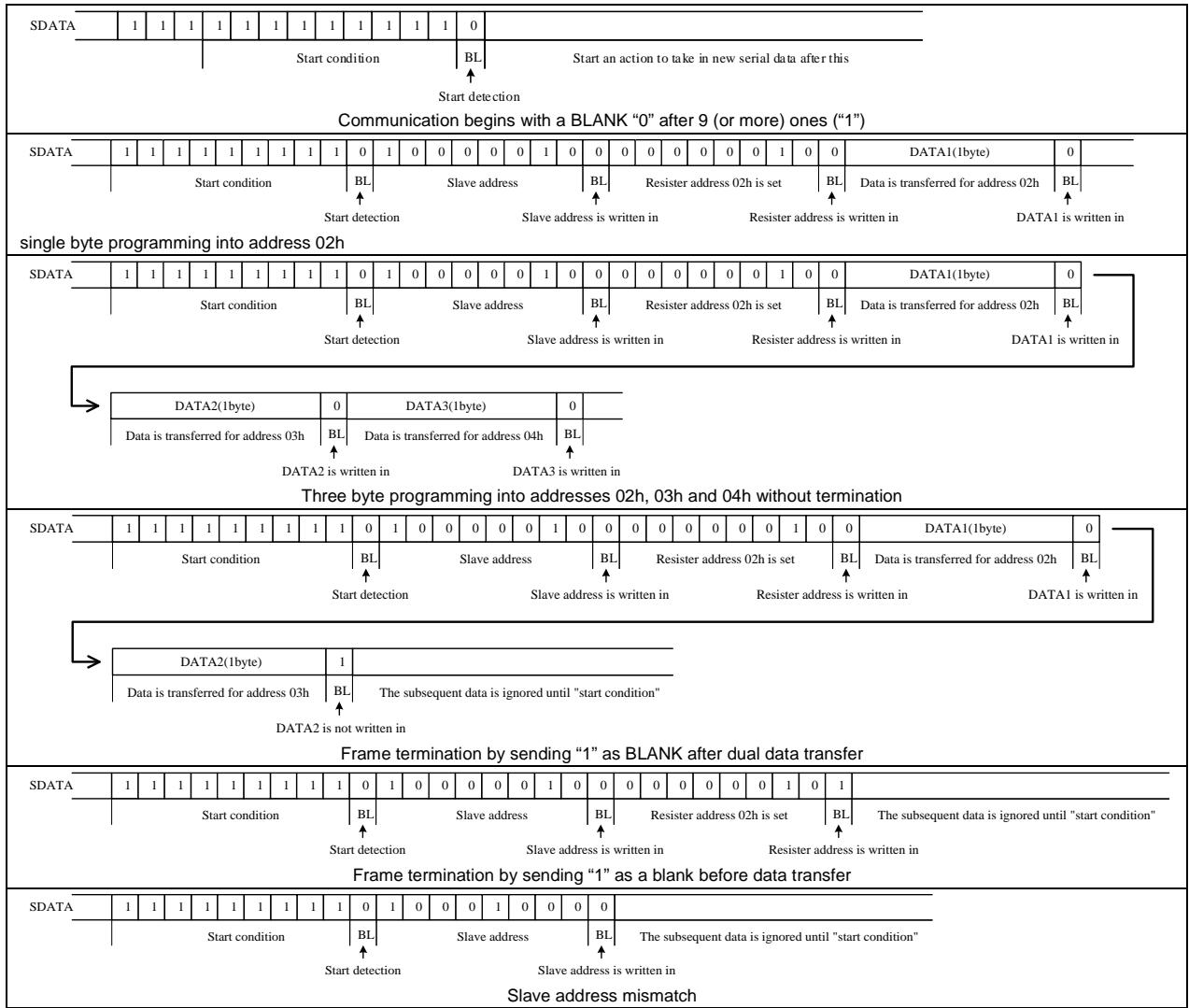
Figure 7 : 2-wire Serial Communication Frame

Minimum Data length is 37bits:
 Start condition “11111111”(9bit) + BLANK(“0”)
 + Slave address(8bit) + BLANK(“0”) + Register
 address(8bit) + BLANK(“0”) + Data(8bit) +
 BLANK(“0”).

Note: When SCLK is less than 27th clocks and/or BLANK is “1” instead of “0” after start detection, will not take in SDATA. When SCLK is higher than 28th clock track, start detection is confirmed, register address is incremented every 1byte (8bit) + BLANK (“0”).

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Data write examples into slave 82h



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Register Map

After POR all registers are cleared.

Frequency and Color Temperature Registers

| Addr. | Register | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Description | | |
|-------|--------------|------------|------|------|-------------|------|------|-------------|--|------------------------------|--|------------------------------|
| 00h | LEDR&fPWM | F_PWM[2:0] | | | I_LEDR[2:0] | | | | | | LEDR current setting (LEDR1 ~ LED8) | |
| | | | | | | | 0 | 0 | 0 | 0 | 20% of I _{max} (6.4 mA @ RT = 30 k) | |
| | | | | | | | 0 | 0 | 1 | 0 | 31% of I _{max} (10.15 mA @ RT = 30 k) | |
| | | | | | | | 0 | 1 | 0 | 0 | 43% of I _{max} (13.90 mA @ RT = 30 k) | |
| | | | | | | | 0 | 1 | 1 | 1 | 54% of I _{max} (17.65 mA @ RT = 30 k) | |
| | | | | | | | 1 | 0 | 0 | 0 | 66% of I _{max} (21.15 mA @ RT = 30 k) | |
| | | | | | | | 1 | 0 | 1 | 1 | 77% of I _{max} (24.90 mA @ RT = 30 k) | |
| | | | | | | | 1 | 1 | 0 | 0 | 88% of I _{max} (28.65 mA @ RT = 30 k) | |
| | | | | | | | 1 | 1 | 1 | 1 | I _{max} = 1.22 x 800 / RT (32.4 mA @ RT = 30 k) | |
| | | 0 | 0 | 0 | | | | | | | | 0.5 ms (PWM-Duty cycle time) |
| | | 0 | 0 | 1 | | | | | | | | 1.0 ms (PWM-Duty cycle time) |
| 0 | 1 | 0 | | | | | | | | 2.0 ms (PWM-Duty cycle time) | | |
| 0 | 1 | 1 | | | | | | | | 4.0 ms (PWM-Duty cycle time) | | |
| 1 | 0 | 0 | | | | | | | | 8.0 ms (PWM-Duty cycle time) | | |
| 01h | LEDG Current | | | | | | | I_LEDG[2:0] | | | LEDG current setting (LEDG1~LEDG8) | |
| | | | | | | | 0 | 0 | 0 | 0 | 20% of I _{max} (6.4 mA @ RT = 30 k) | |
| | | | | | | | 0 | 0 | 1 | 1 | 31% of I _{max} (10.15 mA @ RT = 30 k) | |
| | | | | | | | 0 | 1 | 0 | 0 | 43% of I _{max} (13.90 mA @ RT = 30 k) | |
| | | | | | | | 0 | 1 | 1 | 1 | 54% of I _{max} (17.65 mA @ RT = 30 k) | |
| | | | | | | | 1 | 0 | 0 | 0 | 66% of I _{max} (21.15 mA @ RT = 30 k) | |
| | | | | | | | 1 | 0 | 1 | 1 | 77% of I _{max} (24.90 mA @ RT = 30 k) | |
| | | | | | | | 1 | 1 | 0 | 0 | 88% of I _{max} (28.65 mA @ RT = 30 k) | |
| | | | | | 1 | 1 | 1 | 1 | I _{max} = 1.22 x 800 / RT (32.4 mA @ RT = 30 k) | | | |
| 02h | LEDB Current | | | | | | | I_LEDB[2:0] | | | LEDB current setting (LEDB1~8) | |
| | | | | | | | 0 | 0 | 0 | 0 | 20% of I _{max} (6.4 mA @ RT = 30 k) | |
| | | | | | | | 0 | 0 | 1 | 1 | 31% of I _{max} (10.15 mA @ RT = 30 k) | |
| | | | | | | | 0 | 1 | 0 | 0 | 43% of I _{max} (13.90 mA @ RT = 30 k) | |
| | | | | | | | 0 | 1 | 1 | 1 | 54% of I _{max} (17.65 mA @ RT = 30 k) | |
| | | | | | | | 1 | 0 | 0 | 0 | 66% of I _{max} (21.15 mA @ RT = 30 k) | |
| | | | | | | | 1 | 0 | 1 | 1 | 77% of I _{max} (24.90 mA @ RT = 30 k) | |
| | | | | | | | 1 | 1 | 0 | 0 | 88% of I _{max} (28.65 mA @ RT = 30 k) | |
| | | | | | 1 | 1 | 1 | 1 | I _{max} =1.22x800/RT (32.4 mA @ RT = 30 k) | | | |

Luminance Registers

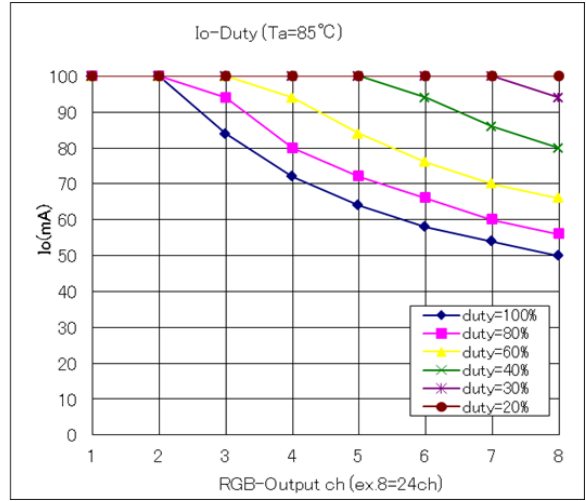
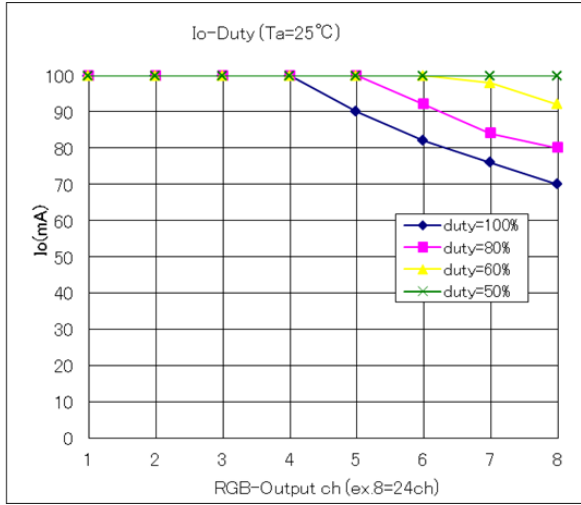
| Addr. | Register | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Description |
|-------|--------------|---------|-------|-------|-------|-------|-------|-------|-------|--|
| 03h | PWM SEL LEDR | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | Select PWM or Full on for LEDR1 ~ LEDR8 0 = Use PWM as set by the registers below. 1 = Full on (100%PWM) |
| 04h | PWM SEL LEDG | G8 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | Select PWM or Full on for LEDG1 ~ LEDG8 0 = Use PWM as set by the registers below. 1 = Full on (100%PWM) |
| 05h | PWM SEL LEDB | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | Select PWM or Full on for LEDB1 ~ LEDB8 0 = Use PWM as set by the registers below. 1 = Full on (100%PWM) |
| 06h | LEDR1 Duty | R1[7] | R1[6] | R1[5] | R1[4] | R1[3] | R1[2] | R1[1] | R1[0] | PWM duty setting for LEDR1 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Duty(%) = 0.0% |
| | | R1[7:0] | | | | | | | | |
| | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Duty(%) = 99.6% |
| 07h | LEDG1 Duty | G1[7:0] | | | | | | | | |
| 08h | LEDB1 Duty | B1[7:0] | | | | | | | | |
| 09h | LEDR2 Duty | R2[7:0] | | | | | | | | |
| 0Ah | LEDG2 Duty | G2[7:0] | | | | | | | | |
| 0Bh | LEDB2 Duty | B2[7:0] | | | | | | | | |
| 0Ch | LEDR3 Duty | R3[7:0] | | | | | | | | |
| 0Dh | LEDG3 Duty | G3[7:0] | | | | | | | | |
| 0Eh | LEDB3 Duty | B3[7:0] | | | | | | | | |
| 0Fh | LEDR4 Duty | R4[7:0] | | | | | | | | |
| 10h | LEDG4 Duty | G4[7:0] | | | | | | | | |
| 11h | LEDB4 Duty | B4[7:0] | | | | | | | | |
| 12h | LEDR5 Duty | R5[7:0] | | | | | | | | |
| 13h | LEDG5 Duty | G5[7:0] | | | | | | | | |
| 14h | LEDB5 Duty | B5[7:0] | | | | | | | | |
| 15h | LEDR6 Duty | R6[7:0] | | | | | | | | |
| 16h | LEDG6 Duty | G6[7:0] | | | | | | | | |
| 17h | LEDB6 Duty | B6[7:0] | | | | | | | | |
| 18h | LEDR7 Duty | R7[7:0] | | | | | | | | |
| 19h | LEDG7 Duty | G7[7:0] | | | | | | | | |
| 1Ah | LEDB7 Duty | B7[7:0] | | | | | | | | |
| 1Bh | LEDR8 Duty | R8[7:0] | | | | | | | | |
| 1Ch | LEDG8 Duty | G8[7:0] | | | | | | | | |
| 1Dh | LEDB8 Duty | B8[7:0] | | | | | | | | |

Same as LEDR1 description

LEDOUT Duty Cycle De-rating

All channels in switch mode(OUTSCT=H)

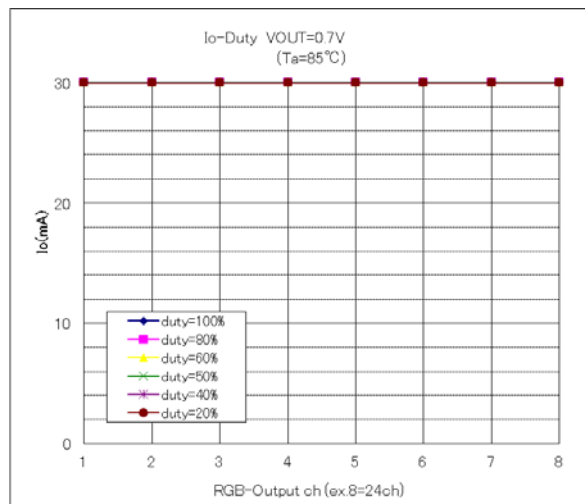
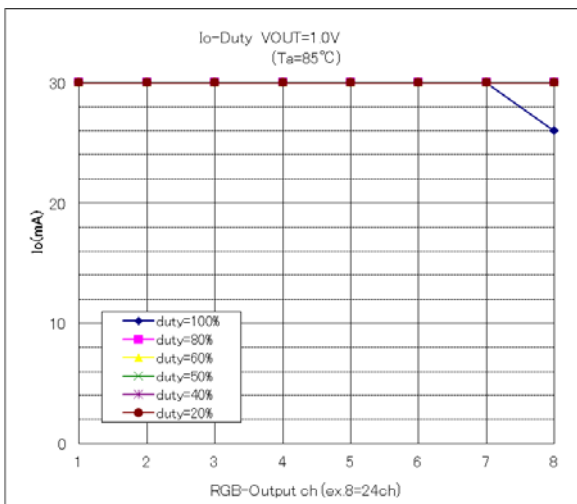
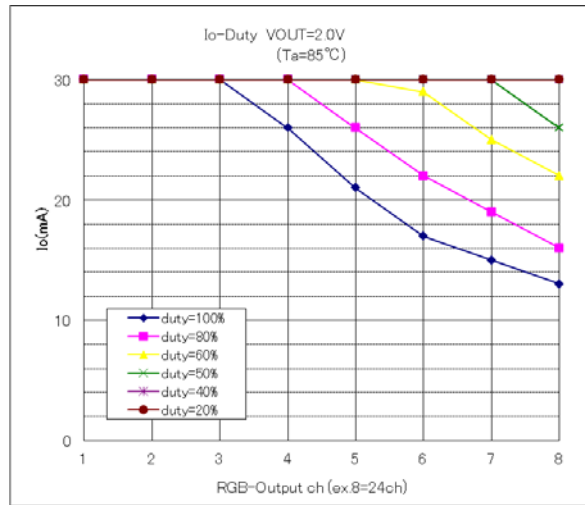
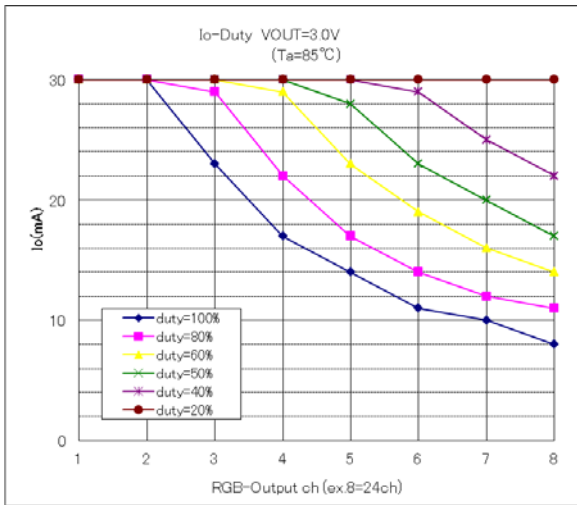
Note: In this case the LED current must be limited by external resistors!



All channels use internal current control (OUTSCT=L)

Note: In this case the LED current must be limited by resistance of RT1. Furthermore, must manage it in

register 00h and 01h and 02h. and manage even the Duty setting.



LV5239TA

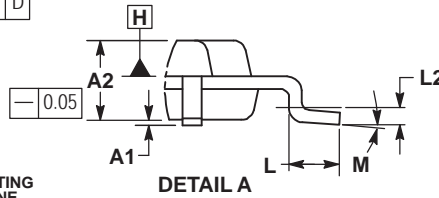
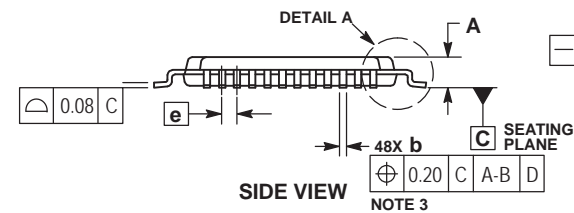
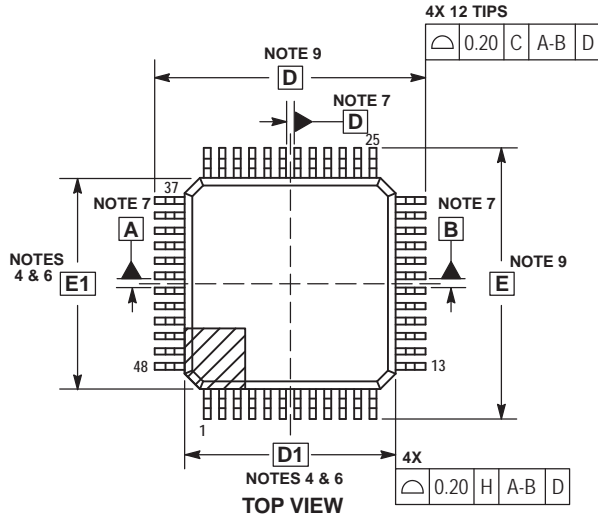
Package Dimensions

unit : mm

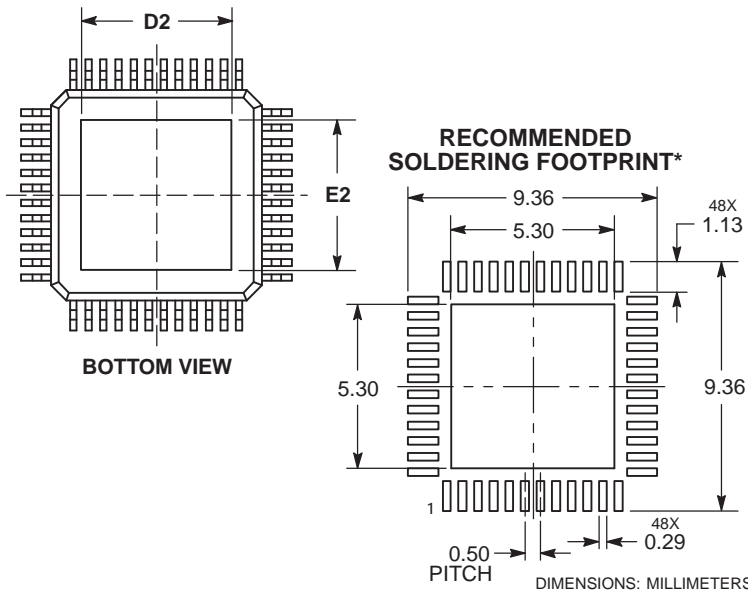
TQFP48 EP 7x7, 0.5P

CASE 932F

ISSUE C



| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.95 | 1.25 |
| A1 | 0.05 | 0.15 |
| A2 | 0.90 | 1.20 |
| b | 0.17 | 0.27 |
| D | 9.00 BSC | |
| D1 | 7.00 BSC | |
| D2 | 4.90 | 5.10 |
| E | 9.00 BSC | |
| E1 | 7.00 BSC | |
| E2 | 4.90 | 5.10 |
| e | 0.50 BSC | |
| L | 0.45 | 0.75 |
| L2 | 0.25 BSC | |
| M | 0° | 7° |



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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