# **MOSFET** – Power, P-Channel, SOT-223

-5.2 A, -30 V

#### **Features**

- Ultra Low R<sub>DS(on)</sub>
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature SOT-223 Surface Mount Package
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable NVF5P03T3G
- These Devices are Pb-Free and are RoHS Compliant

#### **Applications**

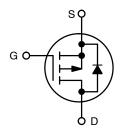
- DC-DC Converters
- Power Management
- Motor Controls
- Inductive Loads
- Replaces MMFT5P03HD



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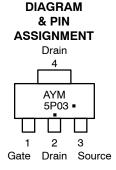
## -5.2 AMPERES, -30 VOLTS $R_{DS(on)} = 100 \text{ m}\Omega$



P-Channel MOSFET



SOT-223 CASE 318E STYLE 3



**MARKING** 

A = Assembly Location

Y = Year

M = Date Code

5P03 = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTF5P03T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NVF5P03T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## $\label{eq:maximum RATINGS} \begin{tabular}{ll} MAXIMUM RATINGS ($T_J=25^{\circ}C$ unless otherwise noted) \\ \begin{tabular}{ll} Negative sign for P-Channel devices omitted for clarity \\ \end{tabular}$

Rating		Symbol	Max	Unit
Drain-to-Source Voltage		V <sub>DSS</sub>	-30	V
Drain-to-Gate Voltage	$e (R_{GS} = 1.0 M\Omega)$	$V_{DGR}$	-30	V
Gate-to-Source Voltage	ge – Continuous	V <sub>GS</sub>	± 20	V
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		P <sub>D</sub>	40 3.13 25 -5.2 -4.1 -26	°C/W Watts mW/°C A A
Minimum FR-4 or G-10 PCB 10 seconds	Thermal Resistance – Junction to Ambient Total Power Dissipation @ $T_A$ = 25°C Linear Derating Factor Drain Current – Continuous @ $T_A$ = 25°C Continuous @ $T_A$ = 70°C Pulsed Drain Current (Note 1)	R <sub>THJA</sub> P <sub>D</sub> I <sub>D</sub> I <sub>D</sub>	80 1.56 12.5 -3.7 -2.9 -19	°C/W Watts mW/°C A A A
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J=25^{\circ}C$ ( $V_{DD}=-30$ Vdc, $V_{GS}=-10$ Vdc, Peak $I_L=-12$ Apk, $L=3.5$ mH, $R_G=25~\Omega$ )		E <sub>AS</sub>	250	mJ

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

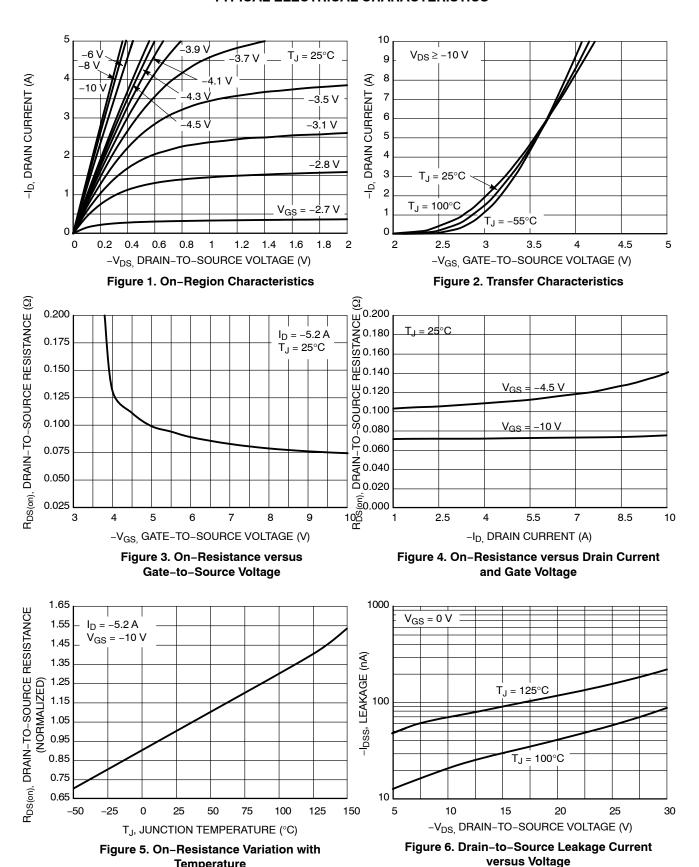
<sup>1.</sup> Repetitive rating; pulse width limited by maximum junction temperature.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C unless otherwise noted)

Chara	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltag	V <sub>(BR)DSS</sub>	00			Vdc	
$(V_{GS} = 0 \text{ Vdc}, I_D = -250 \mu\text{Adc})$ Temperature Coefficient (Positive)		-30 -	- -28		mV/°C	
Zero Gate Voltage Drain Current $(V_{DS} = -24 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = -24 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_{CS})$	I <sub>DSS</sub>		- -	-1.0 -25	μAdc	
Gate-Body Leakage Current (V <sub>GS</sub> = ± 20 Vdc, V <sub>DS</sub> = 0 Vdc)		I <sub>GSS</sub>	-	_	± 100	nAdc
ON CHARACTERISTICS (Note 2	)	1	I	1	I	1
Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 2 and 4) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = −250 μAdc) Threshold Temperature Coefficient (Negative)		V <sub>GS(th)</sub>	-1.0 -	-1.75 3.5	-3.0 -	Vdc mV/°C
Static Drain-to-Source On-Resista	, ,	R <sub>DS(on)</sub>		76	100	mΩ
$(V_{GS} = -10 \text{ Vdc}, I_D = -5.2 \text{ Adc})$ $(V_{GS} = -4.5 \text{ Vdc}, I_D = -2.6 \text{Adc})$			_	107	150	
Forward Transconductance (Note 2) (V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -2.0 Adc)	9fs	2.0	3.9	-	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	$(V_{DS} = -25 \text{ Vdc}, V_{GS} = 0 \text{ V},$	C <sub>iss</sub>	_	500	950	pF
Output Capacitance	f = 1.0 MHz)	C <sub>oss</sub>	_	153	440	
Transfer Capacitance		C <sub>rss</sub>	_	58	140	
SWITCHING CHARACTERISTIC	CS (Note 3)					
Turn-On Delay Time	$(V_{DD} = -15 \text{ Vdc}, I_D = -4.0 \text{ Adc},$	t <sub>d(on)</sub>	_	10	24	ns
Rise Time	$V_{GS}$ = -10 Vdc, R <sub>G</sub> = 6.0 Ω) (Note 2)	t <sub>r</sub>	_	33	48	
Turn-Off Delay Time		t <sub>d(off)</sub>	_	38	94	
Fall Time		t <sub>f</sub>	-	20	92	
Turn-On Delay Time	$(V_{DD} = -15 \text{ Vdc}, I_D = -2.0 \text{ Adc},$	t <sub>d(on)</sub>	-	16	38	ns
Rise Time	$V_{GS} = -10 \text{ Vdc},$ $R_G = 6.0 \Omega) \text{ (Note 2)}$	t <sub>r</sub>	-	45	110	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	23	60	
Fall Time		t <sub>f</sub>	-	24	80	1
Gate Charge	$(V_{DS} = -24 \text{ Vdc}, I_D = -4.0 \text{ Adc}, V_{GS} = -10 \text{ Vdc}) \text{ (Note 2)}$	Q <sub>T</sub>	-	15	38	nC
		Q <sub>1</sub>	-	1.6	=	
		Q <sub>2</sub>	-	3.5	_	
		Q3	-	2.6	-	
SOURCE-DRAIN DIODE CHAR	ACTERISTICS			_		
Forward On-Voltage	$(I_S = -4.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = -4.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$ $T_J = 125^{\circ}\text{C}) \text{ (Note 2)}$	V <sub>SD</sub>		-1.1 -0.89	-1.5 -	Vdc
Reverse Recovery Time	$(I_S = -4.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$	t <sub>rr</sub>	_	34	_	ns
·	dl <sub>S</sub> /dt = 100 A/µs) (Note 2)	t <sub>a</sub>	_	20	_	1
		t <sub>b</sub>	_	14	_	1
Reverse Recovery Stored Charge		Q <sub>RR</sub>	_	0.036	_	μC

- 2. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.
  3. Switching characteristics are independent of operating junction temperatures.
  4. Reflects typical values.  $Cpk = \left | \frac{\text{Max limit} Typ}{3 \times \text{SIGMA}} \right |$

#### TYPICAL ELECTRICAL CHARACTERISTICS



**Temperature** 

#### TYPICAL ELECTRICAL CHARACTERISTICS

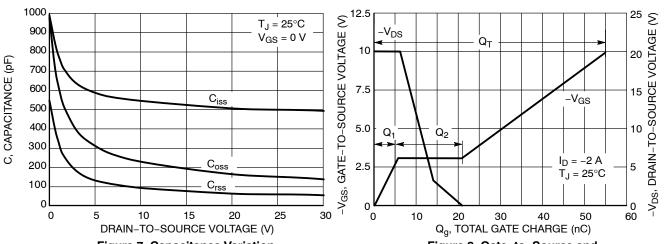


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

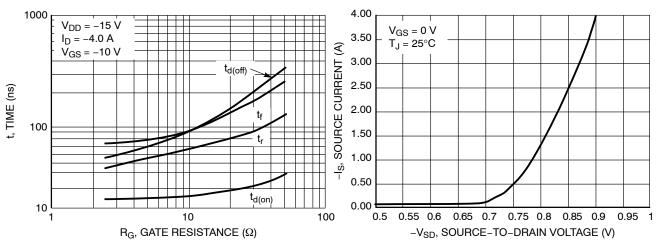


Figure 9. Resistive Switching Time Variation versus Gate Resistance

100

10

 $V_{GS} = 20 V$ 

T<sub>C</sub> = 25°C

SINGLE PULSE

NGLE PULSE DRAIN-TO-SOURCE AVALANCHE ENERGY (mJ) 250  $I_D = -6 A$ 150 100 SINGLE 50 EAS, O 25 100 150 T<sub>J</sub>, STARTING JUNCTION TEMPERATURE (°C)

Figure 10. Diode Forward Voltage versus Current

-ID, DRAIN CURRENT (AMPS) 10 ms 1 ms 100 μs 0.1 R<sub>DS(on)</sub> LIMIT 10 μs THERMAL LIMIT PACKAGE LIMIT 0.01 100 10 -V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (VOLTS) Mounted on 2"sq. FR4 board (1"sq. 2 oz. Cu 0.06" thick single sided) with on die operating, 10 s max.

Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy versus **Starting Junction Temperature** 

#### TYPICAL ELECTRICAL CHARACTERISTICS

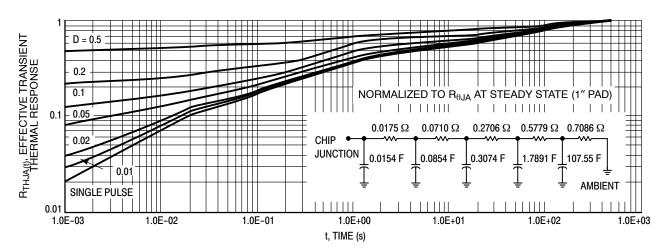
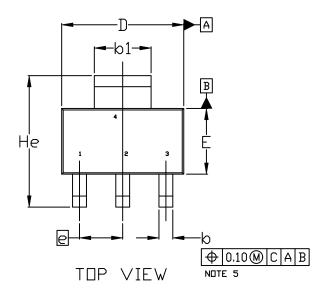


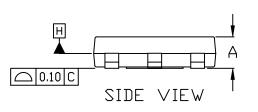
Figure 13. FET Thermal Response

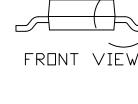


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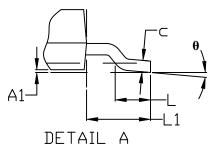
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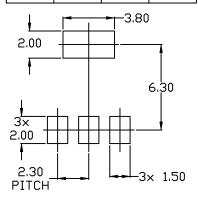
SEE DETAIL A



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
- 4. DATUMS A AND B ARE DETERMINED AT DATUM H.
- 5. ALLIS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS 6 AND 61.

	MILLIMETERS			
DIM	MIN.	N□M.	MAX.	
Α	1.50	1.63	1.75	
A1	0.02	0.06	0.10	
b	0.60	0.75	0.89	
b1	2.90 3.06		3.20	
c	0.24	0.29	0.35	
D	6.30	6.50	6.70	
E	3.30	3.50	3.70	
е	2.30 BSC			
L	0.20			
L1	1.50	1.75	2.00	
He	6.70	7.00	7.30	
θ	0*		10°	



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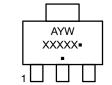
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**DATE 02 OCT 2018** 

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	4. DHAIN STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

## GENERIC MARKING DIAGRAM\*



A = Assembly Location

Y = Year W = Work Week

XXXXX = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)
\*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "•", may
or may not be present. Some products may
not follow the Generic Marking.

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