

NTZD3155C

MOSFET – Small Signal, Complementary with ESD Protection, SOT-563

20 V, 540 mA / -430 mA



ON Semiconductor®

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Features

- Leading Trench Technology for Low $R_{DS(on)}$ Performance
- High Efficiency System Performance
- Low Threshold Voltage
- ESD Protected Gate
- Small Footprint 1.6 x 1.6 mm
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC-DC Conversion Circuits
- Load/Power Switching with Level Shift
- Single or Dual Cell Li-Ion Battery Operated Systems
- High Speed Circuits
- Cell Phones, MP3s, Digital Cameras, and PDAs

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

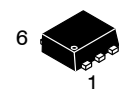
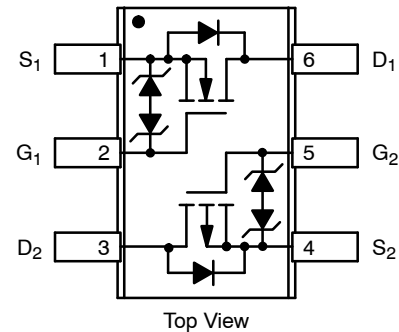
Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	20	V
Gate-to-Source Voltage			V_{GS}	± 6	V
N-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	540	mA
		$T_A = 85^\circ\text{C}$		390	
P-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$		-430	
		$T_A = 85^\circ\text{C}$		-310	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	250	mW
				$t \leq 5 \text{ s}$	
Pulsed Drain Current	N-Channel	$t_p = 10 \mu\text{s}$	I_{DM}	1500	mA
	P-Channel			-750	
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	350	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq [1 oz] including traces).

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max (Note 1)
N-Channel 20 V	0.4 Ω @ 4.5 V	540 mA
	0.5 Ω @ 2.5 V	
	0.7 Ω @ 1.8 V	
P-Channel -20 V	0.5 Ω @ -4.5 V	-430 mA
	0.6 Ω @ -2.5 V	
	1.0 Ω @ -1.8 V	

PINOUT: SOT-563



SOT-563-6
CASE 463A

MARKING DIAGRAM



TW = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTZD3155CT1G	SOT-563 (Pb-Free)	4000 / Tape & Reel
NTZD3155CT2G		
NTZD3155CT5G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Thermal Resistance Ratings

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	500	$^{\circ}C/W$
Junction-to-Ambient – $t = 5$ s (Note 2)		447	

2. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	N/P	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0$ V	$I_D = 250$ μ A	20		V
		P		$I_D = -250$ μ A	-20		
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				18		$mV/^{\circ}C$
Zero Gate Voltage Drain Current	I_{DSS}	N	$V_{GS} = 0$ V, $V_{DS} = 16$ V	$T_J = 25^{\circ}C$		1.0	μ A
		P	$V_{GS} = 0$ V, $V_{DS} = -16$ V			-1.0	
		N	$V_{GS} = 0$ V, $V_{DS} = 16$ V	$T_J = 125^{\circ}C$		2.0	μ A
		P	$V_{GS} = 0$ V, $V_{DS} = -16$ V			-5.0	
Gate-to-Source Leakage Current	I_{GSS}	P	$V_{DS} = 0$ V, $V_{GS} = \pm 4.5$ V			± 2.0	μ A
		N				± 5.0	

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250$ μ A	0.45		1.0	V
		P		$I_D = -250$ μ A	-0.45		-1.0	
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$					-1.9		$-mV/^{\circ}C$
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5$ V, $I_D = 540$ mA			0.4	0.55	Ω
		P	$V_{GS} = -4.5$ V, $I_D = -430$ mA			0.5	0.9	
		N	$V_{GS} = 2.5$ V, $I_D = 500$ mA			0.5	0.7	
		P	$V_{GS} = -2.5$ V, $I_D = -300$ mA			0.6	1.2	
		N	$V_{GS} = 1.8$ V, $I_D = 350$ mA			0.7	0.9	
		P	$V_{GS} = -1.8$ V, $I_D = -150$ mA			1.0	2.0	
Forward Transconductance	g_{FS}	N	$V_{DS} = 10$ V, $I_D = 540$ mA			1.0		S
		P	$V_{DS} = -10$ V, $I_D = -430$ mA			1.0		

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	N	$f = 1$ MHz, $V_{GS} = 0$ V $V_{DS} = 16$ V		80	150	pF
Output Capacitance	C_{OSS}				13	25	
Reverse Transfer Capacitance	C_{RSS}				10	20	
Input Capacitance	C_{ISS}	P	$f = 1$ MHz, $V_{GS} = 0$ V $V_{DS} = -16$ V		105	175	
Output Capacitance	C_{OSS}				15	30	
Reverse Transfer Capacitance	C_{RSS}				10	20	

3. Pulse Test: pulse width ≤ 300 μ s, duty cycle $\leq 2\%$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	N/P	Test Condition	Min	Typ	Max	Unit
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CHARGES, CAPACITANCES AND GATE RESISTANCE

Total Gate Charge	Q _{G(TOT)}	N	V _{GS} = 4.5 V, V _{DS} = -10 V; I _D = 540 mA		1.5	2.5	nC
Threshold Gate Charge	Q _{G(TH)}				0.1		
Gate-to-Source Charge	Q _{GS}				0.2		
Gate-to-Drain Charge	Q _{GD}				0.35		
Total Gate Charge	Q _{G(TOT)}	P	V _{GS} = -4.5 V, V _{DS} = 10 V; I _D = -380 mA		1.7	2.5	
Threshold Gate Charge	Q _{G(TH)}				0.1		
Gate-to-Source Charge	Q _{GS}				0.3		
Gate-to-Drain Charge	Q _{GD}				0.4		

SWITCHING CHARACTERISTICS (V_{GS} = V) (Note 4)

Turn-On Delay Time	t _{d(ON)}	N	V _{GS} = 4.5 V, V _{DD} = -10 V, I _D = 540 mA, R _G = 10 Ω		6.0		ns
Rise Time	t _r				4.0		
Turn-Off Delay Time	t _{d(OFF)}				16		
Fall Time	t _f				8.0		
Turn-On Delay Time	t _{d(ON)}	P	V _{GS} = -4.5 V, V _{DD} = 10 V, I _D = -215 mA, R _G = 10 Ω		10		
Rise Time	t _r				12		
Turn-Off Delay Time	t _{d(OFF)}				35		
Fall Time	t _f				19		

Drain-Source Diode Characteristics

Forward Diode Voltage	V _{SD}	N	V _{GS} = 0 V, T _J = 25°C	I _S = 350 mA		0.7	1.2	V
		P		I _S = -350 mA		-0.8	-1.2	
Reverse Recovery Time	t _{RR}	N	V _{GS} = 0 V, dI _S /dt = 100 A/μs	I _S = 350 mA		6.5		ns
		P		I _S = -350 mA		13		

4. Switching characteristics are independent of operating junction temperatures

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N-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

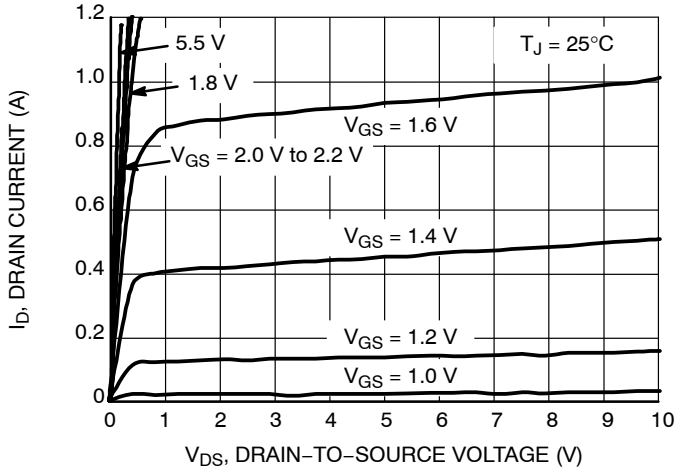


Figure 1. On-Region Characteristics

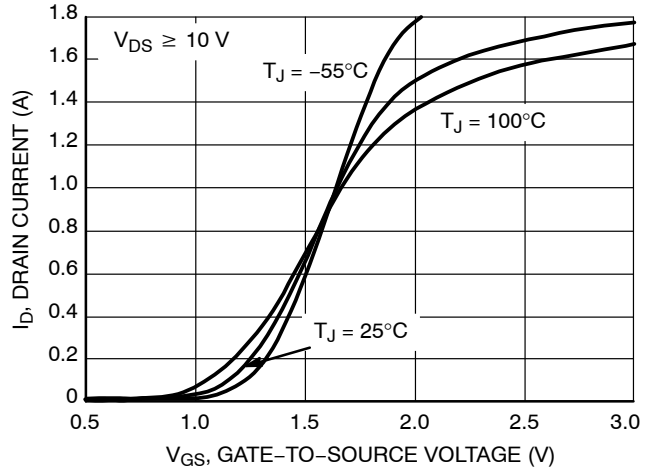


Figure 2. Transfer Characteristics

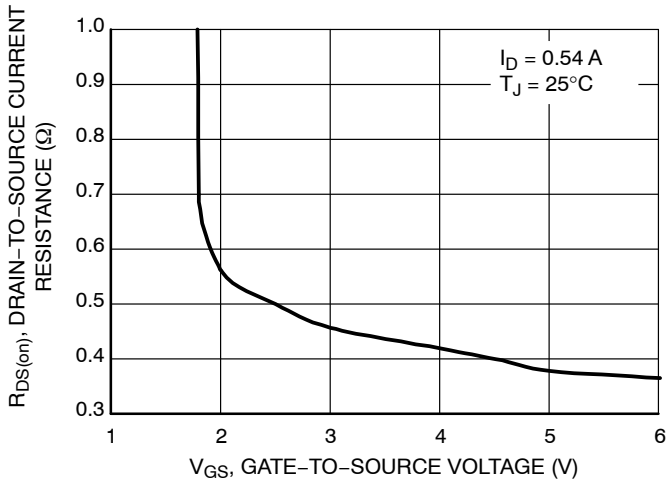


Figure 3. On-Resistance versus Gate-to-Source Voltage

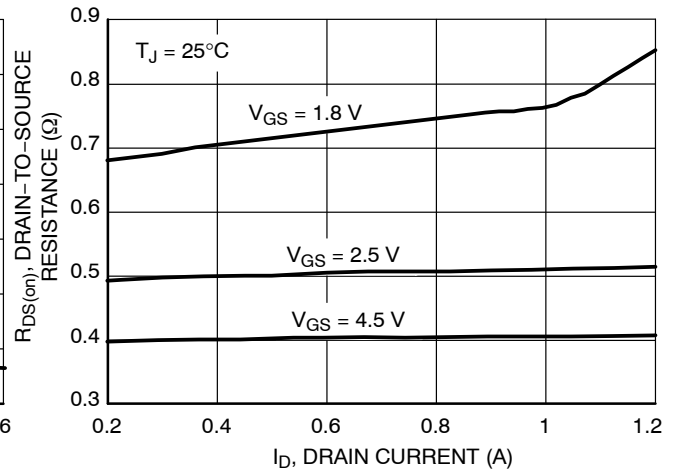


Figure 4. On-Resistance versus Drain Current and Gate Voltage

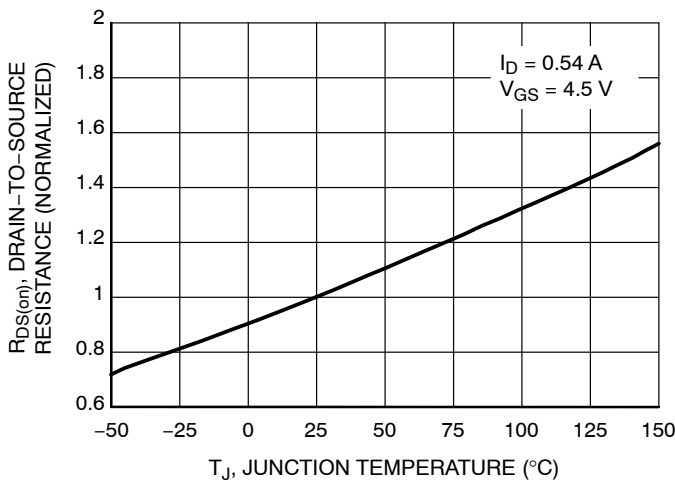


Figure 5. On-Resistance Variation with Temperature

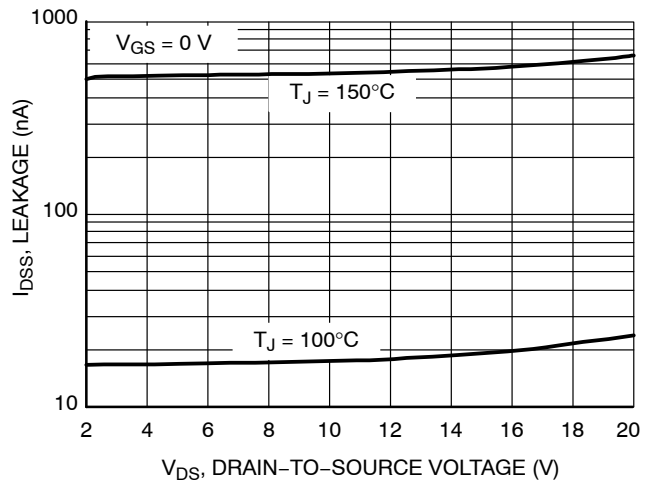


Figure 6. Drain-to-Source Leakage Current versus Voltage

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N-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

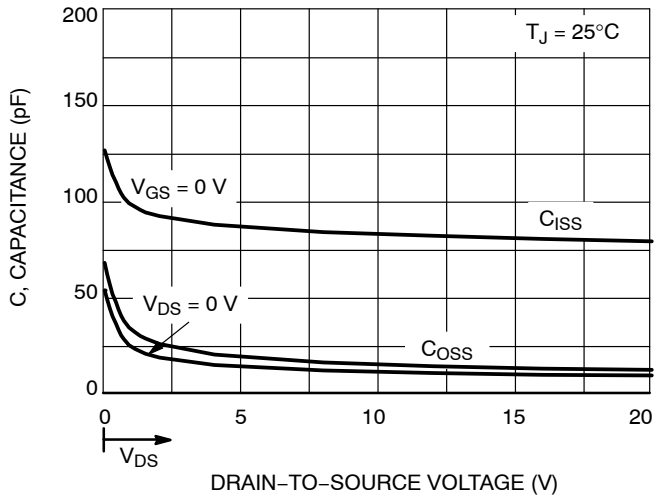


Figure 7. Capacitance Variation

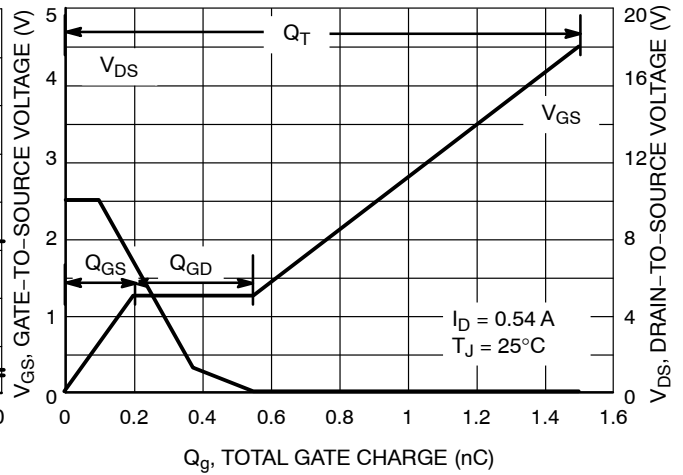


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

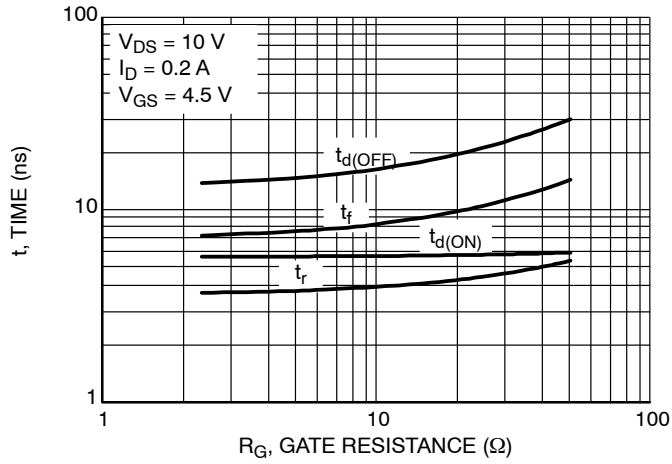


Figure 9. Resistive Switching Time Variation versus Gate Resistance

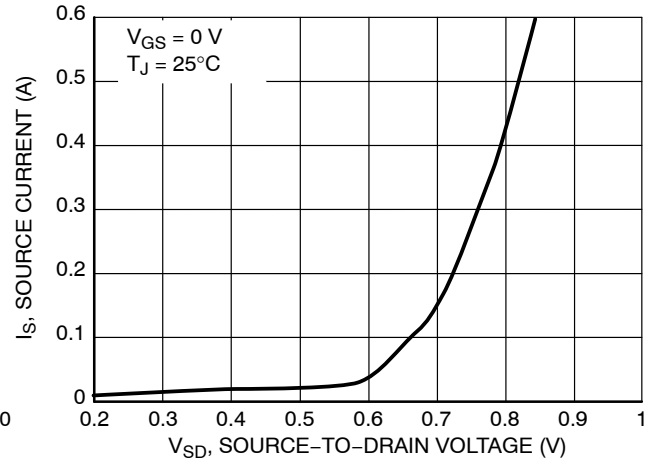


Figure 10. Diode Forward Voltage versus Current

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P-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

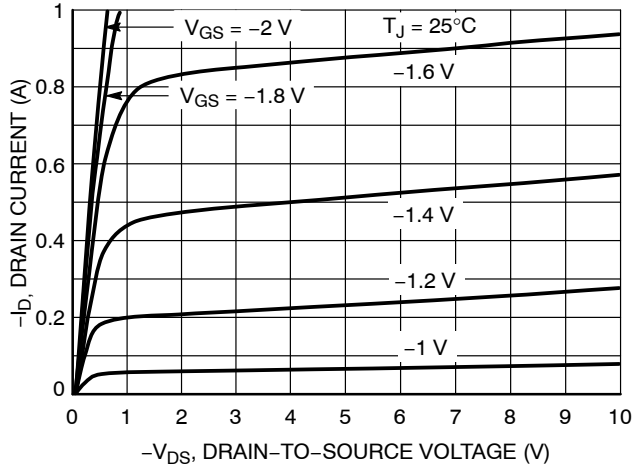


Figure 1. On-Region Characteristics

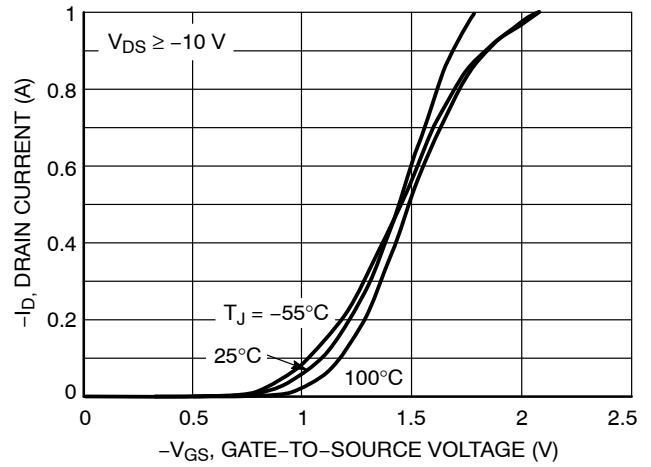


Figure 2. Transfer Characteristics

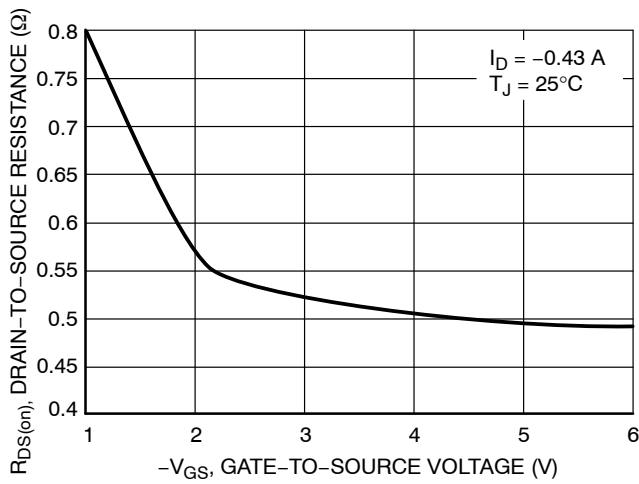


Figure 3. On-Resistance vs. Gate-to-Source Voltage

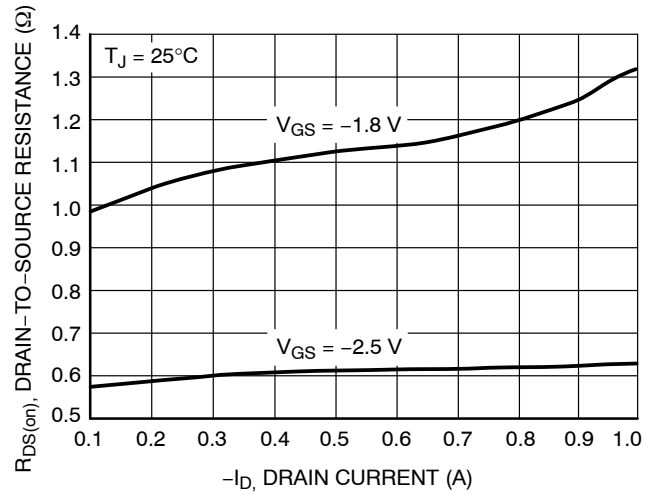


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

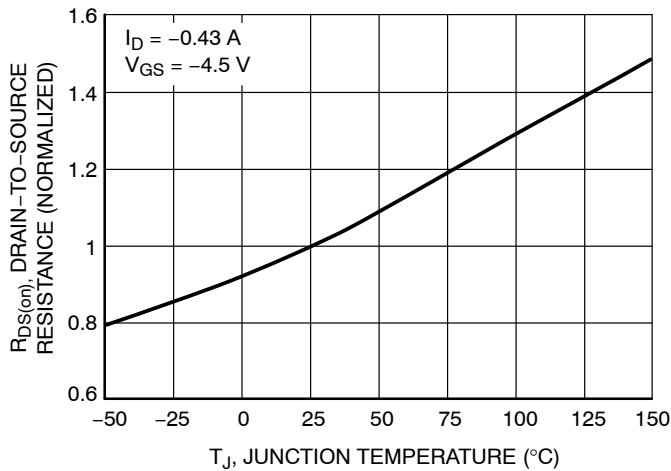


Figure 5. On-Resistance Variation with Temperature

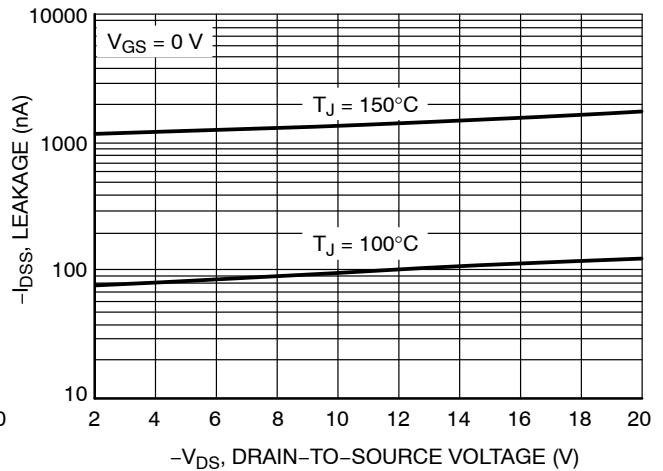


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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P-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

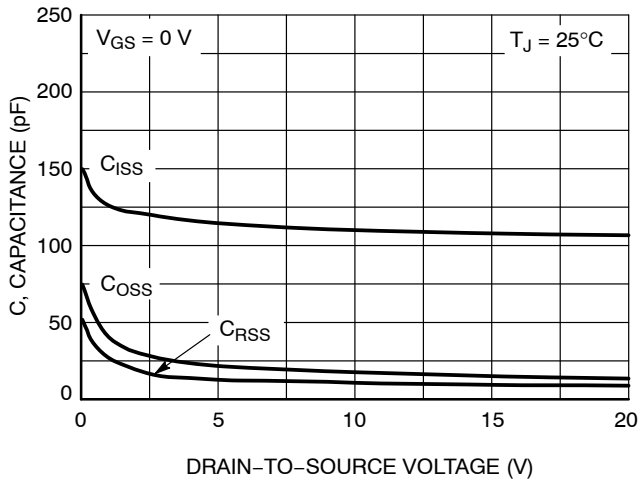


Figure 7. Capacitance Variation

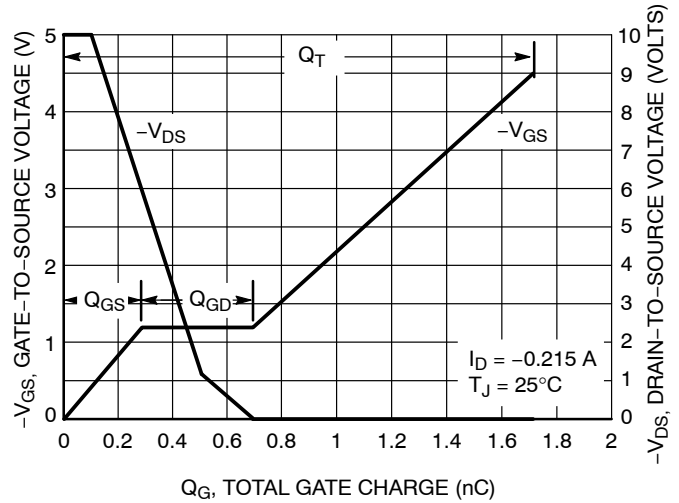


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

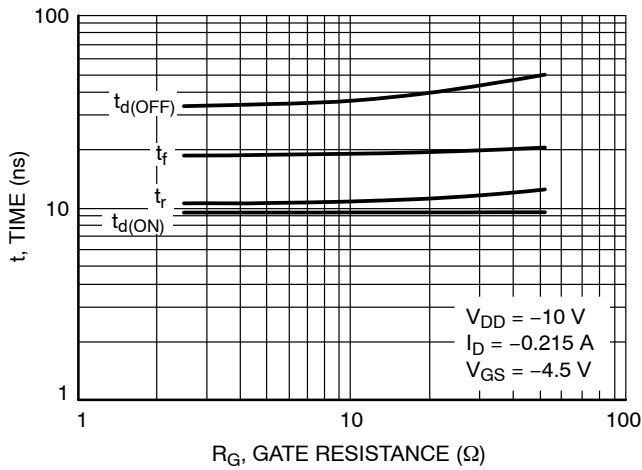


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

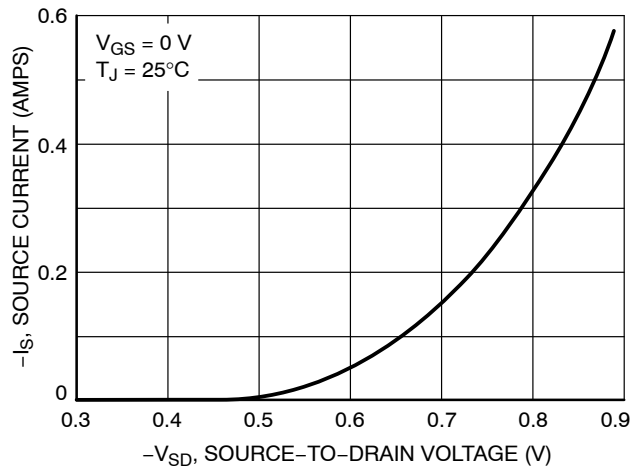


Figure 10. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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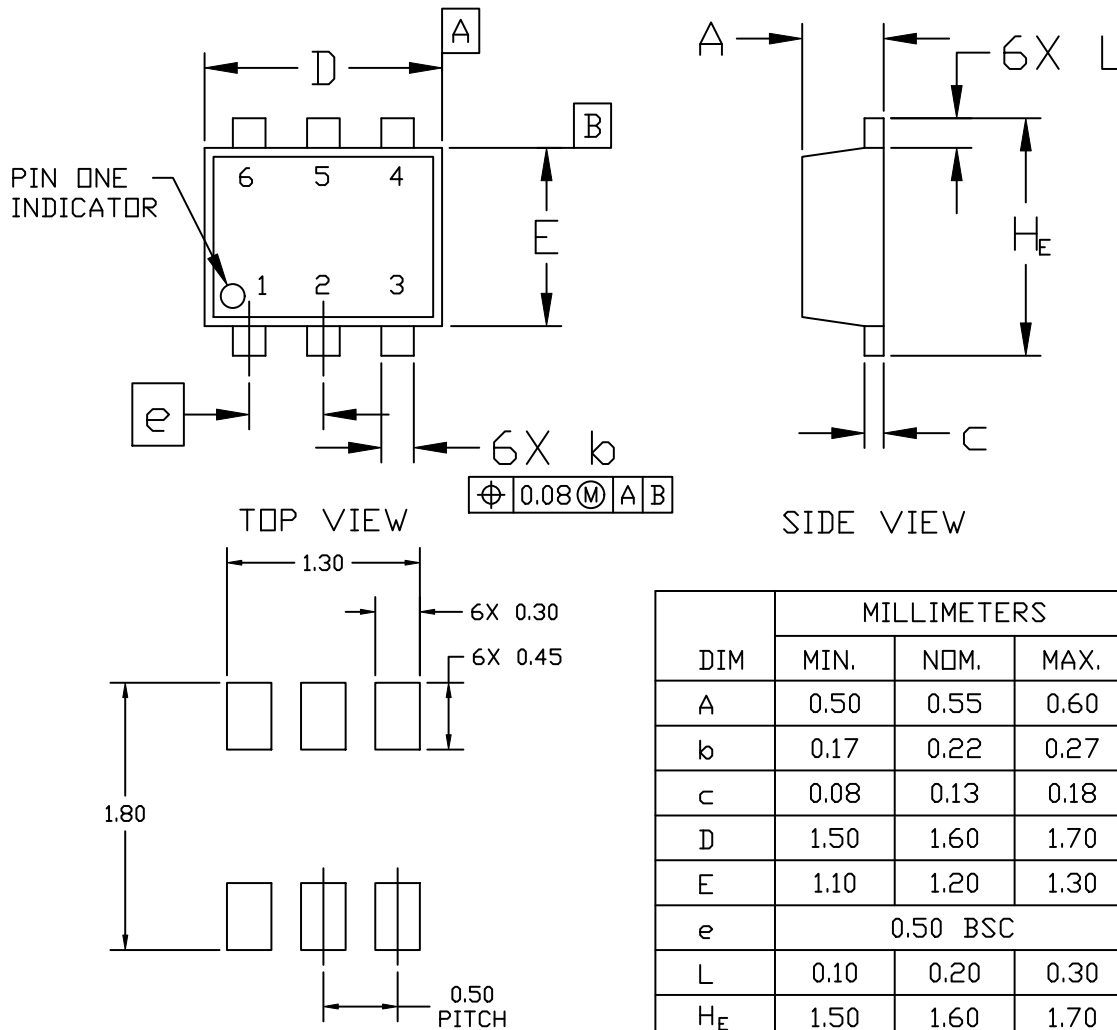
SCALE 4:1

SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
L	0.10	0.20	0.30
H _E	1.50	1.60	1.70

RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

**GENERIC
MARKING DIAGRAM***



XX = Specific Device Code
M = Month Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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