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# 74AUP1G97

## TinyLogic® Low Power Universal Configurable Two-Input Logic Gate

### Features

- 0.8V to 3.6V  $V_{CC}$  Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at  $V_{CC}$  from 0.8V to 3.6V
- High Speed  $t_{PD}$ 
  - 3.1ns: Typical at 3.3V
- Power-Off High-Impedance Inputs and Outputs
- Low Static Power Consumption
  - $I_{CC}$ =0.9 $\mu$ A Maximum
- Low Dynamic Power Consumption
  - $C_{PD}$ =2.5pF Typical at 3.3V
- Ultra-Small MicroPak™ Packages

### Description

The 74AUP1G97 is a universal configurable 2-input logic gate that provides a high performance and low power solution ideal for battery-powered portable applications. This product is designed for a wide low voltage operating range (0.8V to 3.6V) and guarantees very low static and dynamic power consumption across the entire voltage range. All inputs are implemented with hysteresis to allow for slower transition input signals and better switching noise immunity.

The 74AUP1G97 provides for multiple functions as determined by various configurations of the three inputs. The potential logic functions provided are MUX, AND, OR, NAND, and NOR, inverter and buffer. Refer to Figures 3 to 9.

### Ordering Information

Part Number	Top Mark	Package	Packing Method
74AUP1G97L6X	AD	6-Lead MicroPak™, 1.0mm Wide	5000 Units on Tape & Reel
74AUP1G97FHX	AD	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

### Logic Diagram

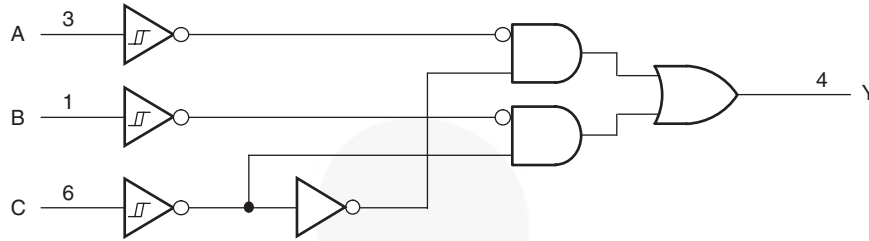


Figure 1. Logic Diagram (Positive Logic)

### Pin Configurations

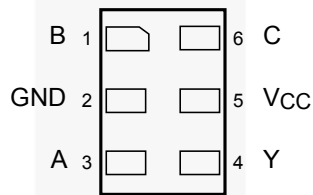


Figure 2. MicroPak™ (Top Through View)

### Pin Definitions

Pin #	Name	Description
1	B	Data Input
2	GND	Ground
3	A	Data Input
4	Y	Output
5	V <sub>CC</sub>	Supply Voltage
6	C	Data Input

**Function Table**

Inputs			74AUP1G97
C	B	A	Y=Output
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

H = HIGH Logic Level

L = LOW Logic Level

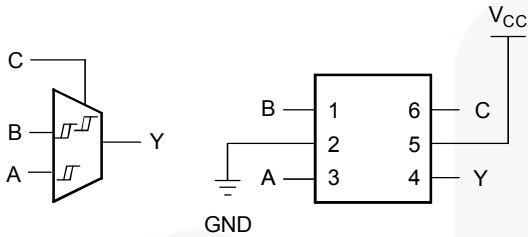
**Function Selection Table**

2-Input Logic Function	Connection Configuration
2-to-1 MUX	Figure 3
2-Input AND Gate	Figure 4
2-Input OR Gate with One Inverted Input	Figure 5
2-Input NAND Gate with One Inverted Input	Figure 5
2-Input AND Gate with One Inverted Input	Figure 6
2-Input NOR Gate with One Inverted Input	Figure 6
2-Input OR Gate	Figure 7
Inverter	Figure 8
Buffer	Figure 9

## 74AUP1G97 Logic Configurations

Figure 3 through Figure 9 show the logical functions that can be implemented using the 74AUP1G97. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical

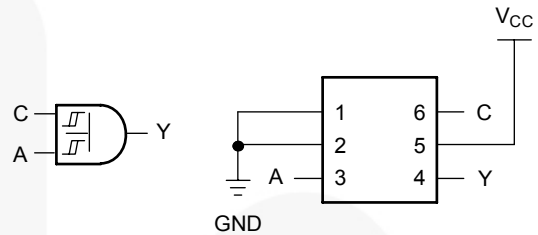
implementation is next to the board-level physical implementation of how the pins of the function should be connected.



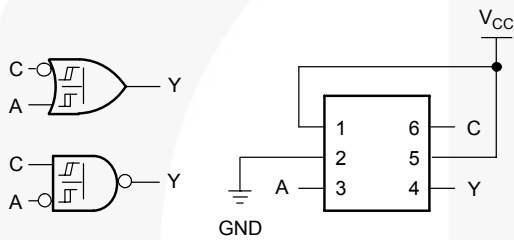
**Note:**

1. When C is L, Y=B.
2. When C is H, Y=A.

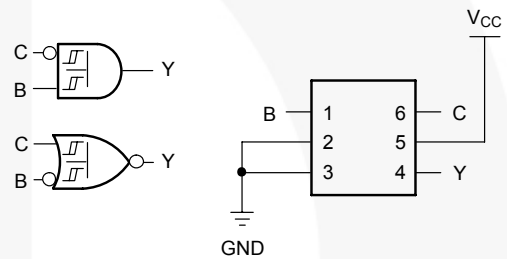
**Figure 3. 2-to-1 MUX**



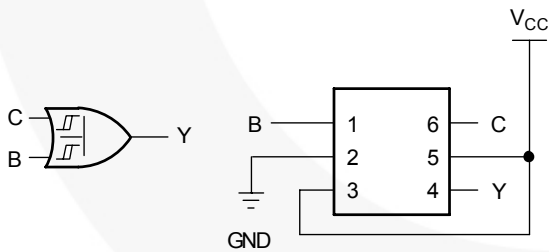
**Figure 4. 2-Input AND Gate**



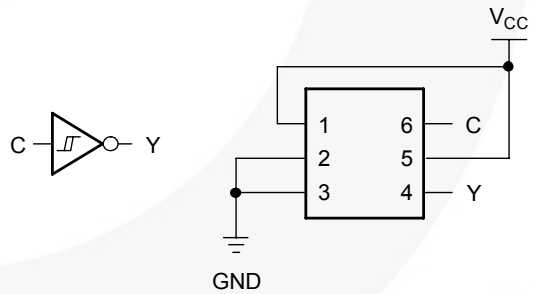
**Figure 5. Input OR Gate with One Inverted Input  
2-Input NAND Gate with One Inverted Input**



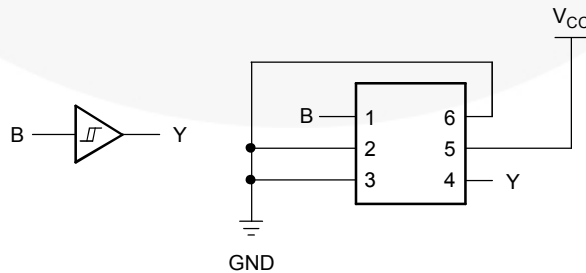
**Figure 6. 2-Input AND Gate with One Inverted Input  
2-Input NOR Gate with One Inverted Input**



**Figure 7. 2-Input OR Gate**



**Figure 8. Inverter**



**Figure 9. Buffer**

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	-0.5	4.6	V
$V_{IN}$	DC Input Voltage	-0.5	4.6	V
$V_{OUT}$	DC Output Voltage	HIGH or LOW State <sup>(3)</sup>	$V_{CC} + 0.5$	V
		$V_{CC}=0V$	4.6	
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0V$	-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < 0V$	-50	mA
		$V_{OUT} > V_{CC}$	+50	
$I_{OH} / I_{OL}$	DC Output Source / Sink Current		±50	mA
$I_o$	Continuous Output Current		±20	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Supply Pin		±50	mA
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$T_J$	Junction Temperature Under Bias		+150	°C
$T_L$	Junction Lead Temperature, Soldering 10s		+260	°C
$P_D$	Power Dissipation at +85°C	MicroPak-6	130	mW
		MicroPak2-6	120	
ESD	Human Body Model, JEDEC:JESD22-A114		5000+	V
	Charged Device Model, JEDEC:JESD22-C101		1500	

### Note:

3.  $I_o$  absolute maximum rating must be observed.

## Recommended Operating Conditions<sup>(4)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage		0.8	3.6	V
$V_{IN}$	Input Voltage		0	3.6	V
$V_{OUT}$	Output Voltage	$V_{CC}=0V$	0	3.6	V
		HIGH or LOW State	0	$V_{CC}$	
$I_{OH}/I_{OL}$	Output Current	$V_{CC}=3.0V$ to 3.6V		±4.0	mA
		$V_{CC}=2.3V$ to 2.7V		±3.1	
		$V_{CC}=1.65V$ to 1.95V		±1.9	
		$V_{CC}=1.4V$ to 1.6V		±1.7	
		$V_{CC}=1.1V$ to 1.3V		±1.1	
		$V_{CC}=0.8V$		±20.0	µA
$T_A$	Operating Temperature, Free Air		-40	+85	°C
$\theta_{JA}$	Thermal Resistance	MicroPak-6		500	°C/W
		MicroPak2-6		560	


### Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =+25°C		T <sub>A</sub> =-40 to +85°C		Units
				Min.	Max.	Min.	Max.	
V <sub>P</sub>	Positive Threshold Voltage	0.80		0.30	0.60	0.30	0.60	V
		1.10		0.53	0.90	0.53	0.90	
		1.40		0.74	1.11	0.74	1.11	
		1.65		0.91	1.29	0.91	1.29	
		2.30		1.37	1.77	1.37	1.77	
		3.00		1.88	2.29	1.88	2.29	
V <sub>N</sub>	Negative Threshold Voltage	0.80		0.10	0.60	0.10	0.60	V
		1.10		0.26	0.65	0.26	0.65	
		1.40		0.39	0.75	0.39	0.75	
		1.65		0.47	0.84	0.47	0.84	
		2.30		0.69	1.04	0.69	1.04	
		3.00		0.88	1.24	0.88	1.24	
V <sub>H</sub>	Hysteresis Voltage	0.80		0.07	0.50	0.07	0.50	V
		1.10		0.08	0.46	0.08	0.46	
		1.40		0.18	0.56	0.18	0.56	
		1.65		0.27	0.66	0.27	0.66	
		2.30		0.53	0.92	0.53	0.92	
		3.00		0.79	1.31	0.79	1.31	
V <sub>OH</sub>	HIGH Level Output Voltage	0.80 ≤ V <sub>CC</sub> ≤ 3.60	I <sub>OH</sub> =-20μA	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		V
		1.10 ≤ V <sub>CC</sub> ≤ 1.30	I <sub>OH</sub> =-1.1mA	0.75 x V <sub>CC</sub>		0.70 x V <sub>CC</sub>		
		1.40 ≤ V <sub>CC</sub> ≤ 1.60	I <sub>OH</sub> =-1.7mA	1.11		1.03		
		1.65 ≤ V <sub>CC</sub> ≤ 1.95	I <sub>OH</sub> =-1.9mA	1.32		1.30		
		2.30 ≤ V <sub>CC</sub> ≤ 2.70	I <sub>OH</sub> =-2.3mA	2.05		1.97		
			I <sub>OH</sub> =-3.1mA	1.90		1.85		
		3.00 ≤ V <sub>CC</sub> ≤ 3.60	I <sub>OH</sub> =-2.7mA	2.72		2.67		
V <sub>OL</sub>	LOW Level Output Voltage	0.80 ≤ V <sub>CC</sub> ≤ 3.60	I <sub>OL</sub> =20μA		0.10		0.10	V
		1.10 ≤ V <sub>CC</sub> ≤ 1.30	I <sub>OL</sub> =1.1mA		0.30 x V <sub>CC</sub>		0.30 x V <sub>CC</sub>	
		1.40 ≤ V <sub>CC</sub> ≤ 1.60	I <sub>OL</sub> =1.7mA		0.31		0.37	
		1.65 ≤ V <sub>CC</sub> ≤ 1.95	I <sub>OL</sub> =1.9mA		0.31		0.35	
		2.30 ≤ V <sub>CC</sub> ≤ 2.70	I <sub>OL</sub> =2.3mA		0.31		0.33	
			I <sub>OL</sub> =3.1mA		0.44		0.45	
		2.70 ≤ V <sub>CC</sub> ≤ 3.60	I <sub>OL</sub> =2.7mA		0.31		0.33	
	I <sub>OL</sub> =4.0mA		0.44		0.45			
I <sub>IN</sub>	Input Leakage Current	0V to 3.6V	0 ≤ V <sub>IN</sub> ≤ 3.6		±0.1		±0.5	μA
I <sub>OFF</sub>	Power Off Leakage Current	0V	0 ≤ (V <sub>IN</sub> , V <sub>O</sub> ) ≤ 3.6		0.2		0.6	μA
ΔI <sub>OFF</sub>	Additional Power Off Leakage Current	0V to 0.2V	V <sub>IN</sub> or V <sub>O</sub> = 0V to 3.6V		0.2		0.6	μA
I <sub>CC</sub>	Quiescent Supply Current	0.8V to 3.6V	V <sub>IN</sub> - V <sub>CC</sub> or GND		0.5		0.9	μA
			V <sub>CC</sub> ≤ V <sub>IN</sub> ≤ 3.6				±0.9	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	3.3V	V <sub>IN</sub> = V <sub>CC</sub> -0.6V		40.0		50.0	μA

### AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =+25°C			T <sub>A</sub> =-40 to +85°C		Units	Figure	
				Min.	Typ.	Max	Min	Max			
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	0.80	C <sub>L</sub> =5pF, R <sub>L</sub> =1MΩ		25.1				ns	Figure 10 Figure 11	
		1.10 ≤ V <sub>CC</sub> ≤ 1.30		2.8	8.6	12.6	2.5	13.0			
		1.40 ≤ V <sub>CC</sub> ≤ 1.60		2.3	5.2	7.6	2.5	8.2			
		1.65 ≤ V <sub>CC</sub> ≤ 1.95		2.1	4.3	6.2	2.0	6.8			
		2.30 ≤ V <sub>CC</sub> ≤ 2.70		1.9	3.3	4.8	1.7	5.3			
		3.00 ≤ V <sub>CC</sub> ≤ 3.60		1.6	3.1	3.9	1.5	4.1			
		0.80	C <sub>L</sub> =10pF, R <sub>L</sub> =1MΩ		29.4						
		1.10 ≤ V <sub>CC</sub> ≤ 1.30		3.2	9.4	14.3	2.9	14.9			
		1.40 ≤ V <sub>CC</sub> ≤ 1.60		2.6	6.3	8.7	2.8	9.4			
		1.65 ≤ V <sub>CC</sub> ≤ 1.95		2.2	4.9	7.0	2.1	7.8			
		2.30 ≤ V <sub>CC</sub> ≤ 2.70		2.0	4.2	5.2	2.1	5.9			
		3.00 ≤ V <sub>CC</sub> ≤ 3.60		1.9	3.6	4.6	1.7	4.9			
		0.80	C <sub>L</sub> =15pF, R <sub>L</sub> =1MΩ		31.3						
		1.10 ≤ V <sub>CC</sub> ≤ 1.30		3.6	9.6	16.0	3.2	16.7			
		1.40 ≤ V <sub>CC</sub> ≤ 1.60		2.9	6.3	9.6	3.1	10.4			
		1.65 ≤ V <sub>CC</sub> ≤ 1.95		2.4	5.4	7.8	2.3	8.7			
		2.30 ≤ V <sub>CC</sub> ≤ 2.70		2.3	4.7	5.8	2.1	6.5			
		3.00 ≤ V <sub>CC</sub> ≤ 3.60		2.0	4.0	5.1	1.8	5.5			
		0.80	C <sub>L</sub> =30pF, R <sub>L</sub> =1MΩ		32.1						
		1.10 ≤ V <sub>CC</sub> ≤ 1.30		3.4	9.5	18.5	3.4	19.0			
1.40 ≤ V <sub>CC</sub> ≤ 1.60	3.1	5.9		10.5	3.1	11.0					
1.65 ≤ V <sub>CC</sub> ≤ 1.95	1.8	4.8		8.7	1.8	9.5					
2.30 ≤ V <sub>CC</sub> ≤ 2.70	1.7	3.7		6.5	1.7	7.1					
3.00 ≤ V <sub>CC</sub> ≤ 3.60	1.3	3.1		5.6	1.3	6.3					
C <sub>IN</sub>	Input Capacitance	0			2.1			pF			
C <sub>OUT</sub>	Output Capacitance	0			3.0			pF			
C <sub>PD</sub>	Power Dissipation Capacitance	0.80	V <sub>IN</sub> =0V or V <sub>CC</sub> , f=10MHz		1.7				pF		
		1.10 ≤ V <sub>CC</sub> ≤ 1.30			1.8						
		1.40 ≤ V <sub>CC</sub> ≤ 1.60			1.81						
		1.65 ≤ V <sub>CC</sub> ≤ 1.95			1.84						
		2.30 ≤ V <sub>CC</sub> ≤ 2.70			2.1						
		3.00 ≤ V <sub>CC</sub> ≤ 3.60			2.5						



## AC Loadings and Waveforms

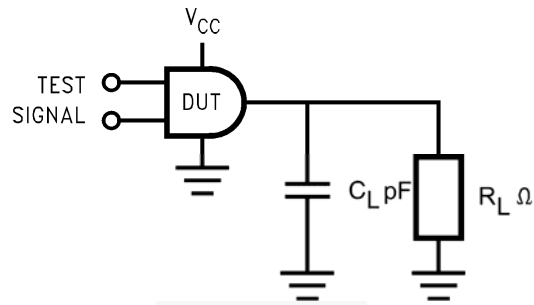


Figure 10. AC Test Circuit

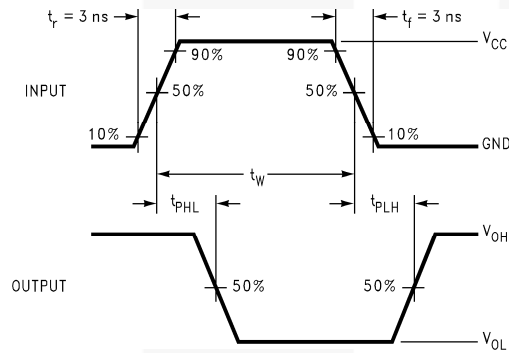
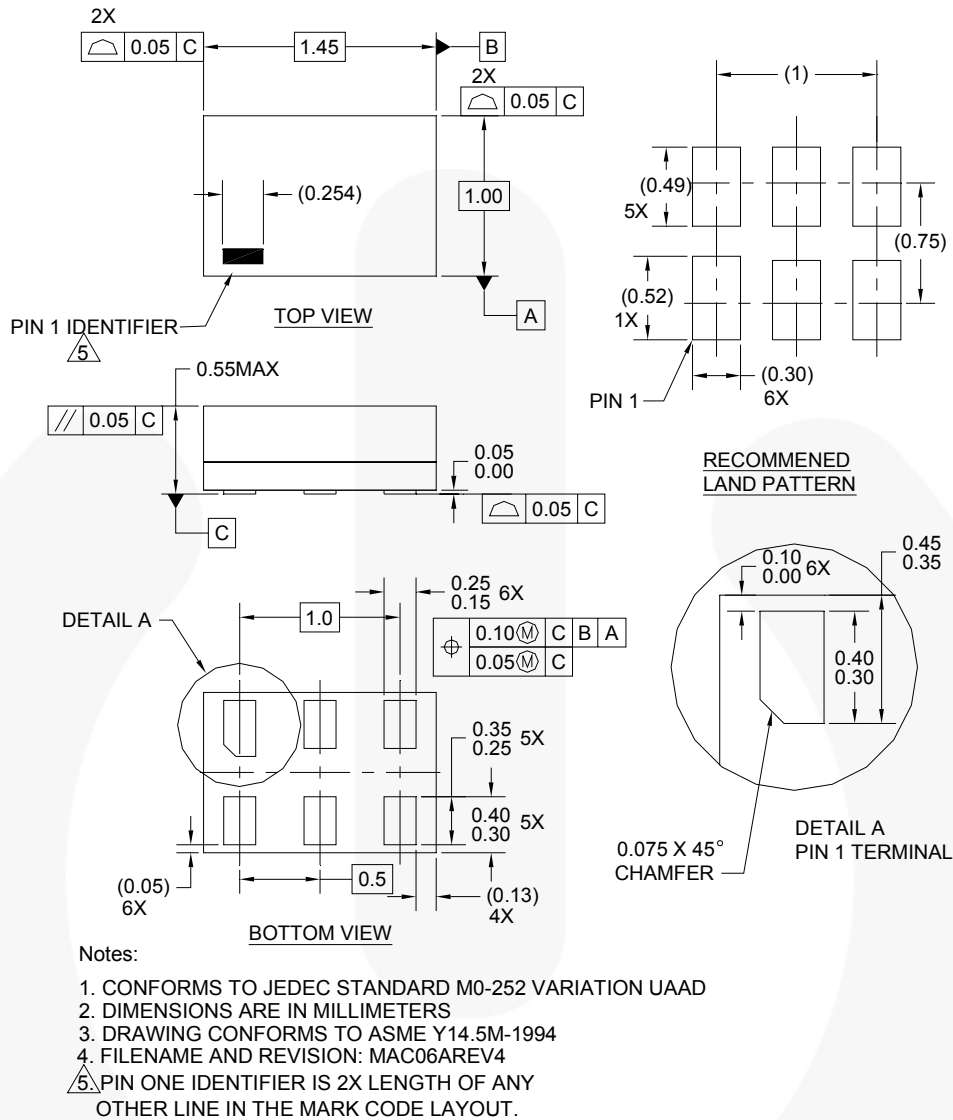


Figure 11. AC Waveforms

Symbol	$V_{CC}$					
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$	$1.5V \pm 0.10V$	$1.2V \pm 0.10V$	$0.8V$
$V_{mi}$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$

## Physical Dimensions



**Figure 12. 6-Lead, MicroPak™, 1.0mm Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

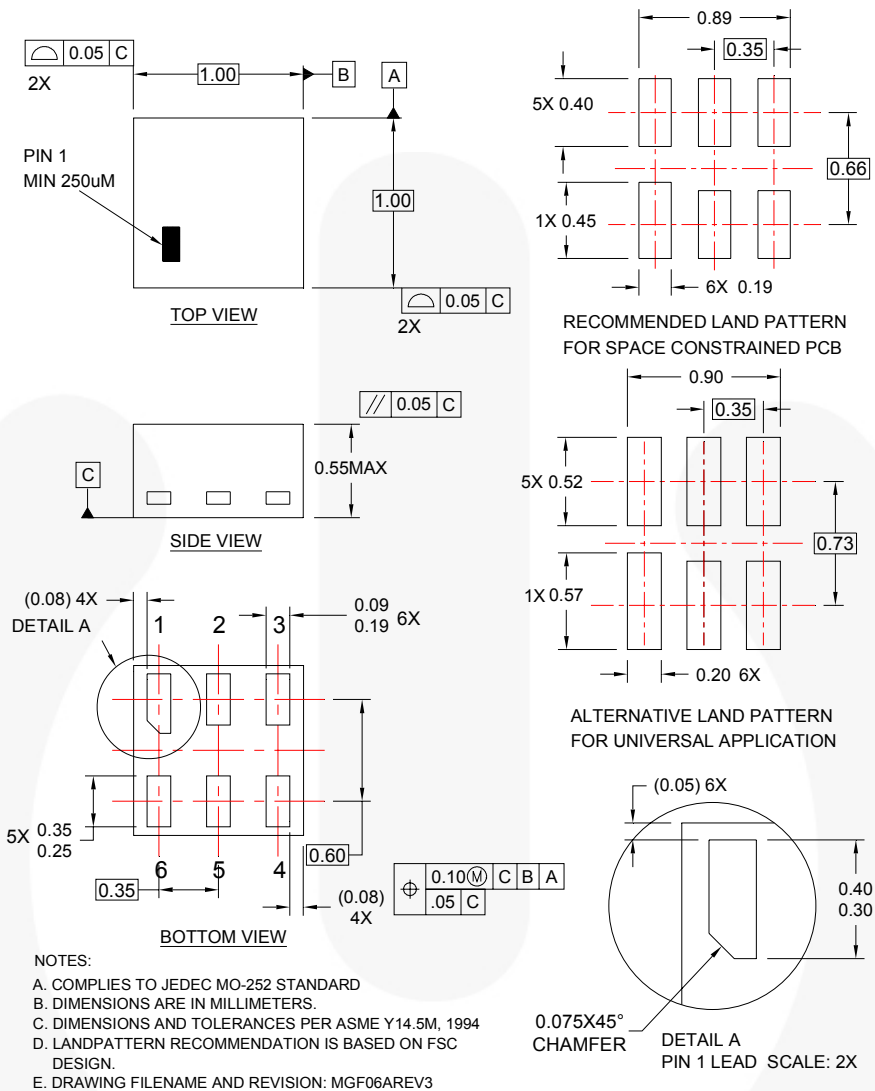
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## Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
[http://www.fairchildsemi.com/products/logic/pdf/micropak\\_tr.pdf](http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf)

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## Physical Dimensions



**Figure 13. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch**

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[http://www.fairchildsemi.com/packaging/MicroPAK2\\_6L\\_tr.pdf](http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf).

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed




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 Gmax™  
 GTO™  
 IntelliMAX™  
 ISOPLANAR™  
 MegaBuck™  
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 SuperSOT™.6  
 SuperSOT™.8  
 SupreMOS®  
 SyncFET™  
 Sync-Lock™

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 The Power Franchise®  
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