NLX2G04

Dual Inverter

The NLX2G04 MiniGate™ is an advanced high−speed CMOS dual inverter in ultra−small footprint.

The NLX2G04 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: t_{PD} = 1.8 ns (Typ) @ V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
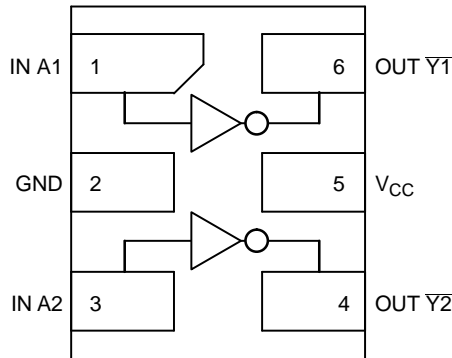- Ultra−Small Packages
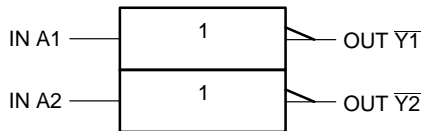- These are Pb−Free Devices

Figure 1. Pinout (Top View)

Figure 2. Logic Symbol

ON Semiconductor®

MARKING DIAGRAMS

ULLGA6 1.2 x 1.0 CASE 613AE	⊙M
UDFN6 1.0 x 1.0 CASE 517BX	∃M
UDFN6 1.2 x 1.0 CASE 517AA	⊓M
UDFN6 1.45 x 1.0 CASE 517AQ	2M

Q = Device Marking
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT $\overline{Y2}$
5	V_{CC}
6	OUT $\overline{Y1}$

FUNCTION TABLE

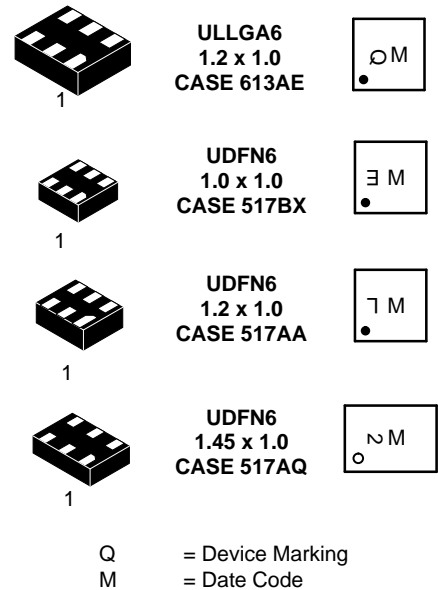| A	$\overline{Y}$
L	H
H	L

NLX2G04

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen	Index: 28 to 34	UL 94 V−0 @ 0.125 in	
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 2)		±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	Digital Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
T_A	Operating Free−Air Temperature		−55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ± 0.2 V V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0 0	20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NLX2G04

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	$T_A = +85°C$ Min	Max	$T_A = -55°C$ to +125°C Min	Max	Unit
V_{IH}	Low–Level Input Voltage		1.65–1.95	0.75 x V_{CC}			0.75 x V_{CC}		0.75 x V_{CC}		V
			2.3 to 5.5	0.70 x V_{CC}			0.70 x V_{CC}		0.70 x V_{CC}		
V_{IL}	Low–Level Input Voltage		1.65–1.95			0.25 x V_{CC}		0.25 x V_{CC}		0.25 x V_{CC}	V
			2.3 – 5.5			0.30 x V_{CC}		0.30 x V_{CC}		0.30 x V_{CC}	
V_{OH}	High–Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -100 \mu A$	1.65 – 5.5	V_{CC}−0.1	V_{CC}		V_{CC}−0.1		V_{CC}−0.1		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA $I_{OH} = -12$ mA $I_{OH} = -16$ mA $I_{OH} = -24$ mA $I_{OH} = -32$ mA	1.65 2.3 2.7 3.0 3.0 4.5	1.29 1.9 2.2 2.4 2.3 3.8	1.52 2.1 2.4 2.7 2.5 4.0		1.29 1.9 2.2 2.4 2.3 3.8		1.29 1.9 2.2 2.4 2.3 3.8		
V_{OL}	Low–Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 100 \mu A$	1.65 – 5.5			0.1		0.1		0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA $I_{OH} = -12$ mA $I_{OH} = -16$ mA $I_{OH} = -24$ mA $I_{OH} = -32$ mA	1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.2 0.22 0.28 0.38 0.42	0.24 0.3 0.4 0.4 0.55 0.55		0.24 0.3 0.4 0.4 0.55 0.55		0.24 0.3 0.4 0.4 0.55 0.55	
I_{IN}	Input Leakage Current	$0 \leq V_{IN} \leq 5.5$ V	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OFF}	Power–Off Output Leakage Current	V_{IN} or $V_{OUT} = 5.5$ V	0			1.0		10		10	μA
I_{CC}	Quiescent Supply Current	$0 \leq V_{IN} \leq V_{CC}$	5.5			1.0		10		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NLX2G04

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 nS)

Symbol	Parameter	V_{CC} (V)	Test Condition	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, Input A to Output $\overline{Y}$	1.65	R_L = 1 MΩ, C_L = 15 pF	1.8	2.3	9.2	1.8	11	ns
		1.8	R_L = 1 MΩ, C_L = 15 pF	1.8	4.4	7.6	1.2	8.4	
		2.3–2.7	R_L = 1 MΩ, C_L = 15 pF	1.2	3.0	5.1	1.2	5.6	
		3.0–3.6	R_L = 1 MΩ, C_L = 15 pF	0.8	2.2	3.4	0.8	3.8	
			R_L = 500 Ω, C_L = 50 pF	1.2	2.9	4.5	1.2	5.0	
		4.5–5.5	R_L = 1 MΩ, C_L = 15 pF	0.5	1.8	2.8	0.5	3.1	
			R_L = 500 Ω, C_L = 50 pF	0.8	2.3	3.6	0.8	4.0	
C_{IN}	Input Capacitance	5.5	V_{IN} = 0 V or V_{CC}		2.5				pF
C_{PD}	Power Dissipation Capacitance (Note 3)	3.3 5.5	10 MHz V_{IN} = 0 V or V_{CC}		9 11				pF

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)}$ = $C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.
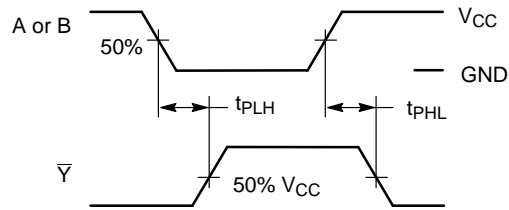
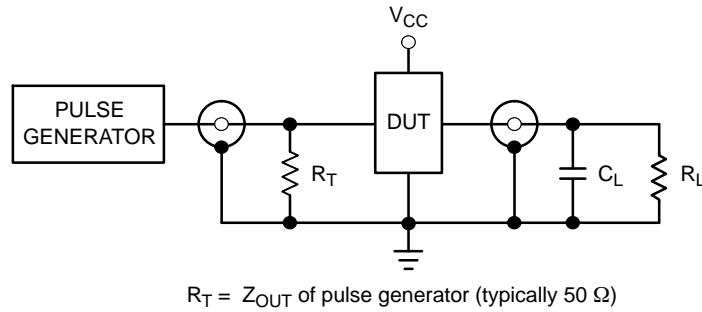# NLX2G04

Figure 3. Switching Waveforms

$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
NLX2G04BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb−Free)	3000 / Tape & Reel
NLX2G04MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb−Free)	3000 / Tape & Reel
NLX2G04AMUTCG	UDFN6, 1.45 x 1.0, 0.5P (Pb−Free)	3000 / Tape & Reel
NLX2G04CMUTCG	UDFN6, 1.0 x 1.0, 0.35P (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
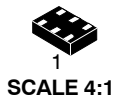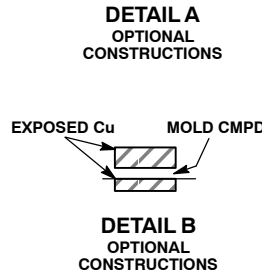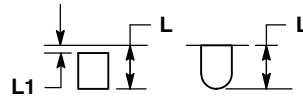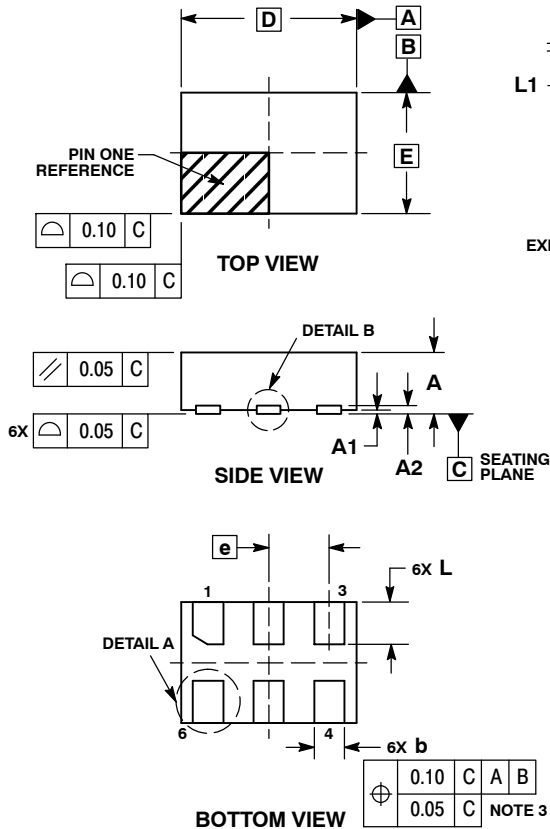
UDFN6, 1.45x1.0, 0.5P
CASE 517AQ–01
ISSUE O

DATE 15 MAY 2008

SCALE 4:1

1

TOP VIEW

PIN ONE REFERENCE

| ⌒ | 0.10 | C |

| ⌒ | 0.10 | C |

D — A
B
E

SIDE VIEW

DETAIL B

| ∥ | 0.05 | C |

6X | ⌒ | 0.05 | C |

A
A1
A2
C SEATING PLANE

DETAIL A
OPTIONAL CONSTRUCTIONS

L   L
L1

DETAIL B
OPTIONAL CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

BOTTOM VIEW

DETAIL A

e
6X L
1   3
6   4
6X b

| ⊕ | 0.10 | C | A | B |
| | 0.05 | C | NOTE 3 |

MOUNTING FOOTPRINT

PACKAGE OUTLINE

6X 0.30
1.24
6X 0.53
1
0.50 PITCH

DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

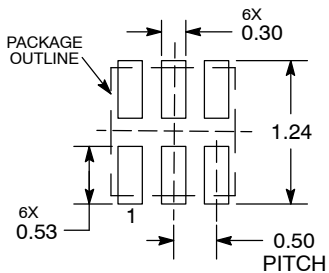| DIM | MILLIMETERS | |
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	–––	0.15

GENERIC MARKING DIAGRAM*

XM

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

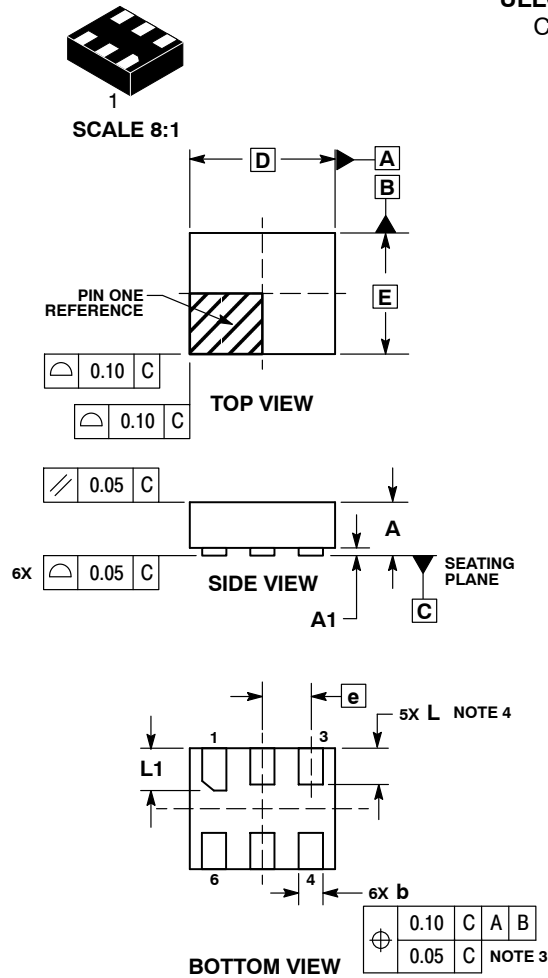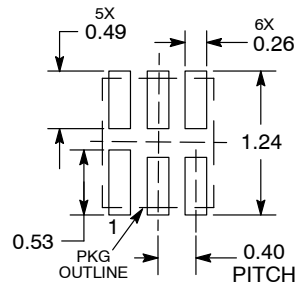| DOCUMENT NUMBER:	98AON30313E	
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	UDFN6, 1.45X1.0, 0.5P	PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY K. VAN TYNE.	15 MAY 2008

UDFN6, 1x1, 0.35P
CASE 517BX–01
ISSUE O

SCALE 4:1

DATE 18 MAY 2011

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

PIN ONE REFERENCE

2X 0.10 C

2X 0.10 C **TOP VIEW**

0.05 C

0.05 C **SIDE VIEW**

A3

A

A1

C SEATING PLANE

e

5X L

1 3

L1

6 4

6X b

⊕ 0.10 Ⓜ C A B
0.05 Ⓜ C NOTE 3

BOTTOM VIEW

GENERIC MARKING DIAGRAM*

X M

1 o

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*

5X
0.48

6X
0.22

1.18

0.53

1

0.35

PKG OUTLINE

PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	UDFN6, 1X1, 0.35P		PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY I. CAMBALIZA.	18 MAY 2011

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

ULLGA6, 1.2x1.0, 0.4P
CASE 613AE–01
ISSUE A

DATE 06 FEB 2008

SCALE 8:1

PIN ONE REFERENCE

TOP VIEW

0.10 | C

0.10 | C

0.05 | C

6X | 0.05 | C

SIDE VIEW

SEATING PLANE

A1 | C

A

e

5X **L** NOTE 4

L1

6X **b**

0.10 | C | A | B
0.05 | C | NOTE 3

BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
---	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

MOUNTING FOOTPRINT
SOLDERMASK DEFINED*

5X
0.49

6X
0.26

1.24

0.53

1

PKG OUTLINE

0.40
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	ULLGA6, 1.2X1.0, 0.4P		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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