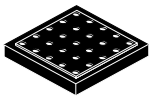
MT9V124

MT9V124 1/13-Inch System-On-A-Chip (SOC) CMOS Digital Image Sensor

ON Semiconductor®

www.onsemi.com



ODCSP25 2.694 × 2.694
CASE 570BN

GENERAL DESCRIPTION

ON Semiconductor's MT9V124 is a 1/13-inch CMOS digital image sensor with an active-pixel array of 648 (H) × 488 (V). It includes sophisticated camera functions such as auto exposure control, auto white balance, black level control, flicker detection and avoidance, and defect correction. It is designed for low light performance. It is programmable through a simple two-wire serial interface. The MT9V124 produces extraordinarily clear, sharp digital pictures that make it the perfect choice for a wide range of medical and industrial applications.

Table 1. KEY PARAMETERS

Parameter		Typical Value
Optical Format		1/13-inch
Active Pixels		648 × 488 = 0.3 Mp (VGA)
Pixel Size		1.75 µm
Color Filter Array		RGB Bayer
Shutter Type		Electronic Rolling Shutter (ERS)
Input Clock Range		18–44 MHz
Output	LVDS	12-bit Packet
Frame Rate, Full Resolution		30 fps
Responsivity		1.65 V/lux × sec
SNR_{MAX}		33.4 dB
Dynamic Range		58 dB
Supply Voltage	Analog	2.5–3.1 V
	Digital	1.7–1.95 V
	Digital I/O	1.7–1.95 V or 2.5–3.1 V
Power Consumption		55 mW
Operating Temperature (Ambient) $-T_A$		–30°C to +70°C
Chief Ray Angle		24°
Package Options		Bare die, CSP

Features

- Superior Low-light Performance
- Ultra-low-power
- VGA Video at 30fps
- Internal Master Clock Generated by On-chip Phase Locked Loop (PLL) Oscillator
- Electronic Rolling Shutter (ERS), Progressive Scan

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features (continued)

- Integrated Image Flow Processor (IFP) for Single-die Camera Module
- One-time Programmable Memory (OTPM)
- Automatic Image Correction and Enhancement, Including Four-channel Lens Shading Correction
- Image Scaling with Anti-aliasing
- Supports ITU-R BT.656 Format with Odd Timing Code
- Two-wire Serial Interface Providing Access to Registers and Microcontroller Memory
- Selectable Output Data Format: YCbCr, 565RGB, and RAW8+2-bit, BT656
- High Speed Serial Data Output in 12-bit Packet
- Independently Configurable Gamma Correction
- Direct XDMA Access (Reducing Serial Commands)
- Integrated Hue Rotation ±22°

Applications

- Medical Tools, Device
- Biometrics
- Industrial Application

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description †
MT9V124D00STCK22DC1−200	RGB color die	Die Sales, 200 μm Thickness
MT9V124EBKSTC−CR	CSP with 400 μm coverglass	Chip Tray without Protective Film

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FUNCTIONAL DESCRIPTION

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

ON Semiconductor's MT9V124 is a 1/13-inch VGA CMOS digital image sensor with an integrated advanced camera system. This camera system features a microcontroller (MCU), a sophisticated image flow processor (IFP), and a serial port (using LVDS signaling). The microcontroller manages all functions of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 648 × 488 pixels with programmable timing and control circuitry. It also includes an analog signal chain with automatic offset correction, programmable gain, and a 10-bit analog-to-digital converter (ADC).

The entire system-on-a-chip (SOC) has an ultra-low power operational mode and a superior low-light performance that is particularly suitable for medical applications. The MT9V124 features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Architecture Overview

The MT9V124 combines a VGA sensor core with an IFP to form a stand-alone solution for both image acquisition and processing. Both the sensor core and the IFP have internal registers that can be controlled by the user. In normal operation, an integrated microcontroller autonomously controls most aspects of operation. The processed image data is transmitted to the external host system through an LVDS bus. Figure 1 shows the major functional blocks of the MT9V124.

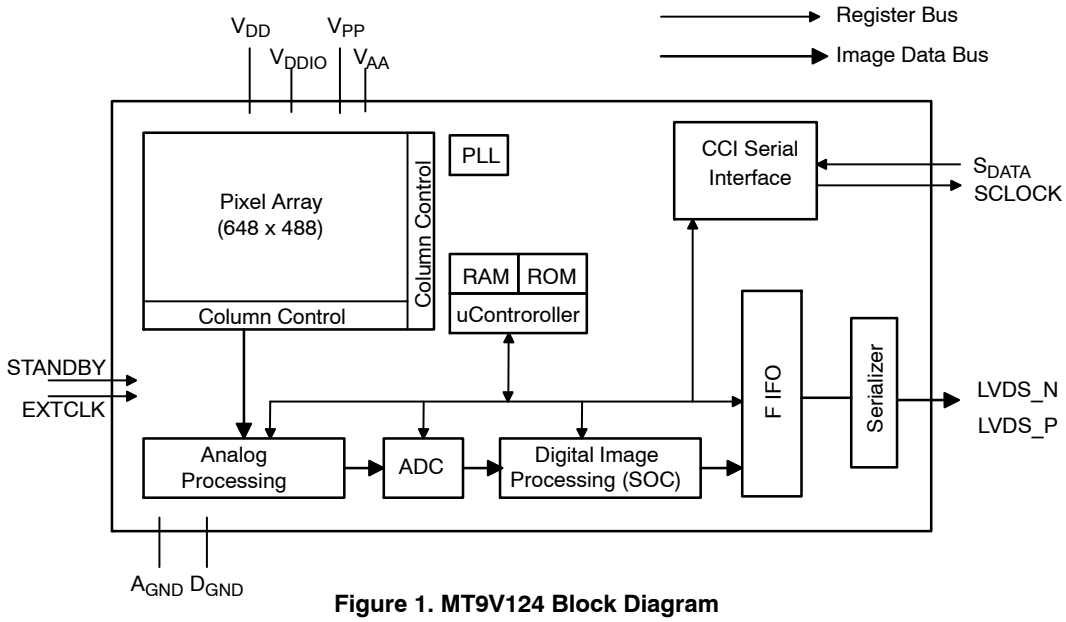


Figure 1. MT9V124 Block Diagram

Sensor Core

The MT9V124 has a color image sensor with a Bayer color filter arrangement and a VGA active-pixel array with electronic rolling shutter (ERS). The sensor core readout is 10 bits. The sensor core also supports separate analog and digital gain for all four color channels (R, Gr, Gb, B).

Image Flow Processor (IFP)

The advanced IFP features and flexible programmability of the MT9V124 can enhance and optimize the image sensor performance. Built-in optimization algorithms enable the MT9V124 to operate with factory settings as a fully automatic and highly adaptable system-on-a-chip (SOC) for most camera systems.

These algorithms include shading correction, defect correction, color interpolation, edge detection, color correction, aperture correction, and image formatting with cropping and scaling.

Microcontroller Unit (MCU)

The MCU communicates with all functional blocks by way of an internal ON Semiconductor proprietary bus interface. The MCU firmware executes the automatic control algorithms for exposure and white balance.

System Control

The MT9V124 has a phase-locked loop (PLL) oscillator that can generate the internal sensor clock from the common system clock. The PLL adjusts the incoming clock frequency up, allowing the MT9V124 to run at almost any desired resolution and frame rate within the sensor's capabilities.

Low-power consumption is a very important requirement for all components of wireless devices. The MT9V124 provides power-conserving features, including an internal soft standby mode and a hard standby mode.

A two-wire serial interface bus enables read and write access to the MT9V124's internal registers and variables. The internal registers control the sensor core, the color pipeline flow, the output interface, auto white balance (AWB) and auto exposure (AE).

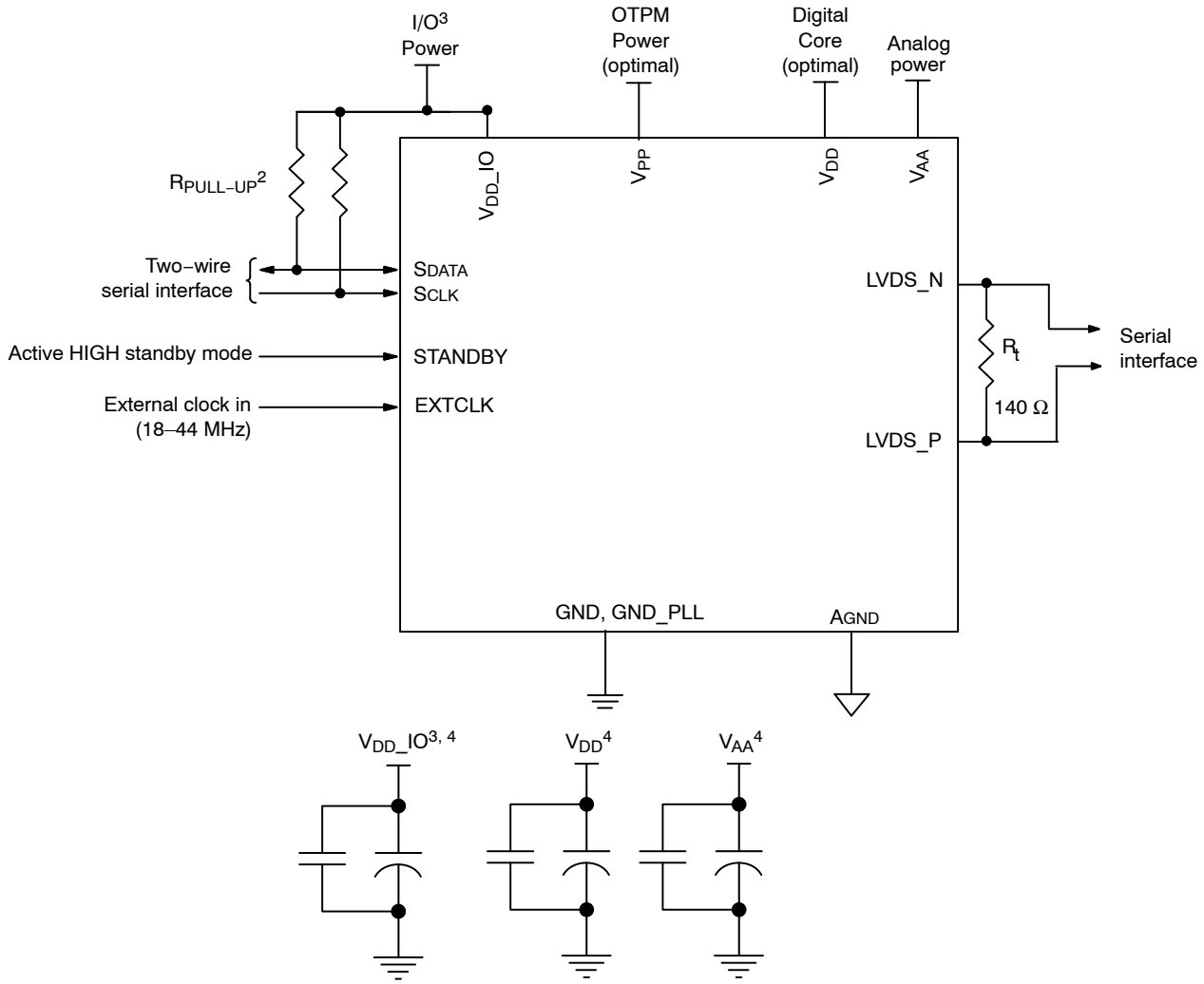
Output Interface

The output interface block can select either raw data or processed data. Image data is provided to the host system by an LVDS serial interface. The LVDS output port provides 8-bit YCbCr, YUV, 565 RGB, BT656, processed Bayer data or extended 10-bit Bayer data achieved using 8 + 2 format.

System Interfaces

Figure 2 shows typical MT9V124 device connections. For low-noise operation, the MT9V124 requires separate power supplies for analog and digital sections. Both power supply rails should be decoupled from ground using capacitors as close as possible to the die.

The MT9V124 provides dedicated signals for digital core and I/O power domains that can be at different voltages. The PLL and analog circuitry require clean power sources. Table 3, “Pin Descriptions,” provides the signal descriptions for the MT9V124.



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. ON Semiconductor recommends a 1.5 kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
3. All inputs must be configured with VDD_IO.
4. ON Semiconductor recommends that 0.1 μF and 1 μF decoupling capacitors for each power supply are mounted as close as possible to the module (Low-Z path). Actual values and numbers may vary depending on layout and design considerations, such as capacitor effective series resistance (ESR), dielectric, or power supply source impedance.
5. LVDS output requires termination resistor (140 Ω) to be placed closely at the sensor side.

Figure 2. Typical Configuration (Connection)

Signal Descriptions

Table 3. PIN DESCRIPTIONS

MT9V124 Sensor Signal Name	Module Signal Name	Ball Number	Type	Description
EXTCLK	EXTCLK	E2	Input	Input clock signal
STANDBY	STBY	A2	Input	Controls sensor's standby mode, active HIGH
SCLK	SCLK	D4	Input	Two-wire serial interface clock
SDATA	SDATA	E4	I/O	Two-wire serial interface data
LVDS_P	LVDS_P	E1	Output	LVDS positive output
LVDS_N	LVDS_N	D2	Output	LVDS negative output
VDD	VDD	C2, D5	Supply	Digital power (TYP 1.8 V)
VAA, VDD_PLL	VAA	C1	Supply	Analog and PLL power (TYP 2.8 V)
VDD_IO	VDD_IO	C3	Supply	I/O power supply (TYP 1.8 V)
DGND, GND_IO, GND_PLL	DGND	B3, B5, D1	Supply	Digital, I/O, and PLL ground
AGND	AGND	B1	Supply	Analog ground
VPP	VPP	A1	Supply	OTPM power
DNU	DNU	A3,A4,A5,B2,B4, C4,C5,D3,E3,E5		

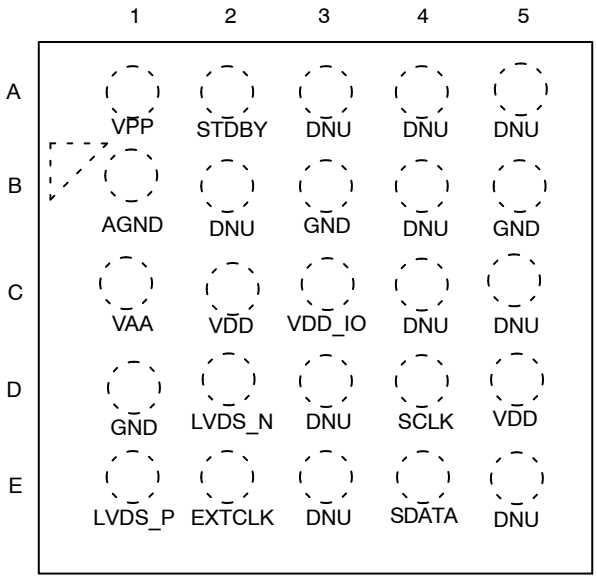


Figure 3. 25-ball Assignments (Top View)

Power-On Reset

The MT9V124 includes a power-on reset feature that initiates a reset upon power-up. A soft reset is issued by writing commands through the two-wire serial interface.

Standby

The MT9V124 supports two different standby modes:

- Hard standby mode
- Soft standby mode

The hard standby mode is invoked by asserting STANDBY pin. It then disables all the digital logic within the image sensor, and only supports being awoken by de-asserting the STANDBY pin. The soft standby mode is enabled by a single register access, which then disables the sensor core and most of the digital logic. However, the two-wire serial interface is kept alive, which allows the image sensor to be awoken via a serial register access.

All output signal status during standby are shown in Table 4.

Table 4. Status of Output Signals During Reset and Standby

Signal	Reset	Post-Reset	Standby
LVDS_P	High−Z	High−Z	High−Z
LVDS_N	High−Z	High−Z	High−Z

Module ID

The MT9V124 provides 4 bits of module ID that can be read by the host processor from register 0x001A[15:12]. The module ID is programmed through the OTPM.

Image Data Output Interface

The High Speed LVDS output port on MT9V124 can transmit the sensor image data to the host system over a lengthy differential twisted pair cable.

The MT9V124 provides a serial high-speed output port, which is able for driving standard IEEE 1596.3−1996 LVDS receiver/deserializers such as the DS92LV1212A LVDS Deserializer by National Semiconductor.

Image data is provided to the host system by the serial LVDS interface. The Start bit, 8-bit image data, LV, FV, and Stop bit are packetized in a 12-bit packet. The output interface block can select either raw data or processed data. Processed data format includes YCbCr, RGB-565, and BT656 with odd SAV/EAV code. It also supports the SOC Bypass 8 + 2 data format over the 12-bit packet.

The LVDS port is disabled when Hard Standby or Soft Standby is asserted.

Sensor Control

The sensor core of the MT9V124 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. Figure 4 shows a block diagram of the sensor core. It includes the VGA active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been selected, the data from each column is sequenced through an analog signal chain, including offset correction, gain adjustment, and ADC. The final stage of sensor core converts the output of the ADC into 10-bit data for each pixel in the array.

The pixel array contains optically active and light-shielded (dark) pixels. The dark pixels are used to provide data for the offset-correction algorithms (black level control).

The sensor core contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers are controlled by the MCU firmware and are also accessible by the host processor through the two-wire serial interface.

The output from the sensor core is a Bayer pattern; alternate rows are a sequence of either green and red pixels or blue and green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

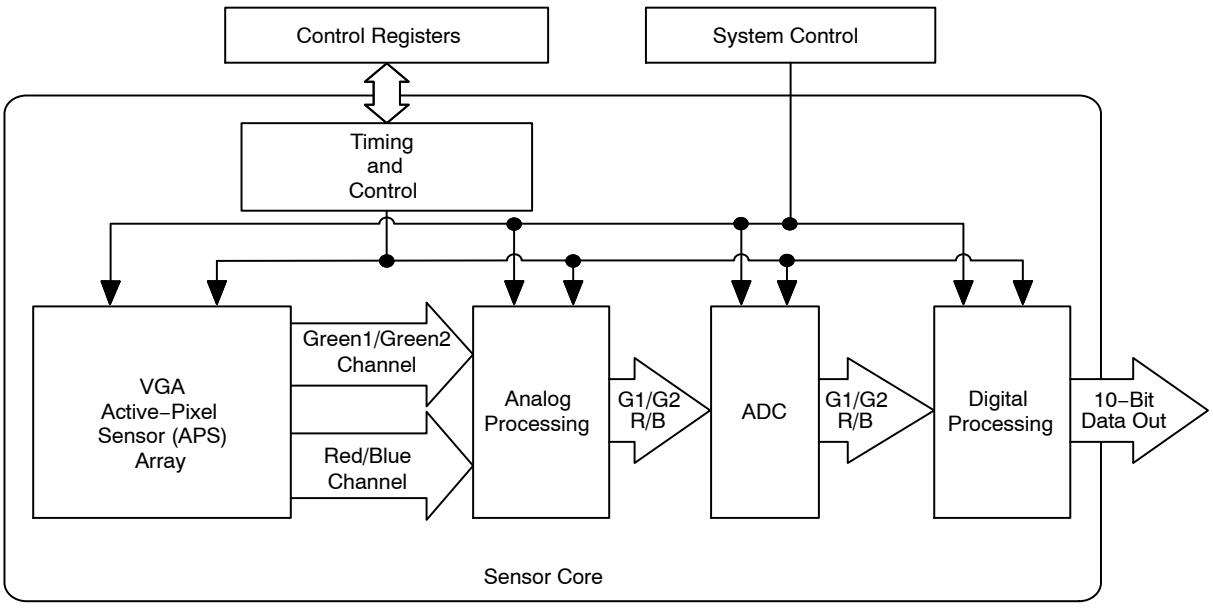


Figure 4. Sensor Core Block Diagram

The sensor core uses a Bayer color pattern, as shown in Figure 5. The even-numbered rows contain green and red pixels; odd-numbered rows contain blue and green pixels. Even-numbered columns contain green and blue pixels; odd-numbered columns contain red and green pixels.

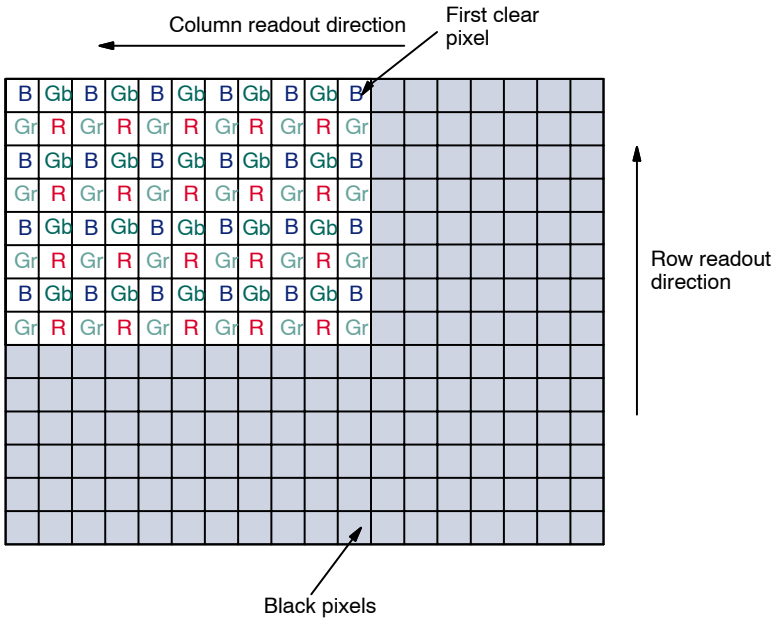


Figure 5. Pixel Color Pattern Detail

The MT9V124 sensor core pixel array is shown with pixel (0,0) in the bottom right corner, which reflects the actual layout of the array on the die. Figure 6 shows the image shown in the sensor during normal operation.

When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced.

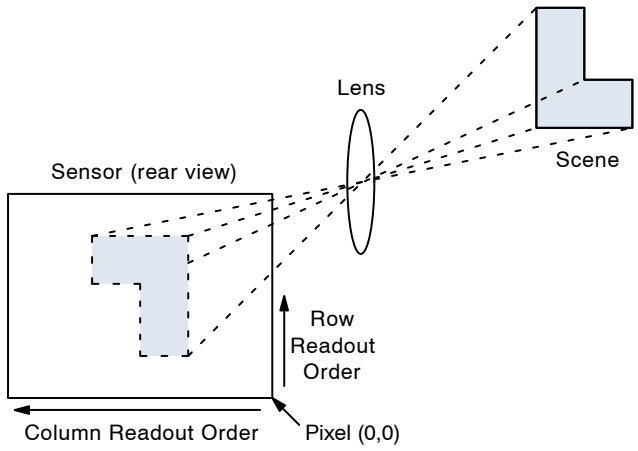


Figure 6. Imaging a Scene

The sensor core supports different readout options to modify the image before it is sent to the IFP. The readout can be limited to a specific window size of the original pixel array.

By changing the readout order, the image can be mirrored in the horizontal direction.

The image output size is set by programming row and column start and end address registers. The edge pixels in the 648 × 488 array are present to avoid edge effects and should not be included in the visible window.

When the sensor is configured to mirror the image horizontally, the order of pixel readout within a row is reversed, so that readout starts from the last column address and ends at the first column address. Figure 7 shows a sequence of 6 pixels being read out with normal readout and reverse readout. This change in sensor core output is corrected by the IFP.

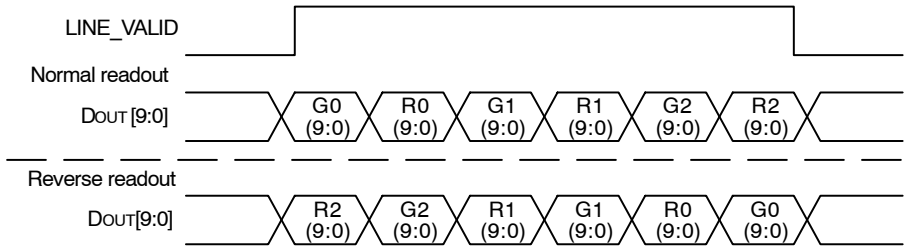


Figure 7. Six Pixels in Normal and Column Mirror Readout Mode (Internal Data Format before Serializer)

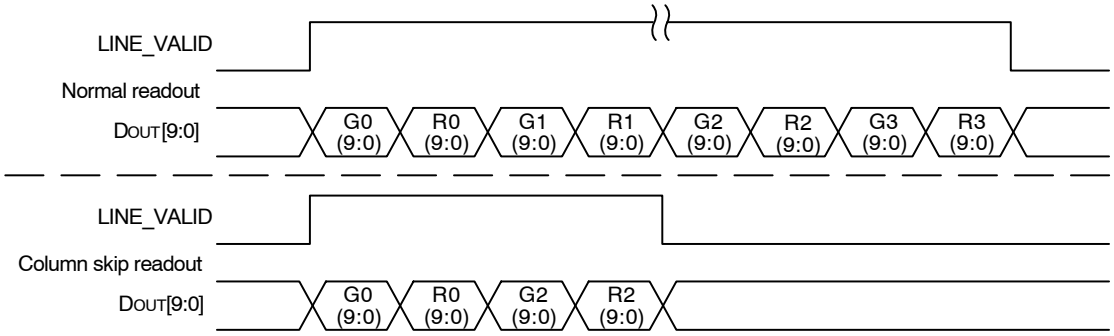


Figure 8. Eight Pixels in Normal and Column Skip 2X Readout Mode (Internal Data Format before Serializer)

Figure 9 through Figure 11 show the different skipping modes supported in MT9V124.

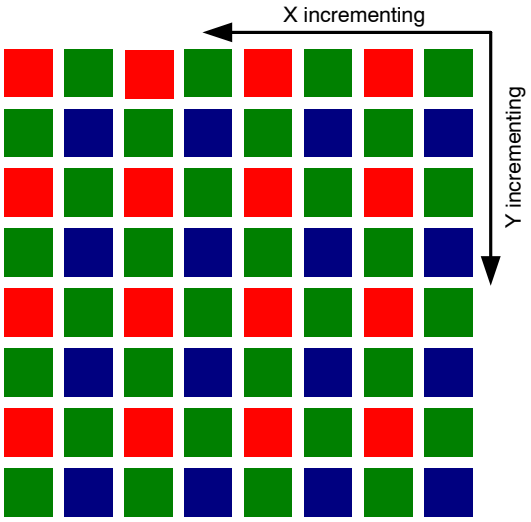


Figure 9. Pixel Readout (no skipping)

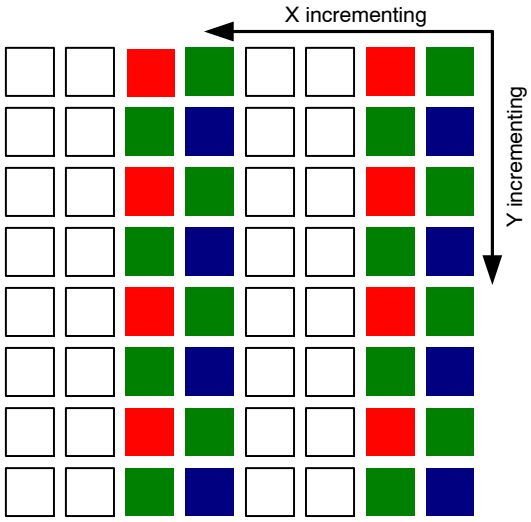


Figure 10. Pixel Readout (x_odd_inc = 3, y_odd_inc = 1)

Image Flow Processor

Image control processing in the MT9V124 is implemented in the IFP hardware logic. The IFP registers can be programmed by the host processor. For normal operation, the microcontroller automatically adjusts the operational parameters of the IFP. Figure 11 shows the image data processing flow within the IFP.

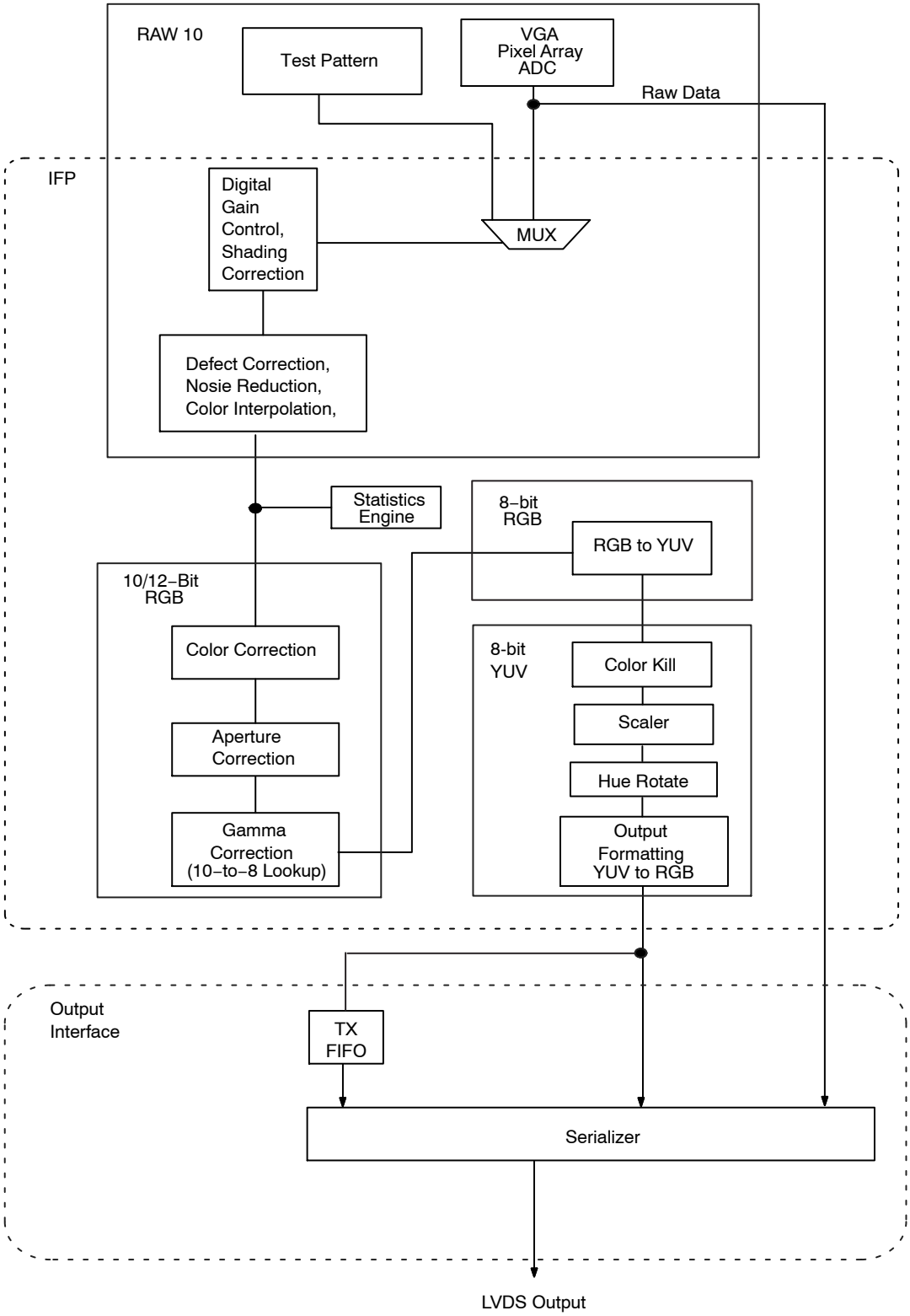


Figure 11. Image Flow Processor

For normal operation of the MT9V124, streams of raw image data from the sensor core are continuously fed into the color pipeline. The MT9V124 features an automatic color bar test pattern generation function to emulate sensor images as shown in Figure 12.

Color bar test pattern generation can be selected by programming a register.

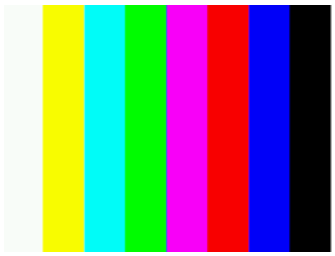
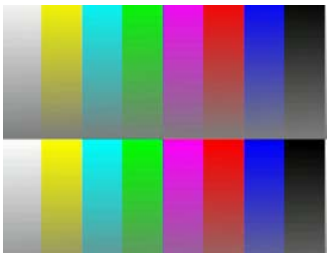
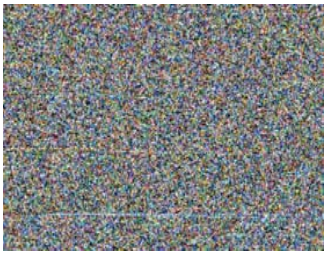
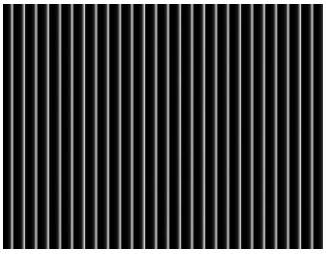
Test Pattern	Example
REG= 0x8400, 0x15 // SEQ_CMD	
REG= 0x8400, 0x16 // SEQ_CMD	
REG= 0x8400, 0x17 // SEQ_CMD	
REG= 0x8400, 0x18 // SEQ_CMD	
REG= 0x8400, 0x19 // SEQ_CMD	

Figure 12. Color Bar Test Pattern

Image Corrections

Image stream processing starts with multiplication of all pixel values by a programmable digital gain. This can be independently set to separate values for each color channel (R, Gr, Gb, B). Independent color channel digital gain can be adjusted with variables.

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The MT9V124 has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

The IFP performs continuous defect correction that can mask pixel array defects such as high dark-current (hot) pixels and pixels that are darker or brighter than their neighbors due to photoresponse nonuniformity. The module is edge-aware with exposure that is based on configurable thresholds. The thresholds are changed continuously based on the brightness of the current scene. Enabling and disabling noise reduction, and setting thresholds can be defined through variable settings.

Color Interpolation and Edge Detection

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10-bit integer, which can be considered proportional to the pixel's response to a one-color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one-color-per-pixel nature of the data stream, but after the defect correction it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module adds the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high-frequency noise in flat field areas. The edge threshold can be set through variable settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3×3 color correction matrix. The color correction matrix can either be programmed by the user or automatically selected by the AWB algorithm implemented in the IFP. Color correction should ideally produce output colors that are independent of the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics. The color correction variables can be adjusted through variable settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color-corrected image data. The gain and threshold for 2D correction can be defined through variable settings.

Gamma Correction

The gamma correction curve (as shown in Figure 13) is implemented as a piecewise linear function with 19 knee points, taking 12-bit arguments and mapping them to 8-bit output. The abscissas of the knee points are fixed at 0, 64, 128, 256, 512, 768, 1024, 1280, 1536, 1792, 2048, 2304, 2560, 2816, 3072, 3328, 3584, 3840, and 4096.

The MT9V124 IFP includes a block for gamma correction that has the capability to adjust its shape, based on brightness, to enhance the performance under certain lighting conditions. Two custom gamma correction tables may be uploaded, one corresponding to a brighter lighting condition, the other one corresponding to a darker lighting condition. The final gamma correction table used depends on the brightness of the scene and can take the form of either uploaded tables or an interpolated version of the two tables. A single (non-adjusting) table for all conditions can also be used.

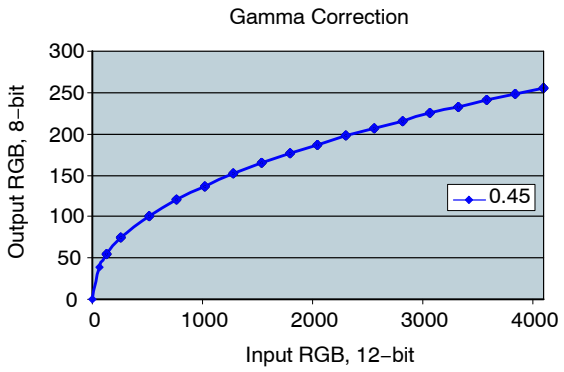


Figure 13. Gamma Correction Curve

Special effects like negative image, sepia, or B/W can be applied to the data stream at this point. These effects can be enabled and selected by registers.

To remove high- or low-light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

Image Scaling and Cropping

To ensure that the size of images output by the MT9V124 can be tailored to the needs of all users, the IFP includes a scaler module. When enabled, this module performs rescaling of incoming images-shrinks them to selected width and height without reducing the field of view and without discarding any pixel values. The scaler ratios are computed from image output size and the FOV. The scaled

output must not be greater than 352. Output widths greater than this must not use the scaler.

By configuring the cropped and output windows to various sizes, different zooming levels for 4X, 2X, and 1X can be achieved. The height and width definitions for the output window must be equal to or smaller than the cropped image. The image cropping and scaler module can be used together to implement a digital zoom.

Hue Rotate

The MT9V124 has integrated hue rotate. This feature will help for improving the color image quality and give customers the flexibility for fine color adjustment and special color effects.

REG= 0xA00F, 0x00 // CAM_HUE_ANGLE

Figure 14. 0° Hue

REG= 0xA00F, 0xEA // CAM_HUE_ANGLE

Figure 15. –22° Hue

REG= 0xA00F, 0x16 // CAM_HUE_ANGLE

Figure 16. +22° Hue

Auto Exposure

The AE algorithm performs automatic adjustments of the image brightness by controlling exposure time, and analog gains of the sensor core as well as digital gains applied to the image.

The AE algorithm analyzes image statistics collected by the exposure measurement engine, and then programs the sensor core and color pipeline to achieve the desired exposure. AE uses 4×4 exposure statistics windows, which can be scaled in size to cover any portion of the image.

The MT9V124 uses Average Brightness Tracking (Average Y), which uses a constant average tracking algorithm where a target brightness value is compared to a current brightness value, and the gain and integration time are adjusted accordingly to meet the target requirement. The MT9V124 also has a weighted AE algorithm that allows the sensor to be configured to respond to scene illuminance based on each of the weights in the windows.

The auto exposure can be configured to respond to scene illuminance based on certain criteria by adjusting gains and integration time based on scene brightness.

Auto White Balance

The MT9V124 has a built-in AWB algorithm designed to compensate for the effects of changing spectra of the scene illumination on the quality of the color rendition. The algorithm consists of two major parts: a measurement engine performing statistical analysis of the image and a module performing the selection of the optimal color correction matrix, digital, and sensor core analog gains. While default settings of these algorithms are adequate in most situations, the user can reprogram base color correction matrices and place limits on color channel gains.

The AWB algorithm estimates the dominant color temperature of a light source in a scene and adjusts the B/G, R/G gain ratios accordingly to produce an image for sRGB display in which grey and white surfaces are reproduced faithfully. This usually means that R,G,B are roughly equal for these surfaces hence the word “balance”.

The AWB algorithm uses statistics collected from the last frame to calculate the required B/G and R/G ratios and set the blue and red analog sensor gains and digital SOC gains to reproduce the most accurate grey and white surfaces

Flicker Detection and Avoidance

Flicker occurs when the integration time is not an integer multiple of the period of the light intensity. The automatic flicker detection module does not compensate for the flicker, but rather avoids it by detecting the flicker frequency and adjusting the integration time. For integration times below the light intensity period (10 ms for 50 Hz environment, 8.33 ms for 60 Hz environment), flicker cannot be avoided.

While this fast flickering is marginally detectable by the human eye, it is very noticeable in digital images because the flicker period of the light source is very close to the range of digital images’ exposure times.

Many CMOS sensors use a “rolling shutter” readout mechanism that greatly improves sensor data readout times. This allows pixel data to be read out much sooner than other methods that wait until the entire exposure is complete before reading out the first pixel data. The rolling shutter mechanism exposes a range of pixel rows at a time. This range of exposed pixels starts at the top of the image and then “rolls” down to the bottom during the exposure period of the frame. As each pixel row completes its exposure, it is ready to be read out. If the light source oscillates (flickers) during this rolling shutter exposure period, the image appears to have alternating light and dark horizontal bands.

If the sensor uses the traditional snapshot readout mechanism, in which all pixels are exposed at the same time and then the pixel data is read out, then the image may appear overexposed or underexposed due to light fluctuations from

the flickering light source. Lights operating on AC electric systems produce light flickering at a frequency of 100 Hz or 120 Hz, twice the frequency of the power line.

To avoid this flicker effect, the exposure times must be multiples of the light source flicker periods. For example, in a scene lit by 120 Hz lighting, the available exposure times are 8.33 ms, 16.67 ms, 25 ms, 33.33 ms, and so on. (The need for an exposure time less than 8.33 ms under artificial light is extremely rare.)

In this case, the AE algorithm must limit the integration time to an integer multiple of the light's flicker period.

By default, the MT9V124 does all of this automatically, ensuring that all exposure times avoid any noticeable light flicker in the scene. The MT9V124 AE algorithm is always setting exposure times to be integer multipliers of either 100 Hz or 120 Hz. The flicker detection module keeps monitoring the incoming frames to detect whether the scene's lighting has changed to the other of the two light source frequencies. A 50 Hz/60 Hz Tungsten lamp can be used to calibrate the flicker detect settings.

Output Conversion and Formatting

The YUV data stream can either exit the color pipeline as is or be converted before exit to an alternative YUV or RGB data format.

Color Conversion Formulas

Y'U'V':

This conversion is BT 601 scaled to make YUV range from 0 through 255. This setting is recommended for JPEG encoding and is the most popular, although it is not well defined and often misused in various operating systems.

$$Y' = 0.299 \times R' + 0.587 \times G' + 0.114 \times B' \quad \text{(eq. 1)}$$

$$U' = 0.564 \times (B' - Y') + 128 \quad \text{(eq. 2)}$$

$$V' = 0.713 \times (R' - Y') + 128 \quad \text{(eq. 3)}$$

There is an option where 128 is not added to U'V'.

Y'Cb'Cr' Using sRGB Formulas:

The MT9V124 implements the sRGB standard. This option provides YCbCr coefficients for a correct 4:2:2 transmission.

NOTE: 16 < Y601< 235; 16 < Cb < 240; 16 < Cr < 240; and 0 < = RGB < = 255

$$Y' = (0.2126 \times R' + 0.7152 \times G' + 0.0722 \times B') \times \times (219/256) + 16 \quad \text{(eq. 4)}$$

$$Cb' = 0.5389 \times (B' - Y') \times (224/256) + 128 \quad \text{(eq. 5)}$$

$$Cr' = 0.635 \times (R' - Y') \times (224/256) + 128 \quad \text{(eq. 6)}$$

Y'U'V' Using sRGB Formulas:

These are similar to the previous set of formulas, but have YUV spanning a range of 0 through 255.

$$Y' = 0.2126 \times R' + 0.7152 \times G' + 0.0722 \times B' + + 128 \quad \text{(eq. 7)}$$

$$U' = 0.5389 \times (B' - Y') + 128 = = - 0.1146 \times R' - 0.3854 \times G' + 0.5 \times B' + 128 \quad \text{(eq. 8)}$$

$$V' = 0.635 \times (R' - Y') + 128 = = 0.5 \times R' - 0.4542 \times G' - 0.0458 \times B' + 128 \quad \text{(eq. 9)}$$

There is an option to disable adding 128 to U'V'. The reverse transform is as follows:

$$R' = Y + 1.5748 \times (V - 128) \quad \text{(eq. 10)}$$

$$G' = Y - 0.1873 \times (U - 128) - 0.4681 \times (V - 128) \quad \text{(eq. 11)}$$

$$B' = Y + 1.8556 \times (U - 128) \quad \text{(eq. 12)}$$

Uncompressed YUV/RGB Data Ordering

The MT9V124 supports swapping YCbCr mode, as illustrated in Table 5.

Table 5. YCbCr OUTPUT DATA ORDERING

Mode	Data Sequence			
Default (no Swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CrCb	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CrCb, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

The RGB output data ordering in default mode is shown in Table 6. The odd and even bytes are swapped when luma/chroma swap is enabled. R and B channels are bitwise swapped when chroma swap is enabled.

Table 6. RGB ORDERING IN DEFAULT MODE

Mode (Swap Disabled)	Byte	$D_7D_6D_5D_4D_3D_2D_1D_0$
565RGB	Odd	$R_7R_6R_5R_4R_3G_7G_6G_5$
	Even	$G_4G_3G_2B_7B_6B_5B_4B_3$

Uncompressed 10-Bit Bypass Output

Raw 10-bit Bayer data from the sensor core can be output in bypass mode by using DOUT[7:0] with a special 8 + 2 data format, shown in Table 7.

Table 7. 2-BYTE BAYER FORMAT

Byte	Bits Used	Bit Sequence
Odd Bytes	8 Data Bits	$D_9D_8D_7D_6D_5D_4D_3D_2$
Even Bytes	2 Data Bits + 6 Unused Bits	0 0 0 0 0 0 D_1D_0

BT656

YUV data can also be output in BT656 format with only Odd field SAV/EAV codes. The BT656 data output will be progressive data and not interlaced (R0x3C00[5] = 1). Figure 17 depicts the data format before the serializer internal to the device, or after the external deserializer.

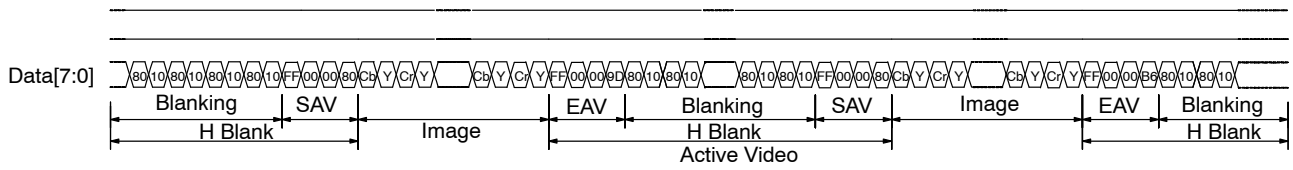


Figure 17. BT656 Image Data with Odd SAV/EAV Codes

REGISTER AND VARIABLE DESCRIPTION

To change internal registers and RAM variables of MT9V124, use the two-wire serial interface through the external host device.

The sequencer is responsible for coordinating all events triggered by the user.

The sequencer provides the high-level control of the MT9V124. Commands are written to the command variable to start streaming, stop streaming, and to select test pattern modes. Command execution is confirmed by reading back the command variable with a value of zero. The sequencer state variable can also be checked for transition to the desired state. All configuration of the sensor (start/stop row/column, mirror, skipping) and the SOC (image size, format) and automatic algorithms for AE, AWB, low light, are performed when the sequencer is in the stopped state.

When the sequencer is in the idle or test pattern state the algorithms and register updates are not performed, allowing the host complete manual control

Table 8. SUMMARY OF MT9V124 VARIABLES

Name	Variable Description
Monitor Variables	General Information
Sequencer Variables	Programming Control Interface
FD Variables	Flicker Detect
AE_Track Variables	Auto Exposure
AWB Variables	Auto White Balance
Stat Variables	Statistics
Low Light Variables	Low Light
Cam Variables	Sensor Specific Settings

SERIAL LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) OUTPUT

The MT9V124 provides a serial high-speed output port which supports all the data formats. MT9V124 is intended to drive standard IEEE 1596.3−1996 LVDS receiver/deserializers. The internal serializer transforms the parallel data into serial in a 12-bit packet, allowing the data be transported via a lengthy (several meters) twisted pair cable.

The LVDS output requires a differential termination resistor (Rtx_term = 140 Ω ±1%) that must be provided off-chip and close to the LVDS pins.

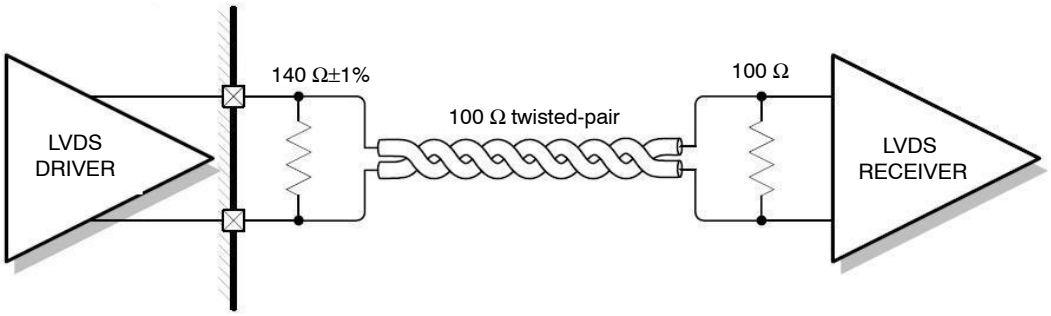


Figure 18. LVDS Typical Serial Interface

LVDS Data Packet Format

The LVDS output is the standard 12-bit package with start bit, 10-bit payload and stop bit supported by many off the shelf deserializers.

Table 9 describes the LVDS packet format; Figure 19 shows the LVDS data timing.

Table 9. LVDS PACKET FORMAT

12-Bit Packet	Data Format
Bit[0]	START BIT “1”
Bit[1]	PixelData[0]
Bit[2]	PixelData[1]
Bit[3]	PixelData[2]
Bit[4]	PixelData[3]
Bit[5]	PixelData[4]
Bit[6]	PixelData[5]
Bit[7]	PixelData[6]
Bit[8]	PixelData[7]
Bit[9]	LINEVALID (LV)
Bit[10]	FRAMEVALID (FV)
Bit[11]	STOP BIT “0”

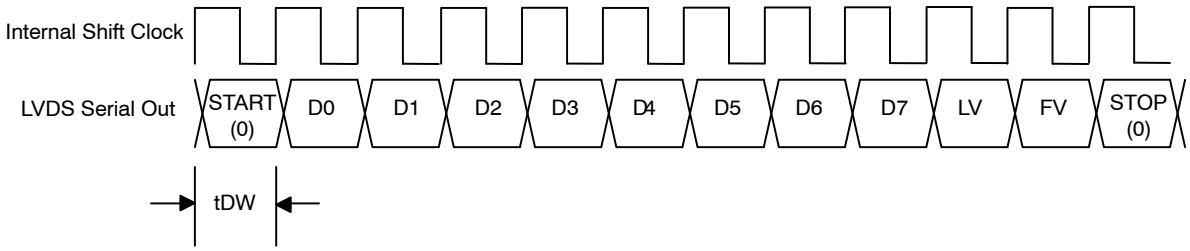


Figure 19. LVDS Serial Output Timing

Table 10. LVDS SERIAL OUTPUT DATA TIMING (FOR EXTCLK = 22 MHz)

Name	Min	Typical	Max	Unit
tDW	3.78	3.78	4.629	nS
1/tDW	216	264	264	Mbps

Table 11. EXTCLK INPUT RANGE

Name	Min	Typical	Max	Unit
EXTCLK	18	22	44	MHz

If EXTCLK is greater than 22 MHz, the PLL must be set to obtain an equivalent internal pixel clock to 22 MHz. The internal pixel clock is multiplied by 12 to achieve the serializer output frequency of maximum 264 MHz.

TWO-WIRE SERIAL INTERFACE

The two-wire serial interface bus enables read and write access to control and status registers within the MT9V124.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The MT9V124 always operates in slave mode. The host (master) generates a clock (SCLK) that is an input to the MT9V124 and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA).

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements, as follows:

1. a (repeated) start condition
2. a slave address/data direction byte
3. a 16-bit register address
   (8-bit addresses are not supported)
4. an (a no) acknowledge bit
5. a 16-bit data transfer
   (8-bit data transfers are supported using XDMA byte access)
6. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH.

At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a repeated start or restart condition.

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data is transferred serially, 8 bits at a time, with the most significant bit (MSB) transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes. One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

MT9V124 Slave Address

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The slave address default is 0x7A.

Messages

Message bytes are used for sending MT9V124 internal register addresses and data. The host should always use 16-bit address (two bytes) and 16-bit data to access internal registers. Refer to READ and WRITE cycles in Figure 20 through Figure 24.

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. For data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

The no-acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Operation

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which a WRITE will take place. This transfer takes place as two 8-bit sequences and the slave

sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16-bit data, as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, just as in the WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

Figure 20 shows the typical READ cycle of the host to MT9V124. The first 2 bytes sent by the host are an internal 16-bit register address. The following 2-byte READ cycle sends the contents of the registers to host.

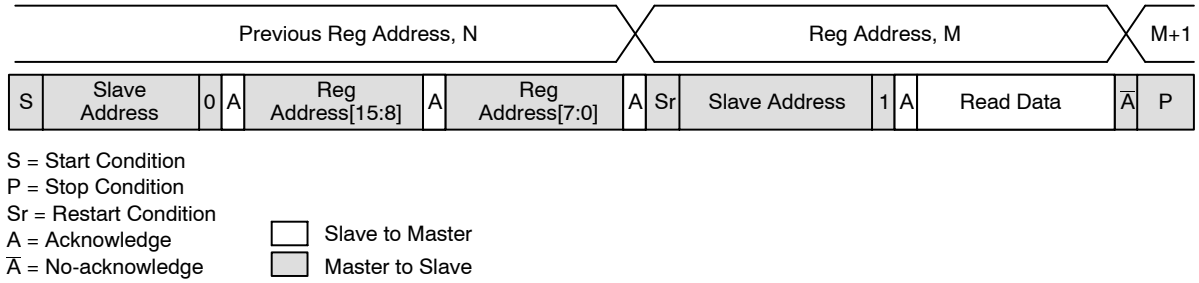


Figure 20. Single READ from Random Location

Single READ from Current Location

Figure 21 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

Figure 21. Single Read from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 22) starts in the same way as the single READ from random location (Figure 20). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

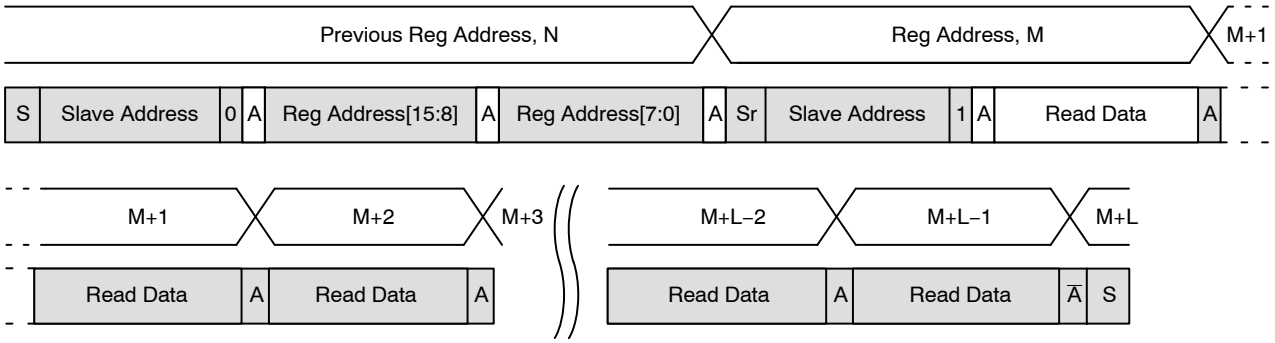


Figure 22. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 23) starts in the same way as the single READ from current location (Figure 21). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until "L" bytes have been read.

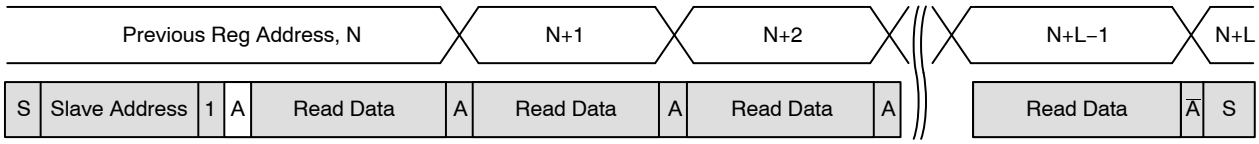


Figure 23. Sequential READ, Start from Current Location

Single Write to Random Location

Figure 24 shows the typical WRITE cycle from the host to the MT9V124. The first 2 bytes indicate a 16-bit address of the internal registers with most-significant byte first. The following 2 bytes indicate the 16-bit data.

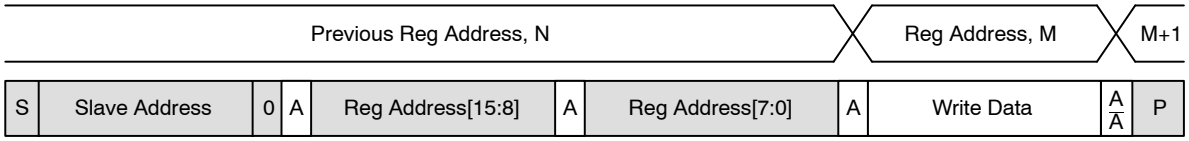


Figure 24. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 25) starts in the same way as the single WRITE to random location (Figure 24). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

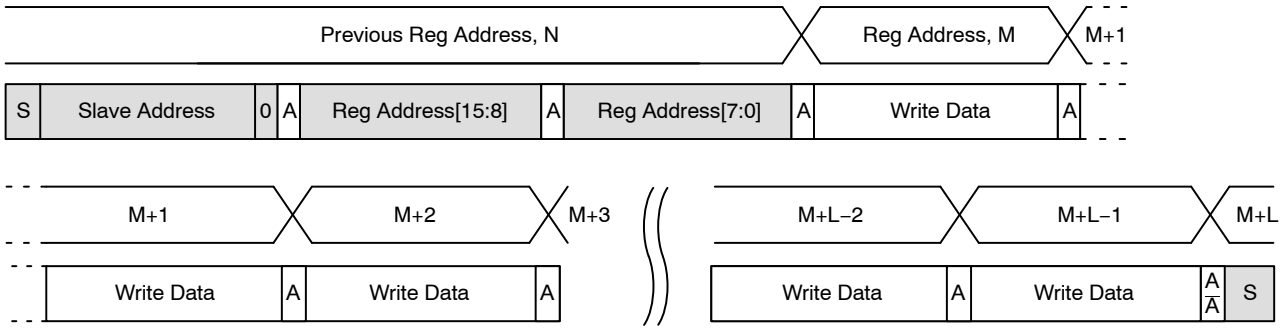


Figure 25. Sequential WRITE, Start at Random Location

One-Time Programming Memory (OTPM)

The MT9V124 has one-time programmable memory (OTPM) for supporting defect correction, module ID, and other customer-related information. There are 2784 bits of OTPM available for features such as Lens Shading Correction, Color Correction Matrix, White Balance Weight, and user-defined information. The OTPM programming requires the data to be first placed in OTPM buffer and the presence of VPP. The proper procedure and timing must be followed.

SPECTRAL CHARACTERISTICS

CRA vs. Image Height Plot

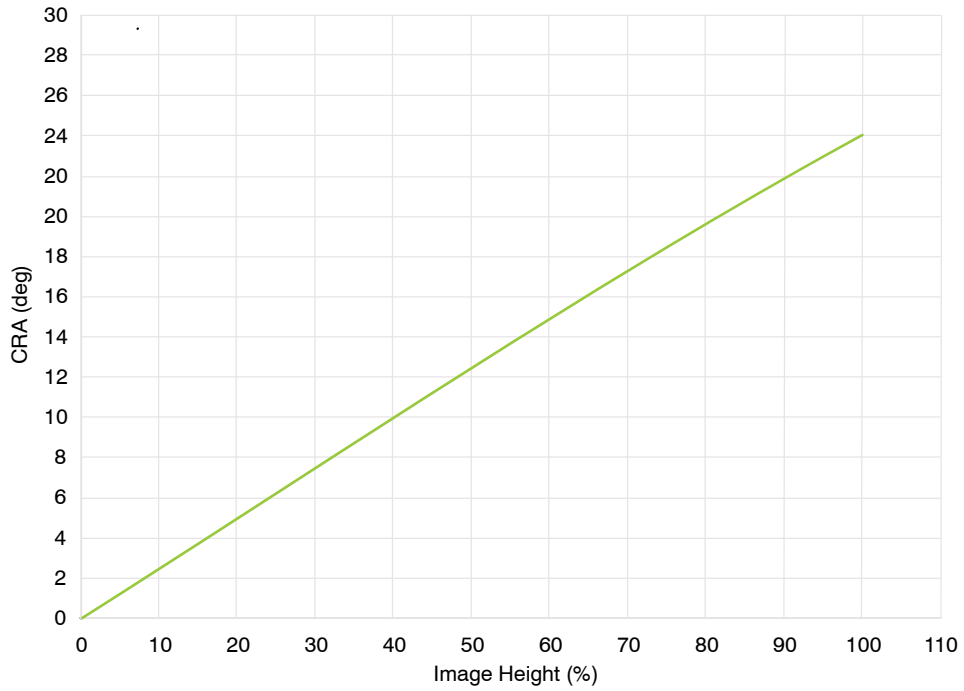


Figure 26. Chief Ray Angle (CRA) vs. Image Height

Image Height (%)	Image Height (mm)	CRA (deg)
0	0	0
5	0.035	1.23
10	0.070	2.46
15	0.105	3.70
20	0.140	4.94
25	0.175	6.18
30	0.210	7.43
35	0.245	8.67
40	0.280	9.90
45	0.315	11.13
50	0.350	12.36
55	0.385	13.57
60	0.420	14.77
65	0.455	15.97
70	0.490	17.14
75	0.525	18.31
80	0.560	19.45
85	0.595	20.58
90	0.630	21.69
95	0.665	22.77
100	0.700	23.83

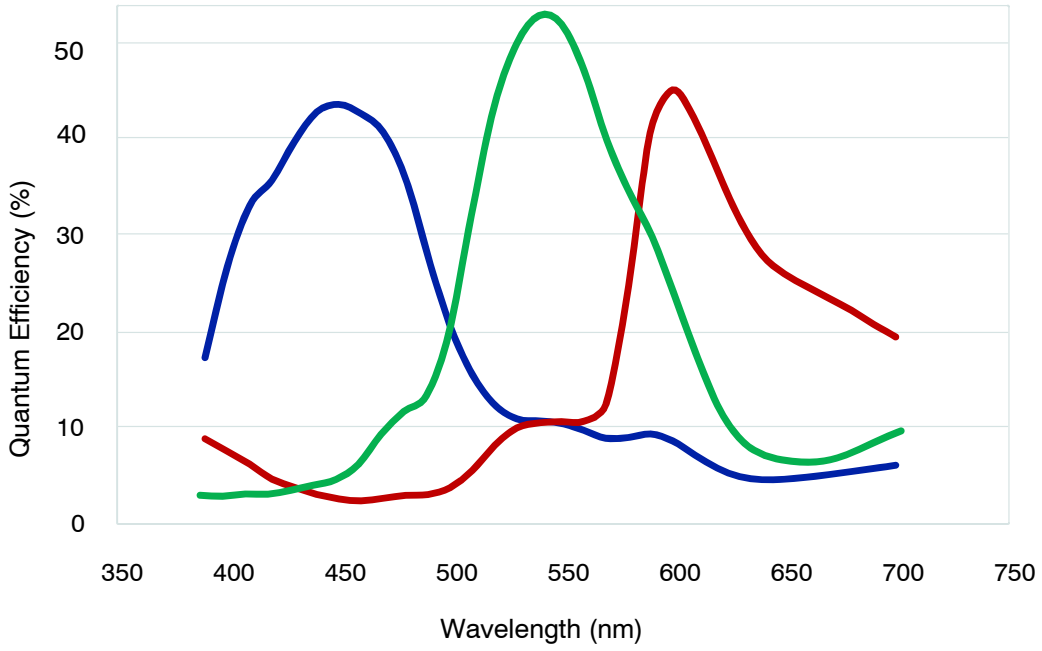


Figure 27. Quantum Efficiency

ELECTRICAL SPECIFICATIONS

Table 12. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Unit
		Min	Max	
V_{DD}	Core Digital Voltage	–0.3	2.4	V
V_{DD}_IO	I/O Digital Voltage	–0.3	4.0	V
V_{AA}	Analog Voltage	–0.3	4.0	V
V_{AA}_PIX	Pixel Supply Voltage	–0.3	4.0	V
V_{PP}	OTPM Power Supply	7.5	9.5	V
V_{IN}	Input Voltage	–0.3	V_{DD}_IO + 0.3	V
T_{OP}	Operating Temperature (Measure at Junction)	–30	70	°C
T_{STG} (Note 1)	Storage Temperature	–40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 13. OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Core Digital Voltage	1.7	1.8	1.95	V
V_{DD}_IO	I/O Digital Voltage	2.5	2.8	3.1	V
		1.7	1.8	1.95	V
V_{AA}	Analog Voltage	2.5	2.8	3.1	V
V_{AA}_PIX	Pixel Supply Voltage	2.5	2.8	3.1	V
V_{DD}_PLL	PLL Supply Voltage	2.5	2.8	3.1	V
V_{PP}	OTPM Power Supply	8.5	8.5	9	V
T_J	Operating Temperature (at Junction)	–30	55	70	°C

Table 14. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input HIGH Voltage		0.7 * V_{DD}_IO	V_{DD}_IO + 0.5	V
V_{IL}	Input LOW Voltage		–0.3	0.3 * V_{DD}_IO	V
I_{IN}	Input Leakage Current	V_{IN} = 0V or V_{IN} = V_{DD}_IO		10	μA
V_{OH}	Output HIGH Voltage	V_{DD}_IO = 1.8 V, I_{OH} = 2 mA	1.7	–	V
		V_{DD}_IO = 1.8 V, I_{OH} = 4 mA	1.6	–	V
		V_{DD}_IO = 1.8 V, I_{OH} = 8 mA	1.4	–	V
		V_{DD}_IO = 2.8 V, I_{OH} = 2 mA	2.7	–	V
		V_{DD}_IO = 2.8 V, I_{OH} = 4 mA	2.6	–	V
		V_{DD}_IO = 2.8 V, I_{OH} = 8 mA	2.5	–	V

Table 14. DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Output LOW Voltage	V_{DD}_IO = 1.8 V, I_{OH} = 2 mA	–	0.1	V
		V_{DD}_IO = 1.8 V, I_{OH} = 4 mA	–	0.2	V
		V_{DD}_IO = 1.8 V, I_{OH} = 8 mA	–	0.4	V
		V_{DD}_IO = 2.8 V, I_{OH} = 2 mA	–	0.1	V
		V_{DD}_IO = 2.8 V, I_{OH} = 4 mA	–	0.2	V
		V_{DD}_IO = 2.8 V, I_{OH} = 8 mA	–	0.4	V

Table 15. OPERATING/STANDBY CURRENT CONSUMPTION
(^{f}EXTCLK = 44 MHz; voltages = Typ or Max; TJ = Typ or Max; excludes V_{DD}_IO current)

Symbol	Parameter	Condition	Typ	Unit
I_{DD}	Digital Operating Current		9.5	mA
I_{DD}	Digital Operating Current		9.5	mA
I_{AA}	Analog Operating Current		7	mA
I_{DD}_PLL	PLL Supply Current		5	mA
	Total Supply Current		21.5	mA
	Total Power Consumption		55	mW
Hard Standby	Total Standby Current when Asserting the STANDBY Signal		19	µA
	Standby Power		44	µW
Soft Standby (Clock On)	Total Standby Current	^{f}EXTCLK = 44 MHz, Soft standby mode	1.67	mA
	Standby Power		3.016	mW
Soft Standby (Clock Off)	Total Standby Current	Soft Standby Mode	19	µA
	Standby Power		44.2	µW

Table 16. LVDS OUTPUT PORT DC SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage High	V_{oh}				1650	mV
Output Voltage Low	V_{ol}		850			mV
Differential Output Voltage	V_{od}		280	360	460	mV
Output Offset Voltage	V_{os}	See text	1000	1192	1400	mV
Single-ended Output Resistance	Ro		150		250	Ω
Output Resistance Mismatch	ΔRo				12	%
Reflection Coefficient Mismatch	Δρ				8	%
Differential Output Mismatch	ΔV_{od}				6	mV
Offset Voltage Mismatch	ΔV_{os}	See text			30	mV
Output Short-circuit Current	I_{sa}, I_{sb}				17	mA
Output Short-circuit Current	I_{sab}				10	mA
Standing Power-supply Current	I_{vddio}				8	mA
Clock Signal Duty Cycle	clock	250 MHz; C_{load} = 6pF	48		53	5
Differential Signal Rise Time	t_r	C_{load} = 6pF			360	ps
Differential Signal Fall Time	t_f	C_{load} = 6pF			360	ps

Table 16. LVDS OUTPUT PORT DC SPECIFICATIONS (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Propagation Delay	t_p	C_{load} = 6pF			2.5	ns
Differential Skew	t_{skew}	C_{load} = 6pF				πΩ

Table 17. TWO-WIRE SERIAL INTERFACE TIMING DATA
(^{f}EXTCLK = 22 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V)

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	^{f}SCL	0	100	0	400	KHz
Hold Time (repeated) START Condition.						
After this Period, the First Clock Pulse is Generated	^{t}HD;STA	4.0	–	0.6	–	µS
LOW Period of the SCLK Clock	^{t}LOW	4.7	–	1.3	–	µS
HIGH Period of the SCLK Clock	^{t}HIGH	4.0	–	0.6	–	µS
Set-up Time for a Repeated START Condition	^{t}SU;STA	4.7	–	0.6	–	µS
Data Hold Time	^{t}HD;DAT	0 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	µS
Data Set-up Time	^{t}SU;DAT	250	–	100 (Note 6)	–	nS
Rise Time of Both SDATA and SCLK Signals	^{t}r	–	1000	20 + 0.1Cb (Note 7)	300	nS
Fall Time of Both SDATA and SCLK Signals	^{t}f	–	300	20 + 0.1Cb (Note 7)	300	nS
Set-up Time for STOP Condition	^{t}SU;STO	4.0	–	0.6	–	µS
Bus Free Time between a STOP and START Condition	^{t}BUF	4.7	–	1.3	–	µS
Capacitive Load for Each Bus Line	Cb	–	400	–	400	pF
Serial Interface Input Pin Capacitance	CIN_SI	–	3.3	–	3.3	pF
SDATA Max Load Capacitance	CLOAD_SD	–	30	–	30	pF
SDATA Pull-up Resistor	RSD	1.5	4.7	1.5	4.7	KΩ

1. This table is based on I^{2}C standard (v2.1 January 2000). On Semiconductor
2. Two-wire control is I^{2}C−compatible
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1V_{DD} levels. Sensor EXCLK = 22 MHz
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal
6. A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLK line is released
7. Cb = total capacitance of one bus line in pF

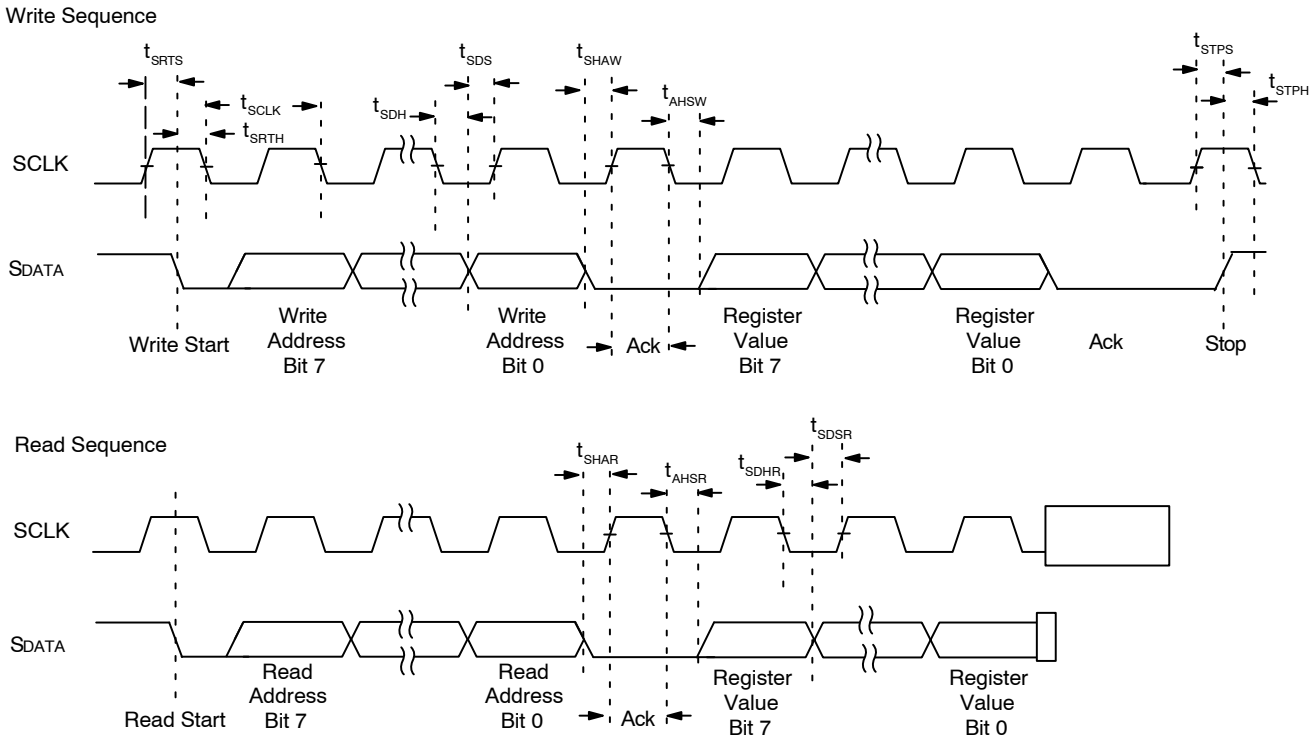


Figure 28. Two-Wire Serial Bus Timing Parameters

POWER SEQUENCE

Powering up the sensor requires the supply rails to be applied in a particular order to ensure sensor start up in a normal operation and prevent undesired condition such as latch up from happening. Refer to Figure 29 and Table 18 for detailed timing requirement.

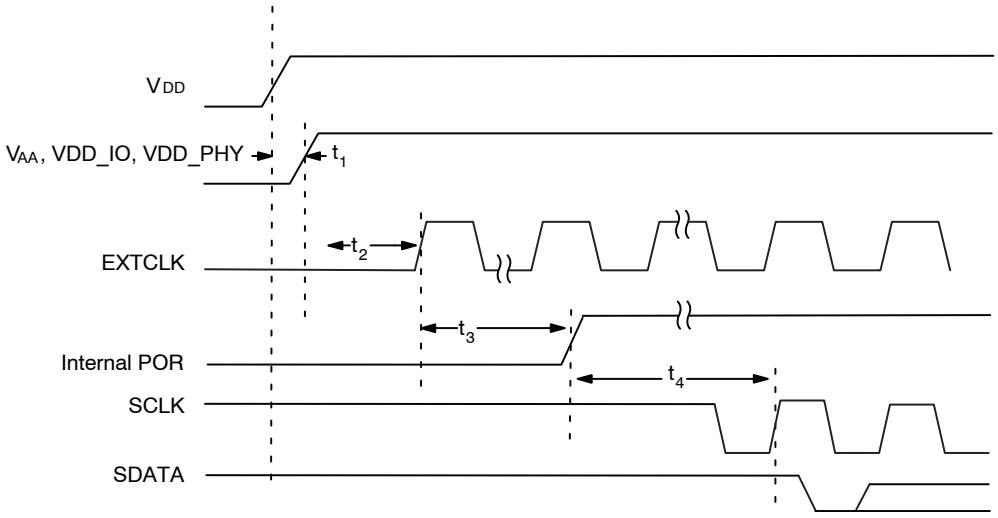


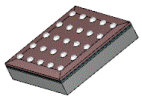
Figure 29. Power-Up Sequence

Table 18. POWER UP SIGNAL TIMING

Symbol	Parameter	Min	Typ	Max	Unit
t1	Delay from V_{DD} to V_{AA} and V_{DD}_IO	0	–	500	ms
t2	EXTCLK Activation	t1	100	–	ms
t3	Internal POR Duration	70	–	–	EXTCLKs
t4	First I^2C Write	50	–	–	EXTCLKs

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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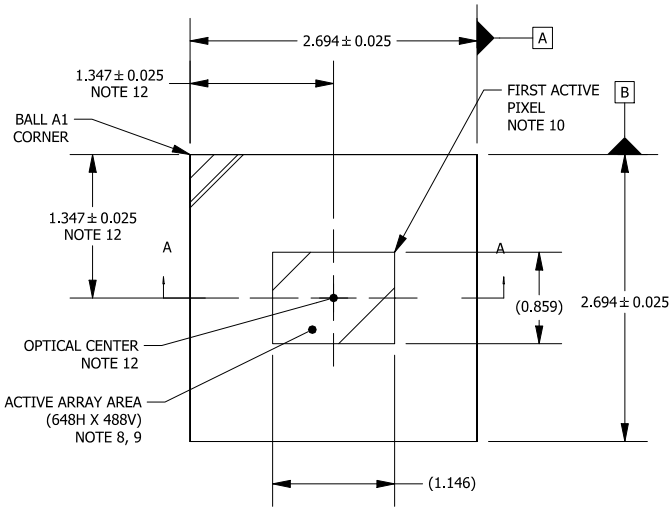
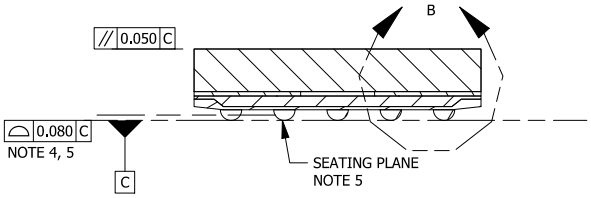


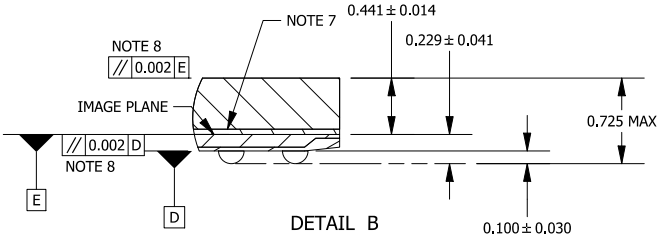
TOP VIEW

NOTES:

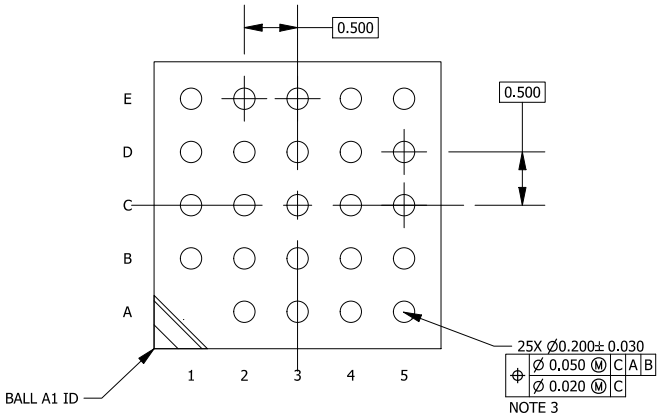
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.400 THICKNESS; REFRACTIVE INDEX = 1.52.
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.041 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 0.1°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. PACKAGE CENTER (X, Y) = (0.000, 0.000).
12. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (0.000, 0.000).



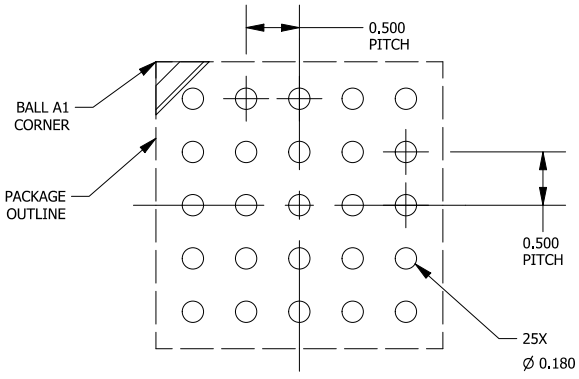
SECTION A-A



DETAIL B



BOTTOM VIEW



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