

NLU1G04

Single Inverter

The NLU1G04 MiniGate™ is an advanced high-speed CMOS inverter in ultra-small footprint.

The NLU1G04 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns (Typ) @ } V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A (Max) at } T_A = 25^\circ\text{C}$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

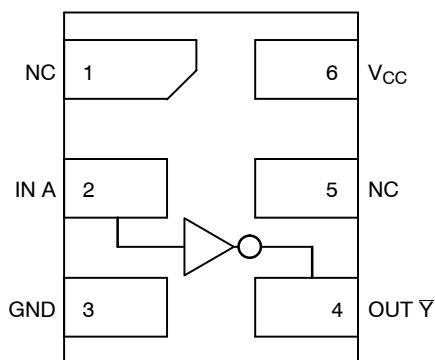


Figure 1. Pinout (Top View)

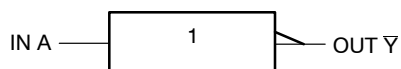


Figure 2. Logic Symbol

PIN ASSIGNMENT

1	NC
2	IN A
3	GND
4	OUT \bar{Y}
5	NC
6	V_{CC}

FUNCTION TABLE

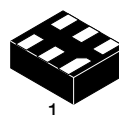
A	\bar{Y}
L	H
H	L



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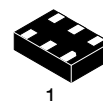
MARKING DIAGRAMS



UDFN6
MU SUFFIX
CASE 517AA



UDFN6
1.0 x 1.0
CASE 517BX



UDFN6
1.45 x 1.0
CASE 517AQ



R = Device Marking
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

NLU1G04

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage	-0.5 to +7.0	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-20	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	±20	mA
I_O	DC Output Source/Sink Current	±12.5	mA
I_{CC}	DC Supply Current Per Supply Pin	±25	mA
I_{GND}	DC Ground Current per Ground Pin	±25	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{LATCHUP1}$	Latchup Performance Above V_{CC} and Below GND at 125 °C (Note 5)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_{IN}	Digital Input Voltage	0	5.5	V
V_{OUT}	Output Voltage	0	5.5	V
T_A	Operating Free-Air Temperature	-55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 0	100 20	ns/V

NLU1G04

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = +85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Low-Level Input Voltage		1.65	0.75 x V _{CC}			0.75 x V _{CC}				V
			2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}				
V _{IL}	Low-Level Input Voltage		1.65			0.25 x V _{CC}		0.25 x V _{CC}		0.25 x V _{CC}	V
			2.3 to 5.5			0.30 x V _{CC}		0.30 x V _{CC}		0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5 V or GND	5.5			1.0		10		40	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 nS)

Symbol	Parameter	V _{CC} (V)	Test Condition	T _A = 25 °C			T _A = +85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{pLH} , t _{pHL}	Propagation Delay, Input A to Output Y	3.0 to 3.6	C _L = 15 pF		4.5	7.1		8.5		10.0	ns
			C _L = 50 pF		6.4	10.6		12.0		14.5	
		4.5 to 5.5	C _L = 15 pF		3.5	5.5		6.5		8.0	
			C _L = 50 pF		4.5	7.5		8.5		10.0	
C _{IN}	Input Capacitance				4	10		10		10.0	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	5.0			8.0						pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NLU1G04

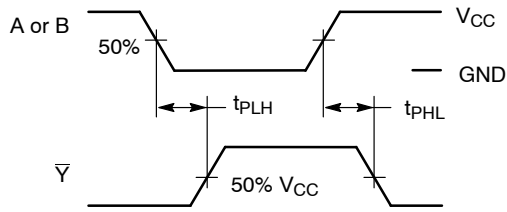
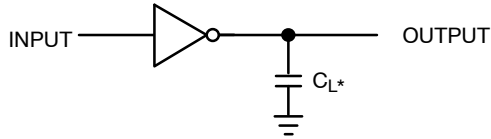


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance.
A 1-MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping [†]
NLU1G04MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLU1G04AMUTCG	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLU1G04CMUTCG	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

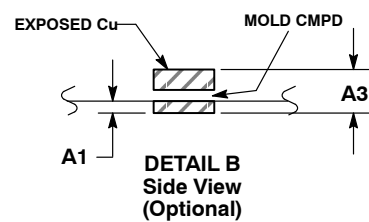
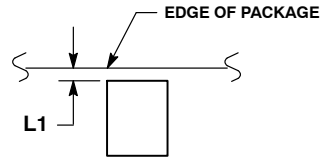
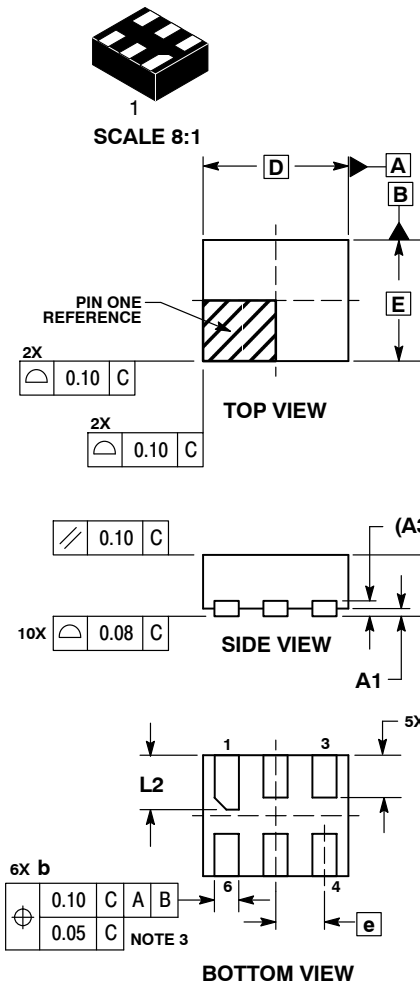
PACKAGE DIMENSIONS

ON Semiconductor®



UDFN6, 1.2x1.0, 0.4P CASE 517AA-01 ISSUE D

DATE 03 SEP 2010



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
D	1.20	BSC
E	1.00	BSC
e	0.40	BSC
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

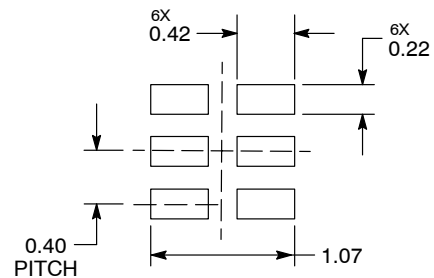
GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

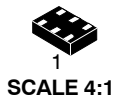
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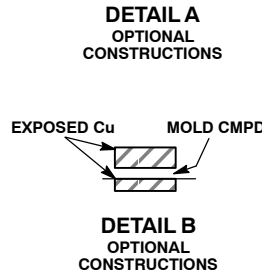
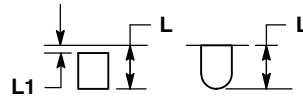
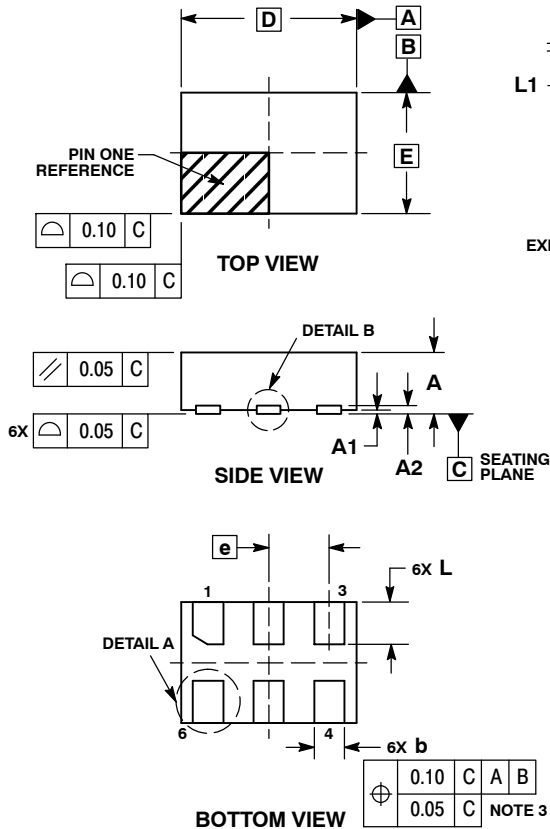
PACKAGE DIMENSIONS

ON Semiconductor®



UDFN6, 1.45x1.0, 0.5P
CASE 517AQ-01
ISSUE O

DATE 15 MAY 2008



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15

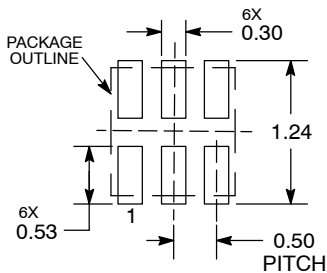
GENERIC MARKING DIAGRAM*



- X = Specific Device Code
- M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

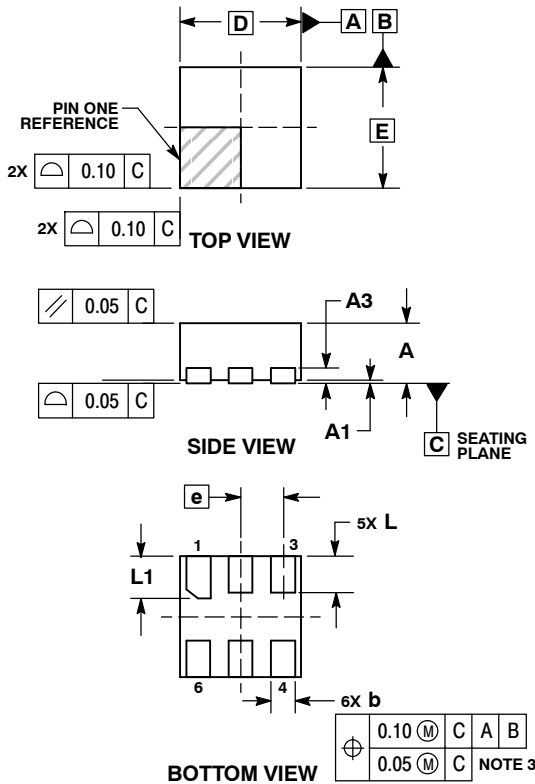
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SCALE 4:1

UDFN6, 1x1, 0.35P
CASE 517BX-01
ISSUE O

DATE 18 MAY 2011

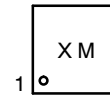


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.12	0.22
D	1.00	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

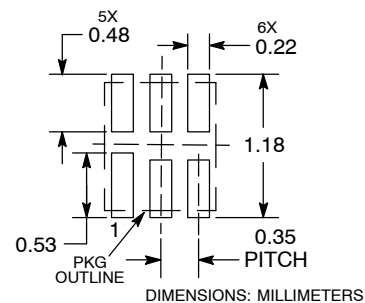
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*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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