

NLSV2T240

2-Bit Dual-Supply Inverting Level Translator

The NLSV2T240 is a 2-bit configurable dual-supply voltage level translator. The input A_n and output B_n ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low-voltage translation from the input A_n to the output B_n port.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non-preferential V_{CCA} and V_{CCB} Sequencing
- Outputs at 3-State until Active V_{CC} is Reached
- Power-Off Protection
- Outputs Switch to 3-State with V_{CCB} at GND
- Ultra-Small Packaging: 1.8 mm x 1.2 mm UDFN8
- This is a Pb-Free Device

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

- ESD Protection for All Pins:
HBM (Human Body Model) > 5000 V

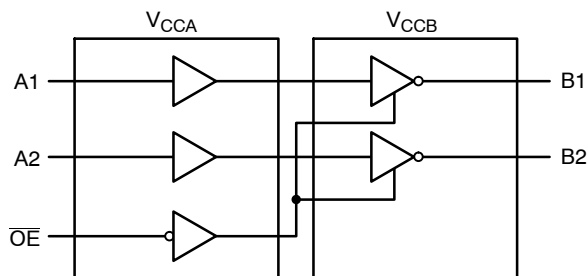


Figure 1. Logic Diagram



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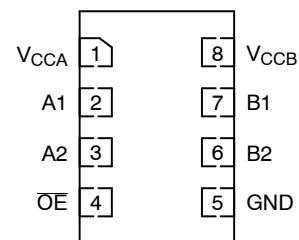
UDFN8
MU SUFFIX
CASE 517AJ

MARKING DIAGRAM



VC = Specific Device Code
M = Date Code
▪ = Pb-Free Package

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NLSV2T240MUTAG	UDFN8 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NLSV2T240

PIN ASSIGNMENT

PIN	FUNCTION
V _{CCA}	Input Port DC Power Supply
V _{CCB}	Output Port DC Power Supply
GND	Ground
A _n	Input Port
B _n	Output Port
\overline{OE}	Output Enable

TRUTH TABLE

Inputs		Outputs
\overline{OE}	A _n	B _n
L	L	H
L	H	L
H	X	3-State

MAXIMUM RATINGS

Symbol	Rating	Value	Condition	Unit
V _{CCA} , V _{CCB}	DC Supply Voltage	-0.5 to +5.5		V
V _I	DC Input Voltage A _n	-0.5 to +5.5		V
V _C	Control Input \overline{OE}	-0.5 to +5.5		V
V _O	DC Output Voltage (Power Down) B _n	-0.5 to +5.5	V _{CCA} = V _{CCB} = 0	V
	(Active Mode) B _n	-0.5 to +5.5		V
	(Tri-State Mode) B _n	-0.5 to +5.5		V
I _{IK}	DC Input Diode Current	-20	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CCA} , I _{CCB}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	-65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CCA} , V _{CCB}	Positive DC Supply Voltage	0.9	4.5	V
V _I	Bus Input Voltage	GND	4.5	V
V _C	Control Input \overline{OE}	GND	4.5	V
V _{IO}	Bus Output Voltage (Power Down Mode) B _n	GND	4.5	V
	(Active Mode) B _n	GND	V _{CCB}	V
	(Tri-State Mode) B _n	GND	4.5	V
T _A	Operating Temperature Range	-40	+85	°C
Δt / ΔV	Input Transition Rise or Rate V _I , from 30% to 70% of V _{CC} ; V _{CC} = 3.3 V ±0.3 V	0	10	nS

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CCA} (V)	V _{CCB} (V)	-40°C to +85°C		Unit
					Min	Max	
V _{IH}	Input HIGH Voltage (An, OE)		3.6 – 4.5	0.9 – 4.5	2.2	–	V
			2.7 – 3.6		2.0	–	
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		0.65 * V _{CCA}	–	
			0.9 – 1.4		0.9 * V _{CCA}	–	
V _{IL}	Input LOW Voltage (An, OE)		3.6 – 4.5	0.9 – 4.5	–	0.8	V
			2.7 – 3.6		–	0.8	
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	0.35 * V _{CCA}	
			0.9 – 1.4		–	0.1 * V _{CCA}	
V _{OH}	Output HIGH Voltage	I _{OH} = -100 μA; V _I = V _{IL}	0.9 – 4.5	0.9 – 4.5	V _{CCB} - 0.2	–	V
		I _{OH} = -0.5 mA; V _I = V _{IL}	0.9	0.9	0.75 * V _{CCB}	–	
		I _{OH} = -2 mA; V _I = V _{IL}	1.4	1.4	1.05	–	
		I _{OH} = -6 mA; V _I = V _{IL}	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I _{OH} = -12 mA; V _I = V _{IL}	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I _{OH} = -18 mA; V _I = V _{IL}	2.3	2.3	1.7	–	
3.0	3.0		2.4	–			
V _{OL}	Output LOW Voltage	I _{OL} = 100 μA; V _I = V _{IH}	0.9 – 4.5	0.9 – 4.5	–	0.2	V
		I _{OL} = 0.5 mA; V _I = V _{IH}	1.1	1.1	–	0.3	
		I _{OL} = 2 mA; V _I = V _{IH}	1.4	1.4	–	0.35	
		I _{OL} = 6 mA; V _I = V _{IH}	1.65	1.65	–	0.3	
			2.3	2.3	–	0.4	
		I _{OL} = 12 mA; V _I = V _{IH}	2.7	2.7	–	0.4	
			2.3	2.3	–	0.6	
		I _{OL} = 18 mA; V _I = V _{IH}	3.0	3.0	–	0.4	
3.0	3.0		–	0.55			
I _I	Input Leakage Current	V _I = V _{CCA} or GND	0.9 – 4.5	0.9 – 4.5	-1.0	1.0	μA
I _{OFF}	Power-Off Leakage Current	OE = 0 V	0 0.9 – 4.5	0.9 – 4.5 0	-1.0 -1.0	1.0 1.0	μA
I _{CCA}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0, V _{CCA} = V _{CCB}	0.9 – 4.5	0.9 – 4.5	–	1.0	μA
I _{CCB}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0, V _{CCA} = V _{CCB}	0.9 – 4.5	0.9 – 4.5	–	1.0	μA
I _{CCA} + I _{CCB}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0, V _{CCA} = V _{CCB}	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
ΔI _{CCA}	Increase in I _{CC} per Input Voltage, Other Inputs at V _{CCA} or GND	V _I = V _{CCA} - 0.6 V; V _I = V _{CCA} or GND	4.5	4.5	–	10	μA
			3.6	3.6	–	5.0	
ΔI _{CCB}	Increase in I _{CC} per Input Voltage, Other Inputs at V _{CCA} or GND	V _I = V _{CCA} - 0.6 V; V _I = V _{CCA} or GND	4.5	4.5	–	10	μA
			3.6	3.6	–	5.0	
I _{OZ}	I/O Tri-State Output Leakage Current	T _A = 25°C, OE = 0 V	0.9 – 4.5	0.9 – 4.5	-1.0	1.0	μA

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TOTAL STATIC POWER CONSUMPTION ($I_{CCA} + I_{CCB}$)

V_{CCA} (V)	-40°C to +85°C										Unit
	V_{CCB} (V)										
	4.5		3.3		2.8		1.8		0.9		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
4.5		2		2		2		2		< 1.5	μ A
3.3		2		2		2		2		< 1.5	μ A
2.8		< 2		< 1		< 1		< 0.5		< 0.5	μ A
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	μ A
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	μ A

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB} . This device is designed with the feature that the power-up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CCA} (V)	-40°C to +85°C										Unit
			V_{CCB} (V)										
			4.5		3.3		2.8		1.8		1.2		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL} (Note 1)	Propagation Delay, A_n to B_n	4.5		1.6		1.8		2.0		2.1		2.3	nS
		3.3		1.7		1.9		2.1		2.3		2.6	
		2.8		1.9		2.1		2.3		2.5		2.8	
		1.8		2.1		2.4		2.5		2.7		3.0	
		1.2		2.4		2.7		2.8		3.0		3.3	
t_{PZH} , t_{PZL} (Note 1)	Output Enable, \overline{OE} to B_n	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{PHZ} , t_{PLZ} (Note 1)	Output Disable, \overline{OE} to B_n	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{OSHL} , t_{OSLH} (Note 1)	Output to Output Skew, Time	4.5		0.15		0.15		0.15		0.15		0.15	nS
		3.3		0.15		0.15		0.15		0.15		0.15	
		2.5		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

1. Propagation delays defined per Figure 2.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
C_{IN}	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or V_{CCA} , $f = 10$ MHz	20	pF

2. Typical values are at $T_A = +25^\circ\text{C}$.

3. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:
 $I_{CC(\text{operating})} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

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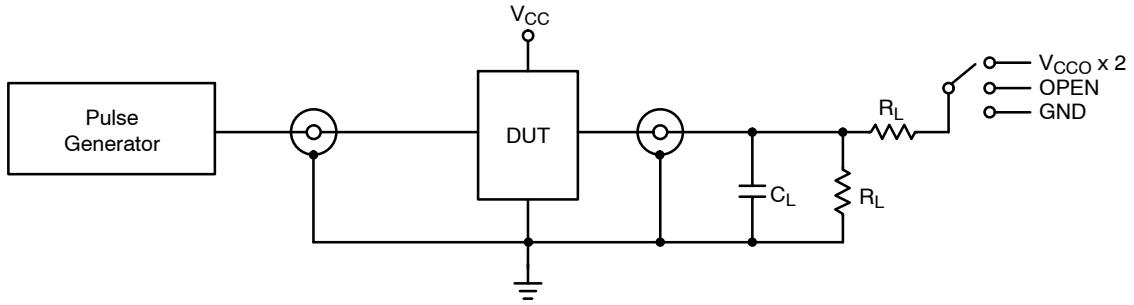
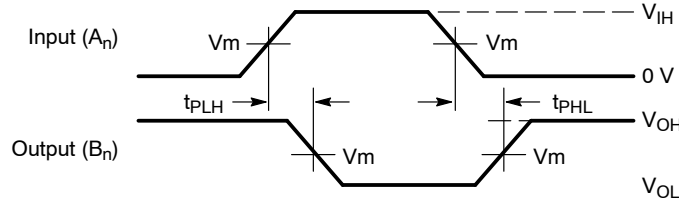


Figure 2. AC (Propagation Delay) Test Circuit

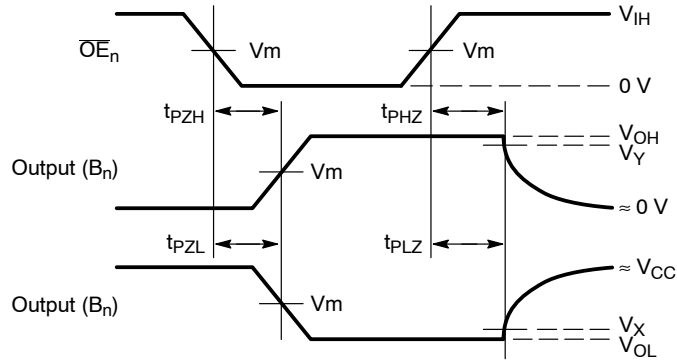
Test	Switch
t_{PLH} , t_{PHL}	OPEN
t_{PLZ} , t_{PZL}	$V_{CC} \times 2$
t_{PHZ} , t_{PZH}	GND

$C_L = 15 \text{ pF}$ or equivalent (includes probe and jig capacitance)
 $R_L = 2 \text{ k}\Omega$ or equivalent
 Z_{OUT} of pulse generator = 50Ω



Waveform 1 - Propagation Delays

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



Waveform 2 - Output Enable and Disable Times

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

Figure 3. AC (Propagation Delay) Test Circuit Waveforms

Symbol	V_{CC}				
	3.0 V - 4.5 V	2.3 V - 2.7 V	1.65 V - 1.95 V	1.4 V - 1.6 V	0.9 V - 1.3 V
V_{mA}	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$
V_{mB}	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$
V_X	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$
V_Y	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

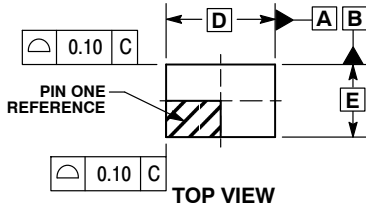
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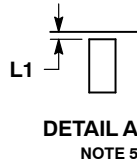
SCALE 4:1

UDFN8 1.8x1.2, 0.4P
CASE 517AJ-01
ISSUE O

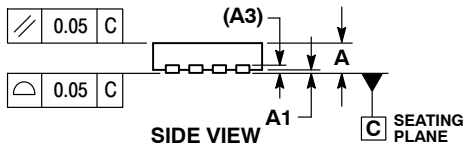
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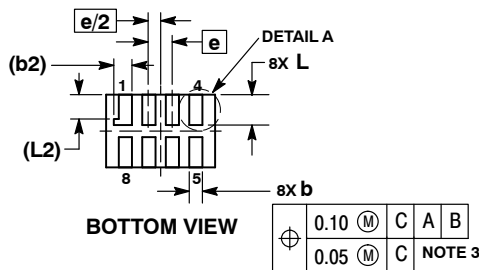
TOP VIEW



DETAIL A
NOTE 5



SIDE VIEW



BOTTOM VIEW

⊕	0.10	(M)	C	A	B
	0.05	(M)	C		

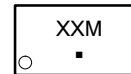
NOTE 3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

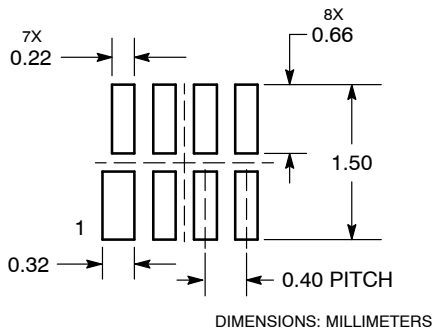
DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
b2	0.30	REF
D	1.80	BSC
E	1.20	BSC
e	0.40	BSC
L	0.45	0.55
L1	0.00	0.03
L2	0.40	REF

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

MOUNTING FOOTPRINT
SOLDERMASK DEFINED



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	UDFN8 1.8X1.2, 0.4P	PAGE 1 OF 1

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