

Configurable Multifunction Gate

NL7SZ57

The NL7SZ57 is an advanced high-speed CMOS multifunction gate. The device allows the user to choose logic functions AND, OR, NAND, NOR, XNOR, INVERT and BUFFER. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 3.3 ns t_{PD} at $V_{CC} = 5$ V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Sink 24 mA at 3.0 V
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



ON Semiconductor®

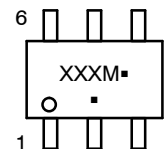
www.onsemi.com

MARKING DIAGRAMS



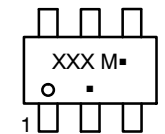
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SC-88/SC70-6/
SOT-363
CASE 419B-02



1

SC-74
CASE 318F-05



1

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ



1

UDFN6, 1x1, 0.35P
CASE 517BX



XXX = Specific Device Code

M = Date Code*

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NL7SZ57

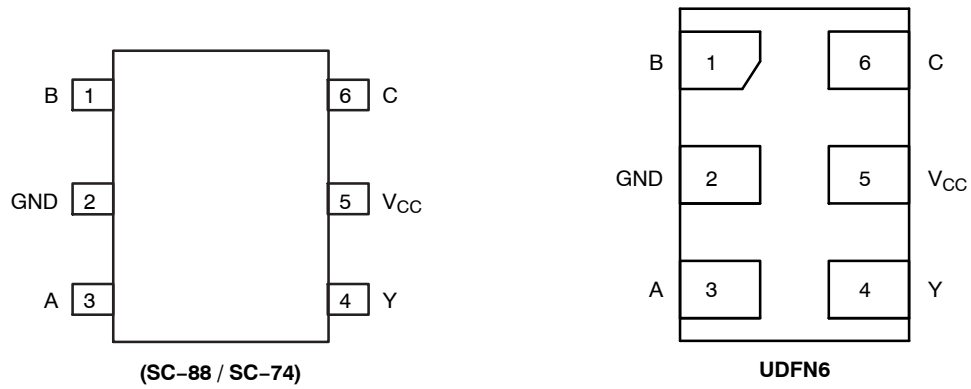


Figure 1. Pinout (Top View)

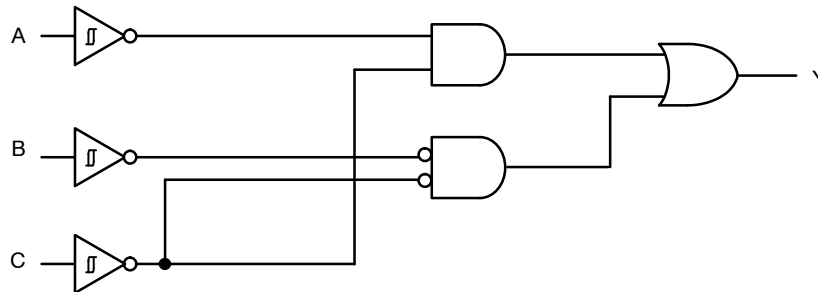


Figure 2. Function Diagram

PIN ASSIGNMENT

Pin	Function
1	B
2	GND
3	A
4	Y
5	V _{CC}
6	C

FUNCTION TABLE*

Input			Output
A	B	C	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

*To select a logic function, please refer to "Logic Configurations section".

LOGIC CONFIGURATIONS

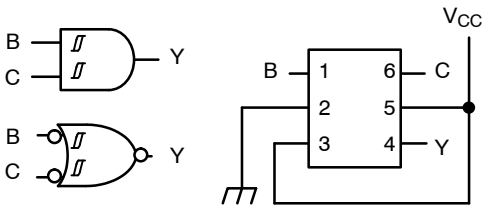


Figure 3. 2-Input AND (When A = "H")

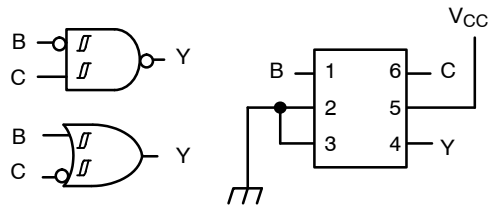


Figure 4. 2-Input NAND with input B inverted (When A = "L")

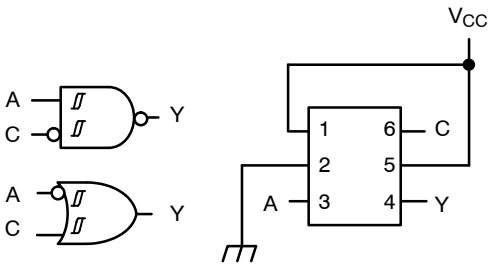


Figure 5. 2-Input NAND with Input C Inverted (When B = "H")

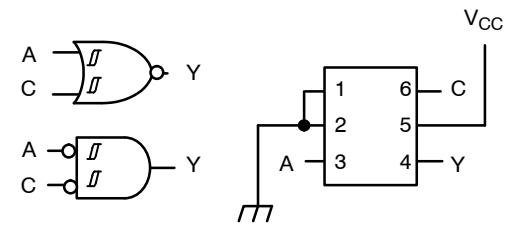


Figure 6. 2-Input NOR (When B = "L")

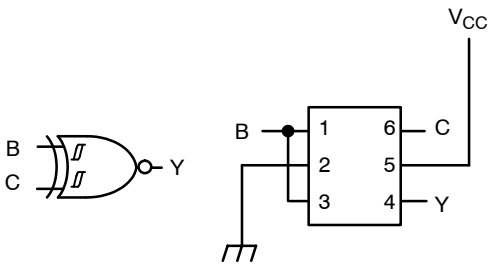


Figure 7. 2-Input XNOR (When A = B)

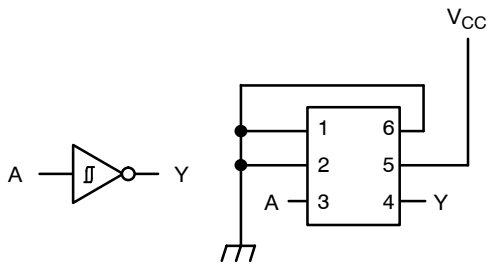


Figure 8. Inverter (When B = C = "L")

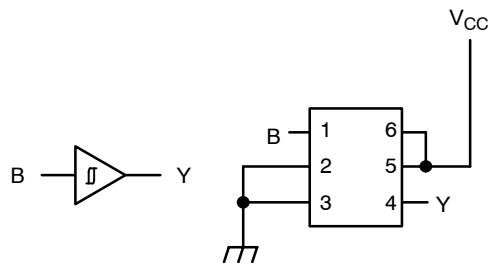


Figure 9. Buffer (When A = "L" and C = "H")

NL7SZ57

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V_{CC}	DC Supply Voltage SC-88 (NLV) SC-88, SC-74, UDFN6	-0.5 to +7.0 -0.5 to +6.5	V	
V_{IN}	DC Input Voltage SC-88 (NLV) SC-88, SC-74, UDFN6	-0.5 to +7.0 -0.5 to +6.5	V	
V_{OUT}	DC Output Voltage SC-88 (NLV) Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +7.0 -0.5 to +7.0	V	
	DC Output Voltage SC-88, SC-74, UDFN6 Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V	
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA	
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA	
I_{OUT}	DC Output Source/Sink Current	± 50	mA	
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	± 100	mA	
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}C$	
T_L	Lead Temperature, 1 mm from Case for 10 Secs	260	$^{\circ}C$	
T_J	Junction Temperature Under Bias	+150	$^{\circ}C$	
θ_{JA}	Thermal Resistance (Note 2)	SC-88	377	$^{\circ}C/W$
		SC-74	320	
		UDFN6	154	
P_D	Power Dissipation in Still Air	SC-88	332	mW
		SC-74	390	
		UDFN6	812	
MSL	Moisture Sensitivity	Level 1		
F_R	Flammability Rating Oxygen Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in		
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Mode Charged Device Model (NLV) Charged Device Model	>2000 >200 N/A	V	
$I_{LATCHUP}$	Latchup Performance (Note 4) (NLV)	± 500 ± 100	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow per JESD51-7.
3. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	0	V_{CC}	V
		0	5.5	
		0	5.5	
T_A	Operating Free-Air Temperature	-55	+125	$^{\circ}C$
t_r, t_f	Input Rise or Fall Rate $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V $V_{CC} = 3.0$ V to 3.6 V $V_{CC} = 4.5$ V to 5.5 V	0	No Limit	nS/V
		0	No Limit	
		0	No Limit	
		0	No Limit	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	Positive Input Threshold Voltage		1.65	-	-	1.4	-	1.4	-	1.4	V
			2.3	-	-	1.8	-	1.8	-	1.8	
			3.0	-	-	2.2	-	2.2	-	2.2	
			4.5	-	-	3.1	-	3.1	-	3.1	
			5.5	-	-	3.6	-	3.6	-	3.6	
V _{T-}	Negative Input Threshold Voltage		1.65	0.2	-	-	0.2	-	0.2	-	V
			2.3	0.4	-	-	0.4	-	0.4	-	
			3.0	0.6	-	-	0.6	-	0.6	-	
			4.5	1.0	-	-	1.0	-	1.0	-	
			5.5	1.2	-	-	1.2	-	1.2	-	
V _H	Input Hysteresis Voltage		1.65	0.1	0.48	0.9	0.1	0.9	0.1	-	V
			2.3	0.25	0.75	1.1	0.25	1.1	0.25	-	
			3	0.4	0.93	1.2	0.4	1.2	0.4	-	
			4.5	0.6	1.2	1.5	0.6	1.5	0.6	-	
			5.5	0.7	1.4	1.7	0.7	1.7	0.7	-	
V _{OH}	High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}	-	V _{CC} - 0.1	-	V _{CC} - 0.1	-	V
		I _{OH} = -4 mA	1.65	1.20	1.52	-	1.20	-	1.20	-	
		I _{OH} = -8 mA	2.3	1.9	2.1	-	1.9	-	1.9	-	
		I _{OH} = -16 mA	3	2.4	2.7	-	2.4	-	2.4	-	
		I _{OH} = -24 mA	3	2.3	2.5	-	2.3	-	2.3	-	
		I _{OH} = -32 mA	4.5	3.8	4	-	3.8	-	3.8	-	
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.65 to 5.5	-	-	0.1	-	0.1	-	0.1	V
		I _{OL} = 4 mA	1.65	-	0.08	0.45	-	0.45	-	0.45	
		I _{OL} = 8 mA	2.3	-	0.2	0.3	-	0.3	-	0.4	
		I _{OL} = 16 mA	3	-	0.28	0.4	-	0.4	-	0.5	
		I _{OL} = 24 mA	3	-	0.38	0.55	-	0.55	-	0.55	
		I _{OL} = 32 mA	4.5	-	0.42	0.55	-	0.55	-	0.65	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	-	-	+0.1	-	+1.0	-	+1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0	-	-	1.0	-	10	-	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5 V or GND	5.5	-	-	1.0	-	10	-	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NL7SZ57

AC ELECTRICAL CHARACTERISTICS

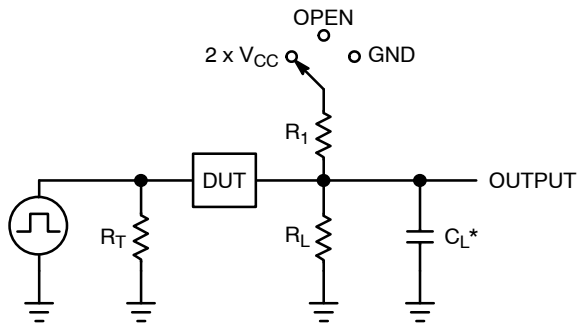
Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, (A or B or C) to Y (Figures 10 and 11)	R _L = 1 kΩ, C _L = 30 pF	1.65 to 1.95	-	8.6	14.4	-	14.4	-	14.4	ns
		R _L = 500 Ω, C _L = 30 pF	2.3 to 2.7	-	5.1	8.3	-	8.3	-	8.3	
		R _L = 500 Ω, C _L = 50 pF	3.0 to 3.6	-	3.9	6.3	-	6.3	-	6.3	
			4.5 to 5.5	-	3.3	5.1	-	5.1	-	5.1	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	4.0	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V _{CC} = 3.3 V, V _{IN} = 0 V or V _{CC} 10 MHz, V _{CC} = 5.0 V, V _{IN} = 0 V or V _{CC}	16 19.5	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Figure 10. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω	R_1 , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care



Figure 11. Switching Waveforms

V_{CC} , V	V_{mi} , V	V_{mo} , V		V_Y , V
		t_{PLH}, t_{PHL}	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.15
2.3 to 2.7	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.15
3.0 to 3.6	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.3
4.5 to 5.5	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.3

NL7SZ57

ORDERING INFORMATION

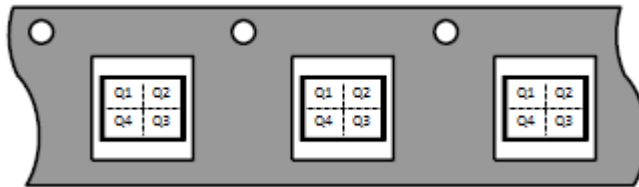
Device	Package			Shipping†
NL7SZ57DFT2G	SC-88 (Pb-Free)	MN	Q4	3000 / Tape & Reel
NLV7SZ57DFT2G*	SC-88 (Pb-Free)	MN	Q4	3000 / Tape & Reel
NL7SZ57DBVT1G	SC-74 (Pb-Free)	AL	Q4	3000 / Tape & Reel
NL7SZ57MU1TCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	TBD	Q4	3000 / Tape & Reel
NL7SZ57MU3TCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	P (Rotated 270° CW)	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel

Direction of Feed



MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

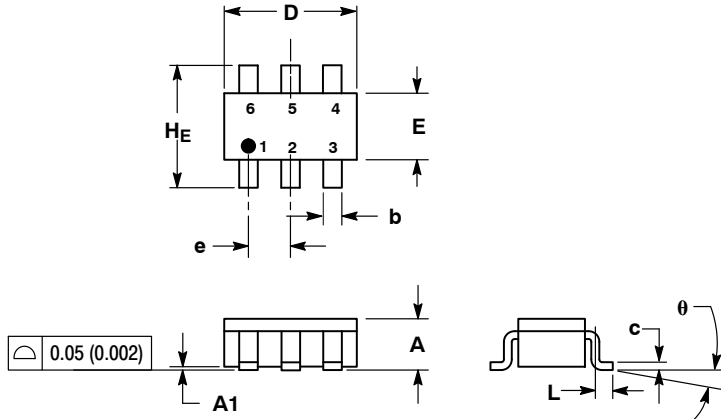


SC-74 CASE 318F-05 ISSUE N

DATE 08 JUN 2012



SCALE 2:1

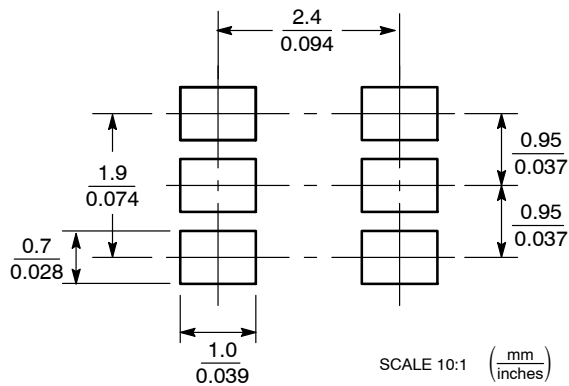


NOTES:

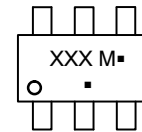
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03, -04 OBSOLETE. NEW STANDARD 318F-05.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- | | | | | | |
|--|---|--|---|--|--|
| <p>STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE</p> | <p>STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE</p> | <p>STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1</p> | <p>STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3</p> | <p>STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4</p> | <p>STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE</p> |
| <p>STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1</p> | <p>STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1</p> | <p>STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

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DESCRIPTION:	SC-74	PAGE 1 OF 1

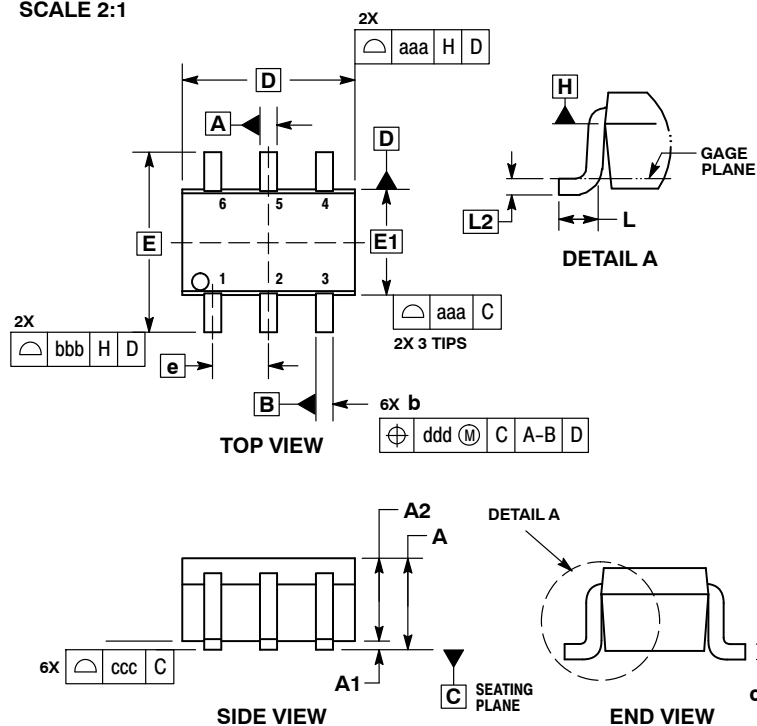
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 SCALE 2:1

SC-88/SC70-6/SOT-363
 CASE 419B-02
 ISSUE Y

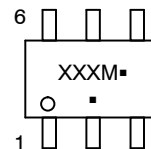
DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*



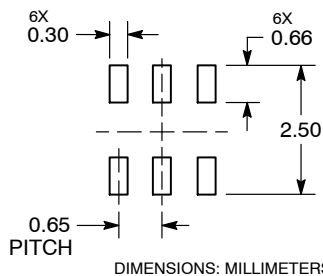
XXX = Specific Device Code
 M = Date Code*
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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