

# 1 Ω SPDT Switch

## NL5S4157A

The NL5S4157A is a low  $R_{ON}$  SPDT analog switch. The device is designed for low operating voltage, high current switching of speaker output for mobile applications. It can switch a balanced stereo output. It can handle a balanced microphone/speaker/ringtone generator in monophone mode.

### Features

- Wide  $V_{CC}$  Operating Range: 1.65 V to 5.5 V
- OVT up to +5.5 V for Control pin
- $R_{ON}$ : Typically  $< 1 \Omega$  at  $V_{CC} = 4.5 V$
- Rail-to-Rail Input/Output
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone-Chip/Amplifier Switching
- Stereo Balanced (Push-Pull) Switching
- RF PA Routing
- General Switching



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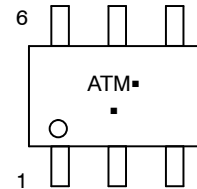
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1

SC-88/SC70-6/SOT-363  
CASE 419B-02

### MARKING DIAGRAM



AT = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)  
\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# NL5S4157A

## PIN ASSIGNMENTS

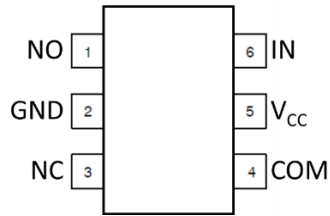


Figure 1. NL5S4157A (Top View)

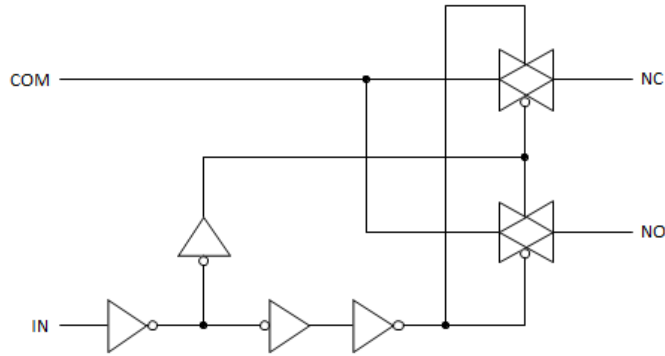


Figure 2. Analog Symbol

### PIN DESCRIPTION

Pin	Name	Description
1	NO	Normally-Open Port
2	GND	Supply Ground
3	NC	Normally-Closed Port
4	COM	Common Port
5	V <sub>CC</sub>	Supply
6	IN	Switch Select Input

### FUNCTION TABLE

IN	Switch
L	NC to COM
H	NO to COM

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## MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{CC}$	Positive DC Supply Voltage	-0.5 to +6.0	V
$V_{IS}$	Switch Input / Output Voltage	-0.5 to $V_{CC}+0.5$	V
$V_{IN}$	Digital Select Input Voltage	-0.5 to +6.0	V
$I_{OK}$	I/O Port Diode Current	$\pm 100$	mA
$I_{IK}$	Select Input Diode Current	-100	mA
$I_{I/O}$	Continuous DC Current Through Analog Switch	$\pm 100$	mA
$I_{I/O-pk}$	Peak Current Through Analog Switch, 10% Duty Cycle	$\pm 300$	mA
$T_s$	Storage Temperature	-65 to +150	$^{\circ}C$
ESD	Human Body Model (HBM)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V	
$V_{IS}$	Switch Input / Output Voltage	GND	$V_{CC}$	V	
$V_{IN}$	Digital Select Input Voltage	GND	5.5	V	
$T_A$	Operating Temperature Range	-40	+125	$^{\circ}C$	
$t_r, t_f$	Input Transition Rise or Fall Time (Select Input IN)	$V_{CC} \leq 3.0\text{ V}$	0	20	ns/V
		$V_{CC} > 3.0\text{ V}$	0	10	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	Guaranteed Limit						Unit	
				25°C			-40°C to 85°C		-40°C to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
V <sub>IH</sub>	Input High Voltage		2.7	1.1			1.1		1.1		V
			5.0	1.42			1.42		1.42		
V <sub>IL</sub>	Input Low Voltage		2.7			0.4		0.4		0.4	V
			5.0			0.7		0.7		0.7	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to 5.5 V	1.65 – 5.5			±0.1		±1		±1	µA
I <sub>OFF</sub>	Input Leakage Current	V <sub>IN</sub> = 0 to 5.5 V	0			0.05		1		1	µA
I <sub>S(ON)</sub>	ON-State Switch Leakage Current	V <sub>IS</sub> = GND to V <sub>CC</sub> , V <sub>OS</sub> = Open	5.5			±10		±200		±600	nA
I <sub>S(OFF)</sub>	OFF-State Switch Leakage Current	V <sub>IS</sub> = V <sub>CC</sub> and V <sub>OS</sub> = GND, or I <sub>S</sub> = GND and V <sub>OS</sub> = V <sub>CC</sub>	5.5			±10		±200		±600	nA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OS</sub> = 0 mA	5.5			0.5		5		5	µA

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## ANALOG SWITCH CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	Guaranteed Limit					Unit
				25°C			-40°C to 125°C		
				Min	Typ	Max	Min	Max	
R <sub>ON</sub> (Note 1)	Switch ON Resistance	V <sub>IS</sub> = 0 to V <sub>CC</sub> , I <sub>O</sub> = 100 mA	2.7		0.9	1.2		1.4	Ω
			4.5		0.6	0.8		1.0	
ΔR <sub>ON</sub> (Notes 1, 2, 3)	ON Resistance Match	V <sub>IS</sub> = 1.5 V, I <sub>A</sub> = 100 mA	2.7		0.05	0.15		0.15	Ω
	Between Channels	V <sub>IS</sub> = 2.5 V, I <sub>A</sub> = 100 mA	4.5		0.04	0.12		0.15	
R <sub>FLAT</sub> (Notes 1, 2, 4)	ON Resistance Flatness	V <sub>IS</sub> = 0 to V <sub>CC</sub> , I <sub>O</sub> = 100 mA	2.7		0.3	0.4		0.4	Ω
			4.5		0.2	0.4		0.4	
Q (Note 5)	Charge Injection	C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 0 V,	2.7		38				pC
		R <sub>GEN</sub> = 0 Ω	4.5		55				
V <sub>ISO</sub> (Note 6)	Off-Isolation	R <sub>L</sub> = 50 Ω, f = 1 MHz	2.7 – 5.5		-66				dB
V <sub>CT</sub>	Crosstalk	R <sub>L</sub> = 50 Ω, f = 1 MHz	2.7 – 5.5		-66				dB
BW	-3 dB Bandwidth	R <sub>L</sub> = 50 Ω	2.7 – 5.5		57				MHz
THD (Note 5)	Total Harmonic Distortion	R <sub>L</sub> = 600 Ω, V <sub>IS</sub> = 0.5 V <sub>P-P</sub> , f = 20 Hz to 20 kHz	2.7 – 5.5		0.004				%
C <sub>I</sub>	Select Input Capacitance	f = 1 MHz	0		3.0				pF
C <sub>OFF</sub>	NC/NO Port Off Capacitance	f = 1 MHz	4.5		23				pF
C <sub>ON</sub>	COM Port ON Capacitance	f = 1 MHz	4.5		93				pF

1. Measured by the voltage drop between NC/NO and COM pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (NO, NC, COM).
2. Parameter is characterized but not tested in production.
3. ΔR<sub>ON</sub> = R<sub>ON</sub> max – R<sub>ON</sub> min measured at identical V<sub>CC</sub>, temperature and voltage levels.
4. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
5. Guaranteed by Design.
6. V<sub>ISO</sub> = 20 log<sub>10</sub> [V<sub>COM</sub>/V<sub>NO,NC</sub>].

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## SWITCHING CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	Guaranteed Limit					Unit
				25°C			-40°C to 125°C		
				Min	Typ	Max	Min	Max	
t <sub>PD</sub> (Note 7)	Propagation Delay	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7			2.0		2.0	ns
			4.5			0.3		0.3	
t <sub>ON</sub>	Turn-on Time, (COM to NO or NC)	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF,							ns
		V <sub>IS</sub> = 1.5 V	2.7			30		35	
		V <sub>IS</sub> = 3.0 V	4.5			20		25	
		R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 100 pF,							
		V <sub>IS</sub> = 1.5 V	3.3			100		100	
t <sub>OFF</sub>	Turn-off Time, (COM to NO or NC)	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF,							ns
		V <sub>IS</sub> = 1.5 V	2.7			20		25	
		V <sub>IS</sub> = 3.0 V	4.5			15		20	
		R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 100 pF,							
		V <sub>IS</sub> = 1.5 V	3.3			100		100	
T <sub>BBM</sub> (Note 5)	Break Before Make Time	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF	2.7	0.5			0.5		ns
			4.5	0.5			0.5		

7. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping <sup>†</sup>
NL5S4157ADFT2G	SC-88/SC70-6/SOT-363	AT	Q4	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PIN 1 ORIENTATION IN TAPE AND REEL

Pin 1 Orientation in Tape and Reel  
Direction of Feed

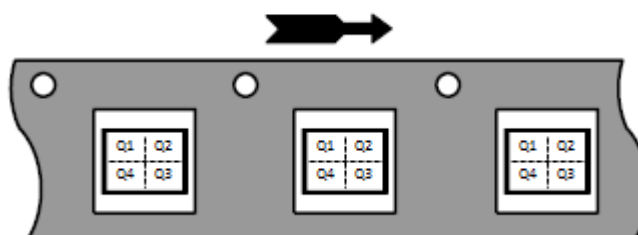


Figure 3.

# NL5S4157A

## Test Setups

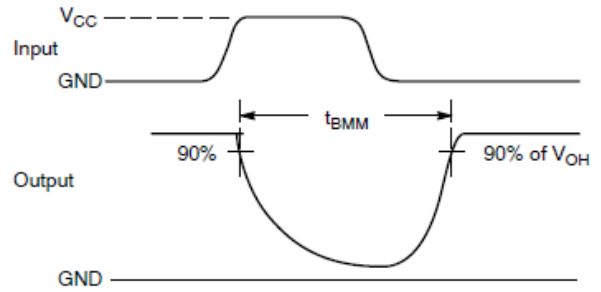
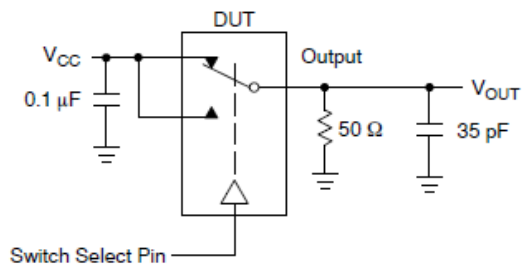


Figure 4.  $t_{BMM}$  (Time Break-Before-Make)

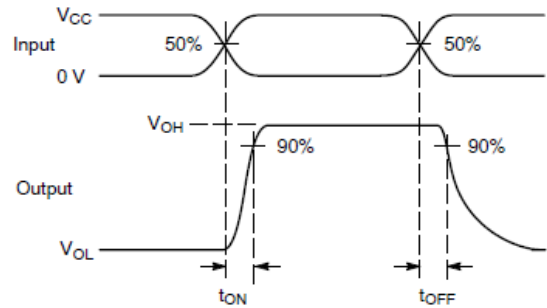
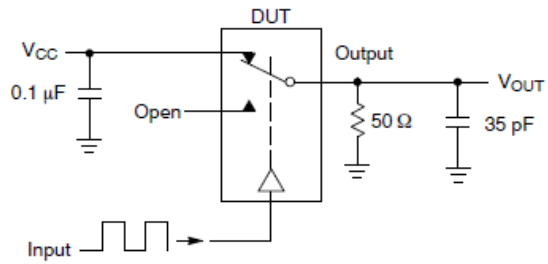


Figure 5.  $t_{ON}/t_{OFF}$

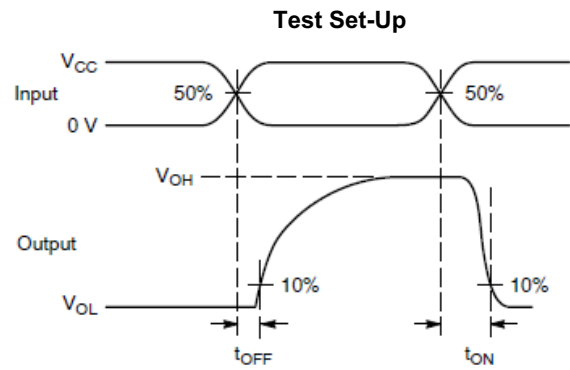
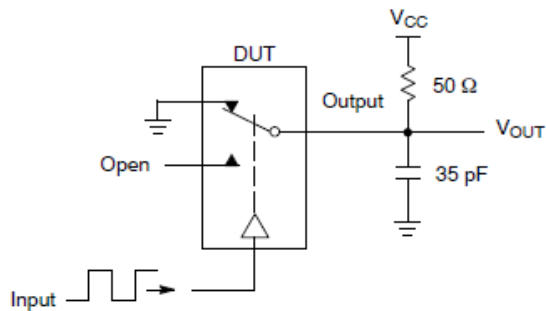
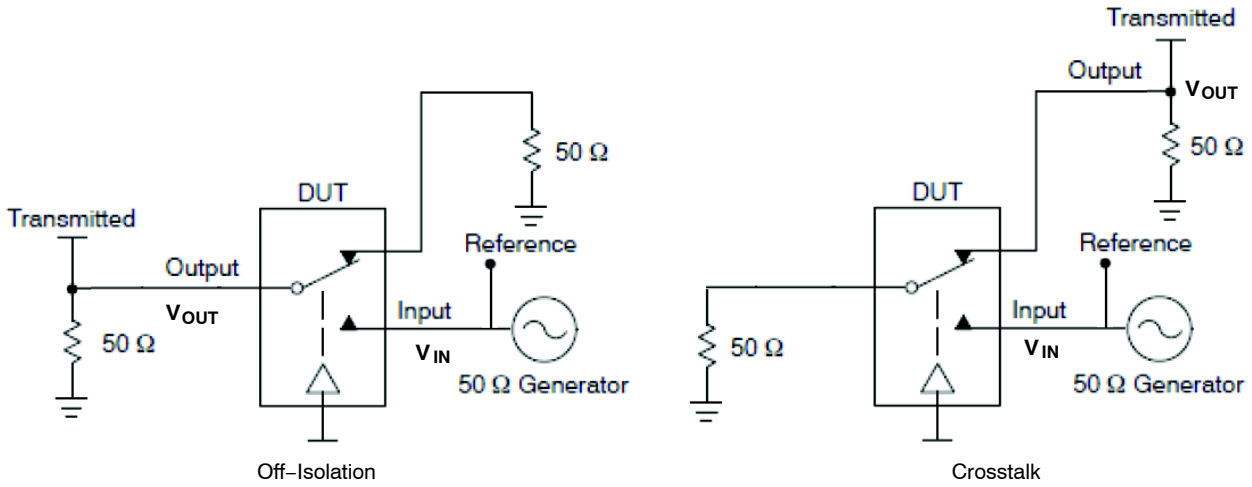


Figure 6.  $t_{ON}/t_{OFF}$



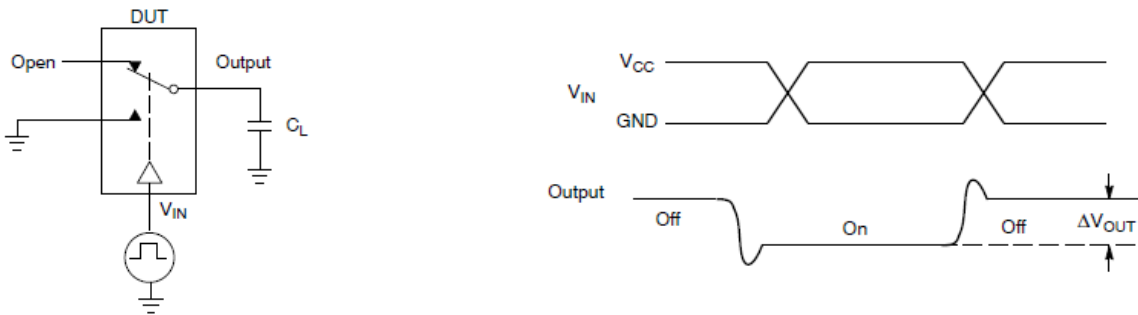
Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. Crosstalk is measured from an off channel to an on channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ ,  $V_{CT}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} \text{ or } V_{CT} = \text{Off Channel Isolation or crosstalk} = 20 \text{ Log for } V_{OUT} / V_{IN}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log for } V_{OUT} / V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

**Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$**



**Figure 8. Charge Injection: (Q)**



TYPICAL CHARACTERISTICS

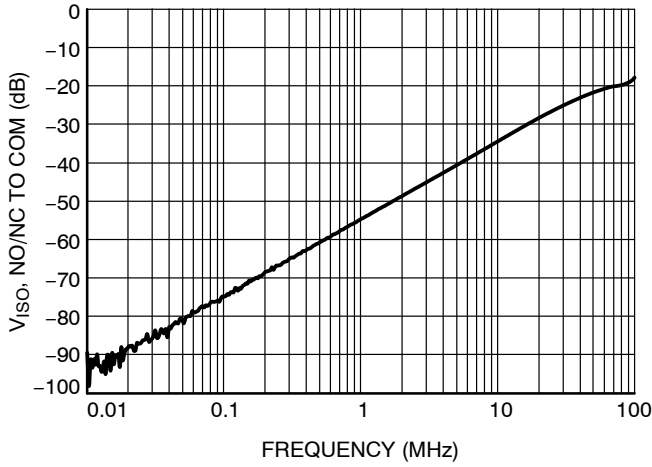


Figure 9.  $V_{ISO}$  vs. Frequency  
@  $V_{CC} = 4.5\text{ V}$

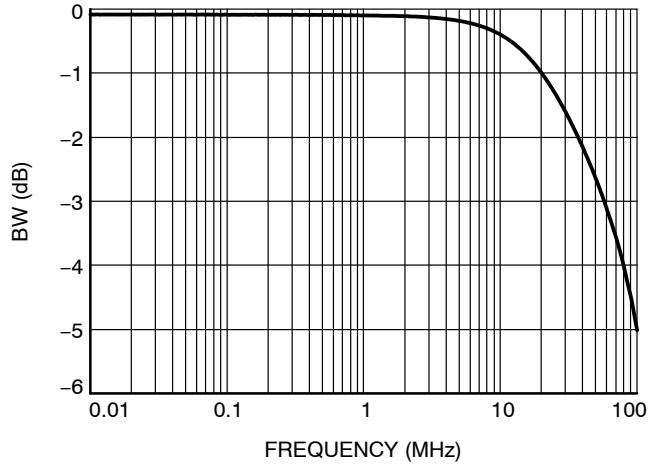


Figure 10. Bandwidth vs. Frequency

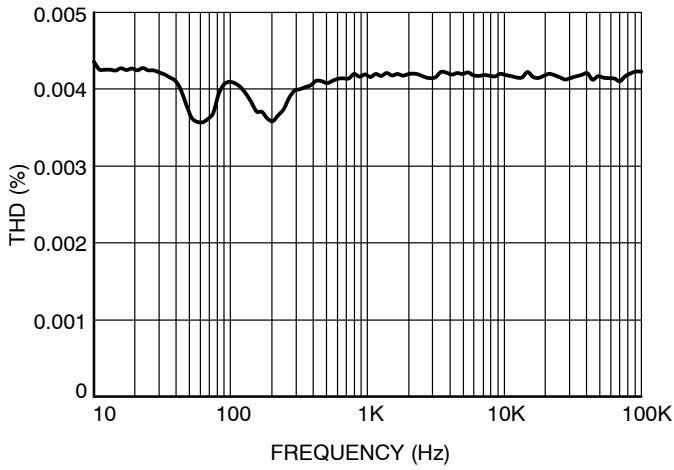


Figure 11. Total Harmonic Distortion

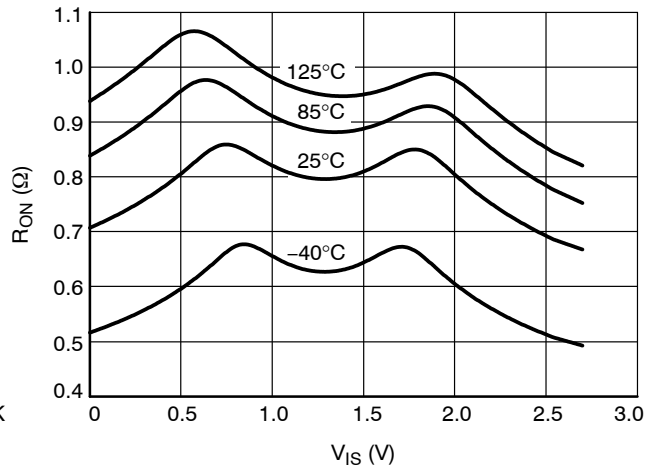


Figure 12. ON Resistance vs. Switch Voltage  
@  $V_{CC} = 2.7\text{ V}$

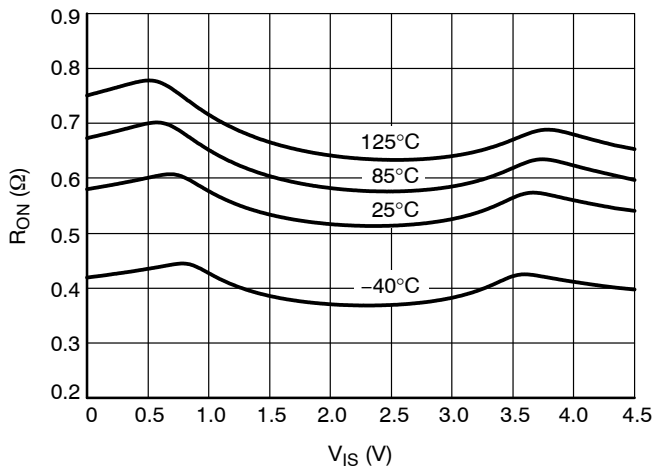


Figure 13. ON Resistance vs. Switch Voltage  
@  $V_{CC} = 4.5\text{ V}$

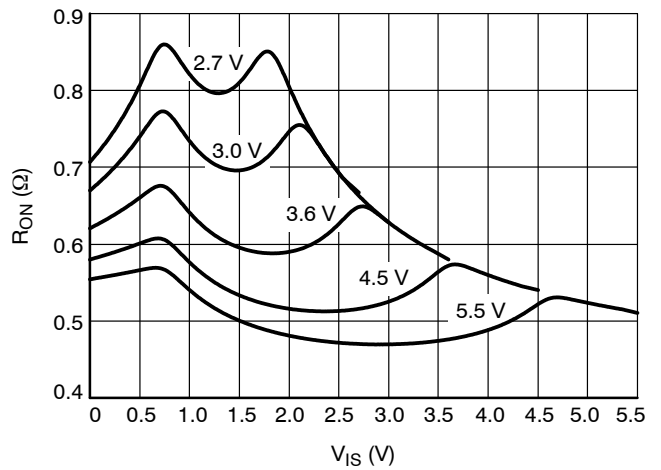


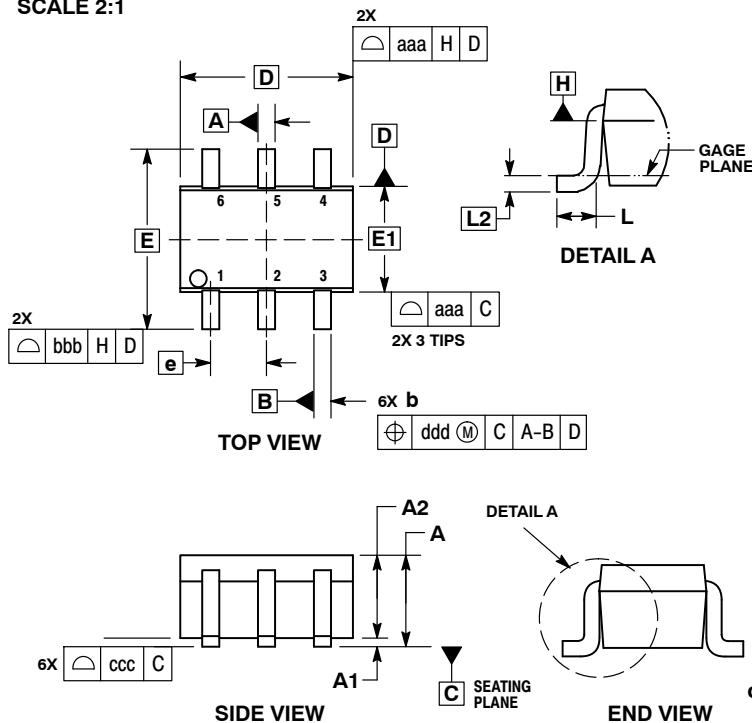
Figure 14. ON Resistance vs. Switch Voltage



1  
 SCALE 2:1

SC-88/SC70-6/SOT-363  
 CASE 419B-02  
 ISSUE Y

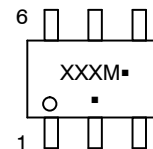
DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

**GENERIC MARKING DIAGRAM\***



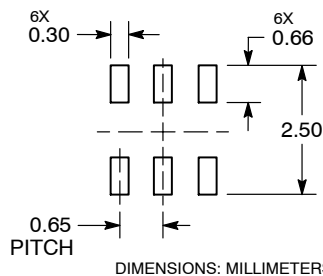
- XXX = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

<b>DOCUMENT NUMBER:</b>	<b>98ASB42985B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-88/SC70-6/SOT-363</b>	<b>PAGE 1 OF 2</b>

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**SC-88/SC70-6/SOT-363**  
**CASE 419B-02**  
**ISSUE Y**


DATE 11 DEC 2012

<b>STYLE 1:</b> PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	<b>STYLE 2:</b> CANCELLED	<b>STYLE 3:</b> CANCELLED	<b>STYLE 4:</b> PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	<b>STYLE 5:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 6:</b> PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
<b>STYLE 7:</b> PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	<b>STYLE 10:</b> PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	<b>STYLE 11:</b> PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	<b>STYLE 12:</b> PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
<b>STYLE 13:</b> PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 14:</b> PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	<b>STYLE 16:</b> PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	<b>STYLE 17:</b> PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	<b>STYLE 18:</b> PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
<b>STYLE 19:</b> PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	<b>STYLE 20:</b> PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	<b>STYLE 21:</b> PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	<b>STYLE 22:</b> PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	<b>STYLE 23:</b> PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	<b>STYLE 24:</b> PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
<b>STYLE 25:</b> PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	<b>STYLE 26:</b> PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	<b>STYLE 27:</b> PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	<b>STYLE 28:</b> PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	<b>STYLE 29:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	<b>STYLE 30:</b> PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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