LC71F7001PVBS0

Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors

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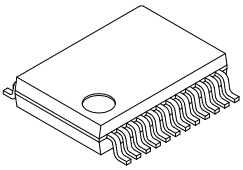
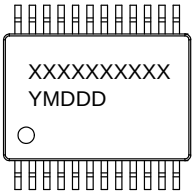


SSOP24 (225 mil)
CASE 565AR

MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

See detailed ordering and shipping information on page 36 of this data sheet.

Overview

The LC71F7001PVB is capacitance digital converter LSI designed for electrostatic capacitance touch sensors. A total of 14 capacitance sensors (7 pairs with 14 sensors in the differential input mode) can be connected to the input pin and, depending on how the sensors are combined, 14 or more switch functions can be provided. The LC71F7001PVB is also provided with up to 14 general-purpose output ports (GPO) that can be used as LED drive ports. The detected capacitance values are output as 16-bit digital data through the I^2C ™ serial interface. The detection sensitivity and capacitance offset value can be adjusted and set (calibrated) from an external device through the I^2C serial interface.

Features

- Detection System: 14 Electrostatic Capacitance Sensors Single/Differential Input, Differential Capacitance Value Output. By the Use of Multiple (Up to 8) LC71F7001PVB Capacitance Digital Converter LSI, They Can Increase the Number of the Input
- Input Capacitance Resolution: Less than 1 fF.
- Measurement Time (14 Single Inputs):
  0.84 ms (high-speed mode: f_{CDRV} = 200 kHz, OSR = 4) to 107.5 ms (high-resolution mode: f_{CDRV} = 200 kHz, OSR = 512)
  OSR: Oversampling Ratio
- External Components: Not Required
- On-chip Calibration: Function for Removing Environmental Factors
- Built-in EEPROM: For Storing Calibration Data, EEPROM Rewriting Times 10000 Cycles, EEPROM Data Retention Time 20 years
- Interface: I^2C Serial Interface Compatible
- Low Power Consumption: Typ 10 μA (during intermittent operation) to Typ 0.8 mA (during continuous operation).
- Supply Voltage: 2.6 V to 3.6 V

Typical Applications

- Consumer: Home Appliance, Digital Cameras
- Industrial: Remote Controllers
- Computing: Cell Phones, Portable Devices, Game Machines

Specifications

Table 1. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	AV_{DD}/DV_{DD}	−0.3 to +4.0	V	
Input Voltage	V_{IN1}	−0.3 to AV_{DD} + 0.3	V	C_{IN}0 to 13, TEST, C_{REF}
	V_{IN2}	−0.3 to DV_{DD} + 0.3		SCL, SDA
Output Voltage	V_{OUT1}	−0.3 to AV_{DD} + 0.3	V	GPO0 to 13, C_{DRV}, C_{DRV}X, C_{DRV}Y, C_{DRV}B, INT
	V_{OUT2}	−0.3 to DV_{DD} + 0.3	V	SDA
Power Dissipation	$P_{d\ max}$	200	mW	T_A = +85°C
Storage Temperature	T_{stg}	−55 to +125	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remarks
Operating Supply Voltage	AV_{DD}		2.6	2.8	3.6	V	
Operating Supply Voltage (for I/F)	DV_{DD}		1.65	−	AV_{DD}	V	
Operating Temperature	T_{opr}		−40	25	85	°C	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS

(V_{SS} = 0 V, AV_{DD} = DV_{DD} = 2.6 to 3.6 V, T_A = −40 to +85°C, Unless otherwise specified, the CDRV drive frequency and oversampling ratio setting are f_{CDRV} = 100 kHz and OSR = 512, respectively.)

Parameter	Symbol	Pin Name/Conditions	Min	Typ	Max	Unit	Remarks
Capacitance Detection Resolution	N				16	bit	
Output Noise RMS	N_{RMS}	Differential input, minimum gain setting			±1.0	LSB	(Notes 1, 3)
Input Offset Capacitance Adjustment Range	$Coff_{RANGE}$	C_{IN} (single input mode)			12.0	pF	(Notes 1, 3)
		C_{IN} (differential input mode)			±6.0		
Input Offset Capacitance Adjustment Resolution	$Coff_{RESO}$			7		bit	
C_{IN} Offset Drift	$C_{INDRIFT}$	Differential input, minimum gain setting			±2000	LSB	(Note 1)
C_{IN} Detection Sensitivity	$C_{INSENSE}$	Differential input, minimum gain setting	10		30	LSB/fF	(Note 2)
C_{IN} Pin Leak Current	I_{CIN}	C_{IN} = HighZ		±25	±500	nA	
C_{IN} Allowable Parasitic Input Capacitance	C_{INSUB}	Against V_{SS} (C_{IN})			30	pF	(Notes 1, 3)
	$C_{INCDRV}1$	Against C_{DRV} (C_{IN}) Differential input mode After static offset calibration is performed		4			
	$C_{INCDRV}2$	Against C_{DRV} (C_{IN}) Single input mode After static offset calibration is performed		8			
C_{DRV} Drive Frequency	f_{CDRV}	at 200 kHz	120		280	kHz	
C_{DRV} Pin Leak Current	I_{CDRV}	C_{DRV} = HighZ		±25	±500	nA	
GPO/C_{DRV}/C_{DRV}X/C_{DRV}Y/ C_{DRV}B/INT Output Voltage	V_{OH_GPO}	High output (I_{GPO} = 3 mA)	0.7 AV_{DD}			V	(Note 4)
	V_{OL_GPO}	Low output (I_{GPO} = −3 mA)			0.3 AV_{DD}		
I^2C Interface Pin Input Voltage	$V_{IH\_I^2C}$	SCL, SDA high input	0.8 DV_{DD}			V	
	$V_{IL\_I^2C}$	SCL, SDA low input			0.2 DV_{DD}		
SDA Output Voltage	$V_{OL\_I^2C}$	SDA low output (I_{SDA} = −3 mA)			0.4	V	
I^2C Interface Pin Leak Current	I_{I^2C}	SCL, SDA (SDA = HighZ)			±1	μA	
Current Consumption	$I_{DD}1$	Intermittent operation mode (4 inputs) Measurement interval = 256 ms set f_{CDRV} = 200 kHz set OSR = 8, moving average count = 8		10	30	μA	(Note 5)
	$I_{DD}2$	Continuous operation mode Measurement Interval = 0 ms set		0.8	1.2	mA	(Note 5)
	I_{STBY}	Standby mode			2.0	μA	(Note 5)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Design guarantee values (not tested before shipment).
2. Measurements conducted using the test mode in the LSI.
3. T_A = 25°C.
4. Maximum output of 3 mA for each port (GPO/C_{DRV}/C_{DRV}X/C_{DRV}Y/C_{DRV}B/INT), total output are 9 mA maximum.
5. AV_{DD} = DV_{DD} = 2.8 V, T_A = 25°C.

Table 4. I²C COMPATIBLE BUS INTERFACE TIMING CHARACTERISTICS

(V_{SS} = 0 V, AV_{DD} = DV_{DD} = 2.6 to 3.6 V, T_A = −40 to +85°C)

Parameter	Symbol	Pin Name/Conditions	Min	Typ	Max	Unit	Remarks
SCL Clock Frequency	f_{SCL}	SCL			400	kHz	
Start Condition Hold Time	$t_{HD;STA}$	SCL, SDA	0.6			μs	
SCL Clock Low Period	t_{LOW}	SCL	1.3			μs	
SCL Clock High Period	t_{HIGH}	SCL	0.6			μs	
Repeated Start Condition Set Up Time	$t_{SU;STA}$	SCL, SDA	0.6			μs	
Data Hold Time	$t_{HD;DAT}$	SCL, SDA	0		0.9	μs	
Data Setup Time	$t_{SU;DAT}$	SCL, SDA	100			ns	(Note 6)
SDA, SCL Rise Time	t_r	SCL, SDA			300	ns	(Note 6)
SDA, SCL Fall Time	t_f	SCL, SDA			300	ns	(Note 6)
Stop Condition Setup Time	$t_{SU;STO}$	SCL, SDA	0.6			μs	
Stop-to-Start Bus Release Time	t_{BUF}	SCL, SDA	1.3			μs	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Design guarantee values (not tested before shipment).

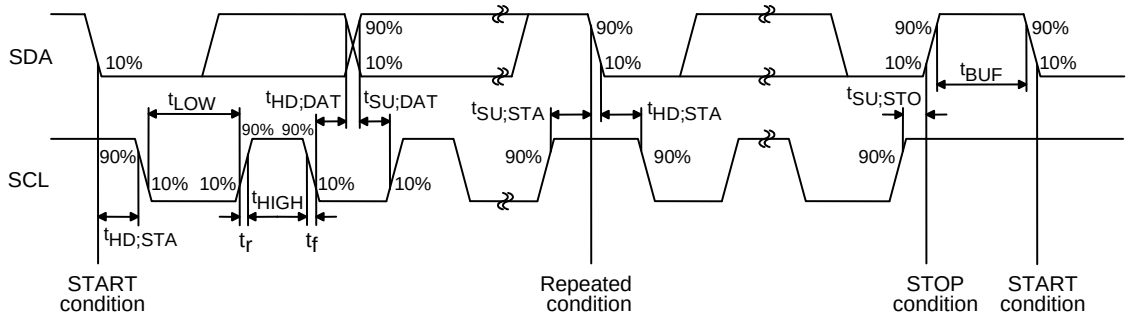


Figure 1. I²C Bus Timing Definition (FAST-MODE: 400 kHz)

7. The SCL and SDA lines are easily subject to noise. They must be connected with lines that are as short as possible.

Block Diagram

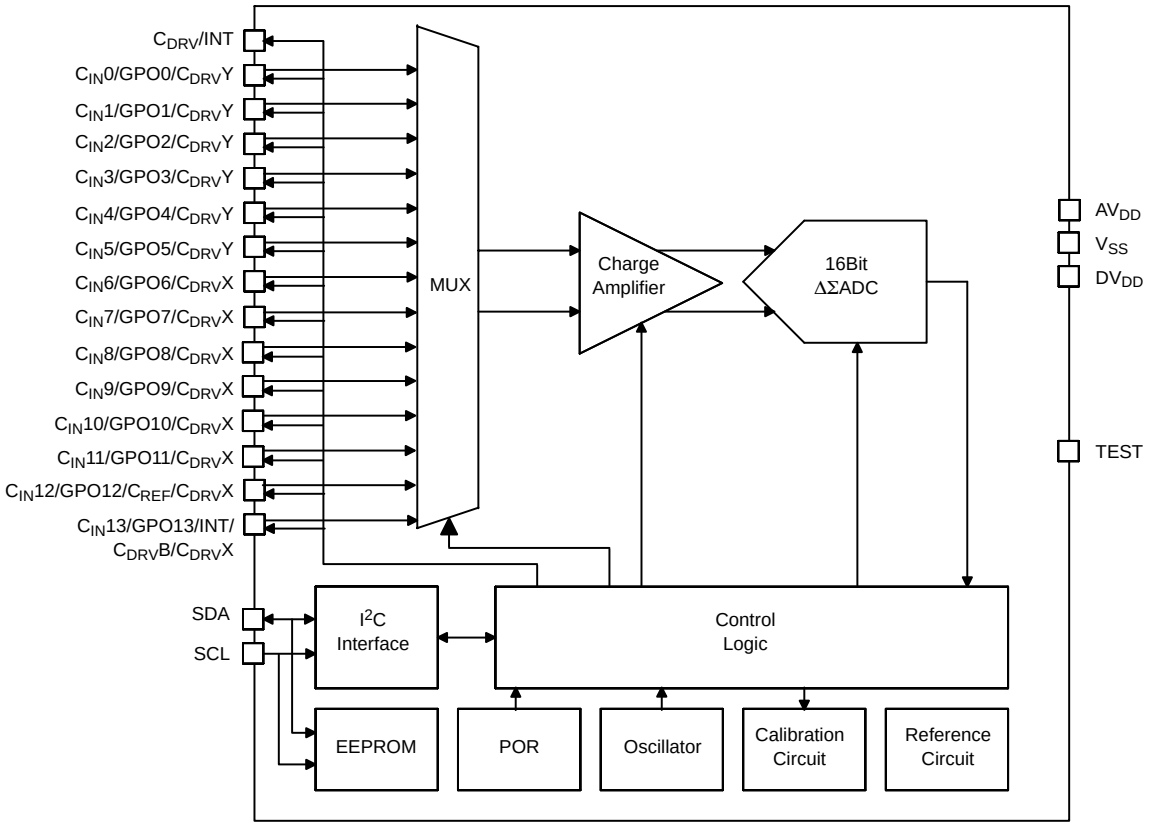


Figure 2. Simplified Block Diagram

The LC71F7001PVB is capacitance digital converter LSI capable of detecting changes in capacitance in the order of femtofarads (fF). It consists of an I^2C serial interface that enables serial communication with external devices, a reference circuit that generates the reference current and voltage, a power-on reset circuit that resets the system when the power is turned on, an oscillation circuit that generates the system clock, a calibration circuit for adjusting the detection sensitivity levels and capacitance offset amounts, an EEPROM that stores the calibration data of the detection sensitivity levels and capacitance offset amounts which have been set, GPO ports with a general-purpose digital output capability, a multiplexer that selects the input channels, a charge amplifier that detects the changes in the capacitance and outputs analog amplitude values, a 16-bit ΔΣA/D converter circuit that converts the analog amplitude values into digital data, and a control logic that controls the entire chip.

Pin Assignment

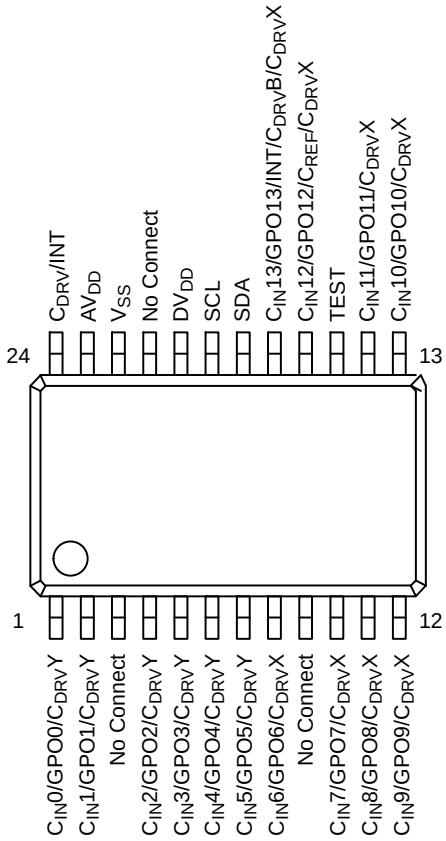


Figure 3. Pin Assignment (Top View)

Table 5. PIN ASSIGNMENT

Pin No.	Pin Name
1	C_{IN}0/GPO0/C_{DRV}Y
2	C_{IN}1/GPO1/C_{DRV}Y
3	No Connect
4	C_{IN}2/GPO2/C_{DRV}Y
5	C_{IN}3/GPO3/C_{DRV}Y
6	C_{IN}4/GPO4/C_{DRV}Y
7	C_{IN}5/GPO5/C_{DRV}Y
8	C_{IN}6/GPO6/C_{DRV}X
9	No Connect
10	C_{IN}7/GPO7/C_{DRV}X
11	C_{IN}8/GPO8/C_{DRV}X
12	C_{IN}9/GPO9/C_{DRV}X
13	C_{IN}10/GPO10/C_{DRV}X
14	C_{IN}11/GPO11/C_{DRV}X
15	TEST (Note 8)
16	C_{IN}12/GPO12/C_{REF}/C_{DRV}X
17	C_{IN}13/GPO13/INT/C_{DRV}B/C_{DRV}X
18	SDA
19	SCL
20	DV_{DD}
21	No Connect
22	V_{SS}
23	AV_{DD}
24	C_{DRV}/INT

8. Must be connected to V_{SS} when mounted.

Table 6. PIN FUNCTION

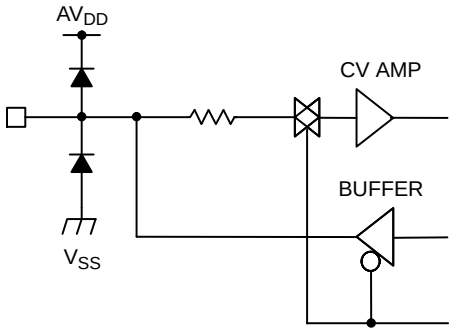
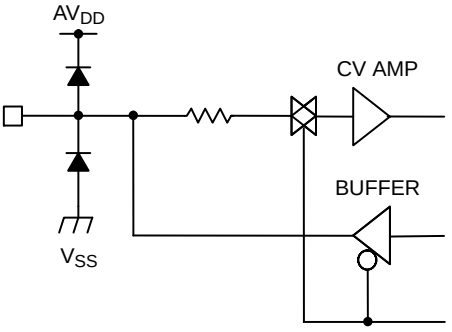
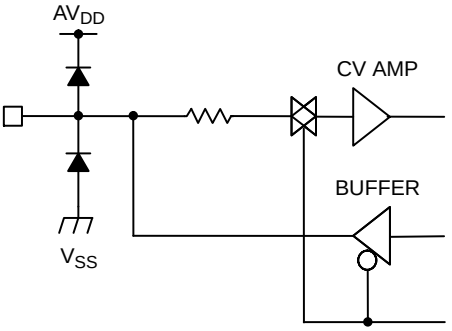
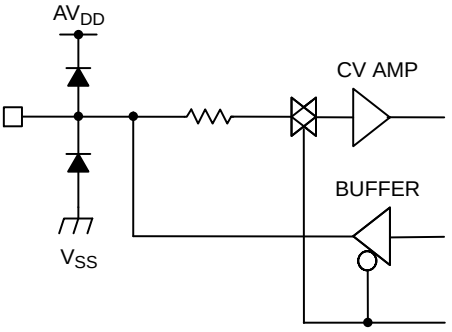
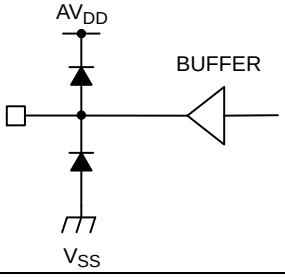
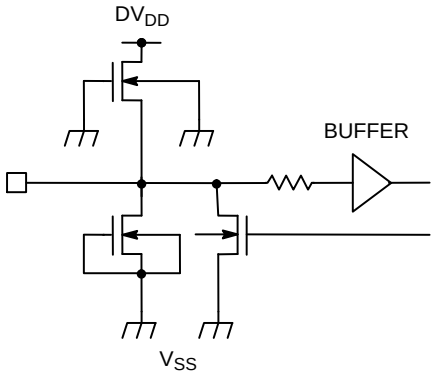
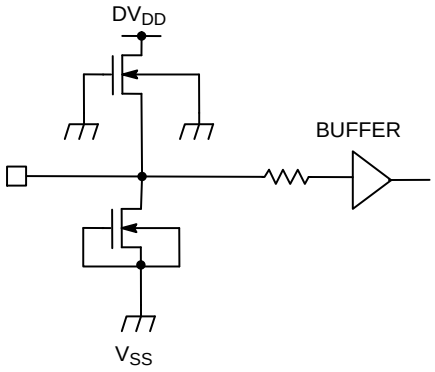
Pin Name	I/O	Pin Functions	Pin Type
$C_{IN}0$/GPO0/$C_{DRV}Y$ $C_{IN}1$/GPO1/$C_{DRV}Y$ $C_{IN}2$/GPO2/$C_{DRV}Y$ $C_{IN}3$/GPO3/$C_{DRV}Y$ $C_{IN}4$/GPO4/$C_{DRV}Y$ $C_{IN}5$/GPO5/$C_{DRV}Y$	I/O	Capacitance sensor input/ General-purpose output/ Y-axis capacitance drive output	
$C_{IN}6$/GPO6/$C_{DRV}X$ $C_{IN}7$/GPO7/$C_{DRV}X$ $C_{IN}8$/GPO8/$C_{DRV}X$ $C_{IN}9$/GPO9/$C_{DRV}X$ $C_{IN}10$/GPO10/$C_{DRV}X$ $C_{IN}11$/GPO11/$C_{DRV}X$	I/O	Capacitance sensor input/ General-purpose output/ X-axis capacitance drive output	
$C_{IN}12$/GPO12/ C_{REF}/$C_{DRV}X$	I/O	Capacitance sensor input/ General-purpose output/ Reference capacitance connection/ X-axis capacitance drive output	
$C_{IN}13$/GPO13/INT/ $C_{DRV}B$/$C_{DRV}X$	I/O	Capacitance sensor input/ General-purpose output/ Interrupt output/ C_{DRV} inverted output/ X-axis capacitance drive output	
C_{DRV}/INT	O	Capacitance drive common output/ Interrupt output	

Table 6. PIN FUNCTION (continued)

Pin Name	I/O	Pin Functions	Pin Type
SDA	I/O	I^2C serial data input/output	
SCL	I	I^2C serial clock input	
TEST	I	Shipment time TEST input It must always be connected to V_{SS}	
V_{SS}	−	Ground	
DV_{DD}	−	I^2C serial interface power supply (1.65 V to AV_{DD})	
AV_{DD}	−	Power supply (2.6 V to 3.6 V)	

I²C-compatible Bus Interface Formats

- Write format (data can be written into sequentially incremented addresses)

Figure 4.

- Read format (data can be read from sequentially incremented addresses)

Figure 5.

9. Controller slave address: bxxxxxxx (7-bit data written into 0x00 EEPROM address. Any address can be set after shipment) EEPROM slave address: b1010xxx (lower-order 3 bits are set to one of the 8 address types prior to shipment. Refer to Table 7)
10. EEPROM rewrite time: 10 ms after stop condition (ACK signal is not output during rewrite operation)
11. When data is written sequentially into the EEPROM, only the lower-order 4 bits of the register addresses are incremented.
    Example: When the 4-byte sequential writes are started from address 0x0D, the data is written into the address in the order of 0x0D => 0x0E => 0x0F => 0x00.

Table 7. EEPROM SLAVE ADDRESS SETTINGS (Product Name Differs Depending on Address Type)

Address Type	Product Name	EEPROM Slave Address Lower-order 3 bits
A0	LC71F7001PVBS0−TLM−H	(0, 0, 0)
A1	−	(0, 0, 1)
A2	−	(0, 1, 0)
A3	−	(0, 1, 1)
A4	−	(1, 0, 0)
A5	−	(1, 0, 1)
A6	−	(1, 1, 0)
A7	−	(1, 1, 1)

General Registers

Table 8. CONTROL REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x00	Name	SoftRst	FFR	INTHIZ	IVAL3	IVAL2	IVAL1	IVAL0	RUN
	Reset	0	1	0	0	0	0	0	0
	W/R	W	RW	W	RW	RW	RW	RW	RW

SoftRst: Software reset
0: Not used
1: Reset (Disabled when the value of 0x24 First Fixed Register is any value other than 0x00)

FFR: Initialization register
0: Normal operation mode
1: Reset value

INTHIZ: Interrupt output high-impedance select
0: Normal operation mode
1: Interrupt output high-impedance

IVAL0−IVAL3: MEASUREMENT INTERVALS, f_{CDRV} = 200 kHz SET

IVAL3	IVAL2	IVAL1	IVAL0	Measurement Interval
0	0	0	0	0 ms
0	0	0	1	1 ms
0	0	1	0	2 ms
0	0	1	1	4 ms
0	1	0	0	8 ms
0	1	0	1	16 ms
0	1	1	0	32 ms
0	1	1	1	64 ms
1	0	0	0	128 ms
1	0	0	1	256 ms
1	0	1	0	512 ms
1	0	1	1	1024 ms
1	1	0	0	2048 ms

RUN: Measurement start
0: Standby (sensor-connection pin is high-impedance state)
1: Measurement start (if OFFCAL = 1, automatic offset calibration is started)

12. When RUN is set to 1, do not write a register value other than RUN = 0 (standby).

Table 9. CONFIGURATION REGISTER 1

	Bit	7	6	5	4	3	2	1	0
Address 0x01	Name	INTZ	SCF3	SCF2	SCF1	SCF0	OSR2	OSR1	OSR0
	Reset	0	0	0	0	0	0	0	0
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

INTZ: Interrupt output type select
0: CMOS output
1: N-channel open drain

SCF0−SCF3: SAMPLING CLOCK FREQUENCY (C_{DRV} DRIVE FREQUENCY)

SCF3	SCF2	SCF1	SCF0	Sampling Clock Frequency
0	0	0	0	20.8 kHz
0	0	0	1	31.3 kHz
0	0	1	0	50.0 kHz
0	0	1	1	83.3 kHz
0	1	0	0	100.0 kHz
0	1	0	1	125.0 kHz
0	1	1	0	166.7 kHz
0	1	1	1	200.0 kHz
1	0	0	0	250.0 kHz
1	0	0	1	333.3 kHz
1	0	1	0	500.0 kHz

13. The optimum frequency varies depending on the sensor load.

OSR0−OSR2: OVERSAMPLING RATIO

OSR2	OSR1	OSR0	OSR
0	0	0	512 times
0	0	1	256 times
0	1	0	128 times
0	1	1	64 times
1	0	0	32 times
1	0	1	16 times
1	1	0	8 times
1	1	1	4 times

Table 10. CONFIGURATION REGISTER 2

	Bit	7	6	5	4	3	2	1	0
Address 0x02	Name	OFFCAL	−	TPDRV	OFINTEN	INTPOL	INTSEL	AVG1	AVG0
	Reset	0	−	0	0	0	0	0	0
	W/R	RW	−	RW	RW	RW	RW	RW	RW

OFFCAL: Static offset calibration
0: Normal operation mode
1: Static offset calibration mode

14. It performs offset calibration for the parasitic capacitance of the sensor pattern using the on-chip capacitance of the LSI. The calibration data is automatically stored in the C_{IN} Static Offset Registers.
15. When static offset calibration is performed, dynamic offset calibration must be disabled without fail. (Using both static offset calibration and dynamic offset calibration at the same time is prohibited.)

TPDRV: Touch panel drive function enable/disable
0: Disables the touch panel drive function
1: Enables the touch panel drive function. ($C_{IN}0$ to $C_{IN}5$ are capacitance drive outputs during X-axis sensing; $C_{IN}6$ to $C_{IN}13$ are capacitance drive outputs during Y-axis sensing.)

OFINTEN: Dynamic offset overflow interrupt enable/disable
0: Disables dynamic offset interrupts
1: Enables dynamic offset interrupts

INTPOL: Interrupt polarity
0: High active
1: Low active

INSEL: INTERRUPT MODE SELECT

INTSEL	Interrupt Occurrence Conditions
0	When the first valid data is established after measurement is started. When offset calibration is completed. When a dynamic offset calibration overflow occurs.
1	When output data whose value exceeds the one specified in the Threshold Register occurs successively the number of times specified in the INT Count Register (operations detected). When a dynamic offset calibration overflow occurs.

AVG0−AVG1: MOVING AVERAGING COUNT

AVG1	AVG0	Moving Averaging Count
0	0	1 time (no averaging)
0	1	2 times
1	0	4 times
1	1	8 times

16. Assume that the moving average count specified in AVG0−AVG1 is N (= 1, 2, 4, 8).
When the number of measurement times is under N, the following averaging data is output.
(Data_N + Data_ (N−1) + ~ + Data_1 + Data_1 + Data_1) / N
When the number of measurement times is N or more, the following averaging data is output.
(Data_N + Data_ (N−1) + ~ + Data_3 + Data_2 + Data_1) / N

Table 11. GPO CONTROL REGISTER 1

	Bit	7	6	5	4	3	2	1	0
Address 0x03	Name	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0
	Reset	0	0	0	0	0	0	0	0
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

GPO0−GPO7: GPO output control
0: Low level output
1: High level output

Table 12. GPO CONTROL REGISTER 2

	Bit	7	6	5	4	3	2	1	0
Address 0x04	Name	−	−	GPO13	GPO12	GPO11	GPO10	GPO9	GPO8
	Reset	−	−	0	0	0	0	0	0
	W/R	−	−	RW	RW	RW	RW	RW	RW

GPO8−GPO13: GPO output control
0: Low level output
1: High level output

Table 13. INT STATUS REGISTER 1

	Bit	7	6	5	4	3	2	1	0
Address 0x05	Name	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
	W/R	R	R	R	R	R	R	R	R

INT0−INT7: $C_{IN}0$ to $C_{IN}7$ operation detection interrupt status flag
0: No interrupt has occurred
1: An interrupt has occurred

Table 14. INT STATUS REGISTER 2

	Bit	7	6	5	4	3	2	1	0
Address 0x06	Name	INTOFF	−	INT13	INT12	INT11	INT10	INT9	INT8
	W/R	R	−	R	R	R	R	R	R

INTOFF: Dynamic offset overflow
0: No interrupt has occurred
1: The dynamic offset has exceeded the expected range
(Dynamic Offset Threshold register > C_{IN} Dynamic Offset Register)

INT8−INT13: $C_{IN}8$ to $C_{IN}13$ operation detection interrupt status flag
0: No interrupt has occurred
1: An interrupt has occurred

17. Reading the INT Status Register 2 in byte units clears the interrupt outputs and the interrupt status flags.
When the INT Status Register 2 is read in sequential order, the interrupt outputs and interrupt status flags are not cleared.

Table 15. DATA00 REGISTER TO DATA27 REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x07 to 0x22	Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
	W/R	R	R	R	R	R	R	R	R

These registers store the computation results for Data Register = ΣΔA/D converter data + C_{IN} Static Offset Registers (0x49 to 0x52) + C_{IN} Dynamic Offset Registers (0x53 to 0x66) in two's complement number.

Example:
0x7FFF = +32767
0x0000 = ±0
0x8000 = −32768

Data00 Register	$C_{IN}0$ measurement data (higher-order 8 bits)
Data01 Register	$C_{IN}1$ measurement data (higher-order 8 bits) $C_{IN}0$ data is valid in the differential input mode
Data02 Register	$C_{IN}2$ measurement data (higher-order 8 bits)
Data03 Register	$C_{IN}3$ measurement data (higher-order 8 bits) $C_{IN}2$ data is valid in the differential input mode
Data04 Register	$C_{IN}4$ measurement data (higher-order 8 bits)
Data05 Register	$C_{IN}5$ measurement data (higher-order 8 bits) $C_{IN}4$ data is valid in the differential input mode
Data06 Register	$C_{IN}6$ measurement data (higher-order 8 bits)
Data07 Register	$C_{IN}7$ measurement data (higher-order 8 bits) $C_{IN}6$ data is valid in the differential input mode
Data08 Register	$C_{IN}8$ measurement data (higher-order 8 bits)
Data09 Register	$C_{IN}9$ measurement data (higher-order 8 bits) $C_{IN}8$ data is valid in the differential input mode
Data10 Register	$C_{IN}10$ measurement data (higher-order 8 bits)
Data11 Register	$C_{IN}11$ measurement data (higher-order 8 bits) $C_{IN}10$ data is valid in the differential input mode
Data12 Register	$C_{IN}12$ measurement data (higher-order 8 bits)

Data13 Register	C_{IN}13 measurement data (higher-order 8 bits) C_{IN}12 data is valid in the differential input mode
Data14 Register	C_{IN}0 measurement data (lower-order 8 bits)
Data15 Register	C_{IN}1 measurement data (lower-order 8 bits) C_{IN}0 data is valid in the differential input mode
Data16 Register	C_{IN}2 measurement data (lower-order 8 bits)
Data17 Register	C_{IN}3 measurement data (lower-order 8 bits) C_{IN}2 data is valid in the differential input mode
Data18 Register	C_{IN}4 measurement data (lower-order 8 bits)
Data19 Register	C_{IN}5 measurement data (lower-order 8 bits) C_{IN}4 data is valid in the differential input mode
Data20 Register	C_{IN}6 measurement data (lower-order 8 bits)
Data21 Register	C_{IN}7 measurement data (lower-order 8 bits) C_{IN}6 data is valid in the differential input mode
Data22 Register	C_{IN}8 measurement data (lower-order 8 bits)
Data23 Register	C_{IN}9 measurement data (lower-order 8 bits) C_{IN}8 data is valid in the differential input mode
Data24 Register	C_{IN}10 measurement data (lower-order 8 bits)
Data25 Register	C_{IN}11 measurement data (lower-order 8 bits) C_{IN}10 data is valid in the differential input mode
Data26 Register	C_{IN}12 measurement data (lower-order 8 bits)
Data27 Register	C_{IN}13 measurement data (lower-order 8 bits) C_{IN}12 data is valid in the differential input mode

Table 16. EEPROM WRITE PROTECT/INITIALIZE REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x23	Name	−	−	−	−	−	−	−	EEPWP
	Reset	−	−	−	−	−	−	−	0
	W/R	−	−	−	−	−	−	−	RW

Internal EEPROM write protection and initialization

EEPWP:
0: Enables write operation (default)
1: Disables write operation

18. Be sure to perform writes to this register in the order of 0x01 → 0x00 → 0x01 during power-on-time initialization.

Table 17. FIRST FIXED REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x24	Name	FFR7	FFR6	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
	Reset	0	0	0	0	0	0	0	0
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

Initialization register

FFR0−FFR7:
0: Reset value (fixed)
1: Write protected

19. Be sure to write a 0x00 into this register when using the LSI. The LSI will not run normally with any value other than 0x00.

Parameter Registers

Table 18. CONTROLLER I²C SLAVE ADDRESS REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x25	Name	SLAVE6	SLAVE5	SLAVE4	SLAVE3	SLAVE2	SLAVE1	SLAVE0	−
	W/R	R	R	R	R	R	R	R	−

SLAVE0−SLAVE6: Controller side I²C Slave Address (7 bits not including the R/W bit). This takes effect by turning the LSI off and back on again after writing this value into the EEPROM address 0x00

Table 19. C_{IN}0−C_{IN}1: CONFIGURATION REGISTER 1

	Bit	7	6	5	4	3	2	1	0
Address 0x26	Name	−	Cref1EN	Cref0EN	C_{IN}1EN	C_{IN}0EN	C_{IN}1POL	C_{IN}0POL	C_{IN}01diff
	W/R	−	RW	RW	RW	RW	RW	RW	RW

Cref0EN−Cref1EN: C_{IN}0, C_{IN}1 external reference capacitance connection enable/disable
0: Connects no reference capacitance in the single input mode
1: Connects the reference capacitance in the single input mode

C_{IN}0EN−C_{IN}1EN: C_{IN}0, C_{IN}1 capacitance (touch) detection enable/disable
0: Disables capacitance (touch) detection (the sensor connection pin is in high-impedance state)
1: Enables capacitance (touch) detection

20. In the differential input mode, C_{IN}0EN and C_{IN}1EN must be set to 0 or 1 at the same time (setting them to 01 and 10 is prohibited).

C_{IN}0POL−C_{IN}1POL: C_{IN}0, C_{IN}1 charge amplifier input polarity (valid only when single input has been selected)
0: Positive input
1: Negative input

C_{IN}01diff: C_{IN}0, C_{IN}1 single input/differential input select
0: Single input
1: Differential input (C_{IN}0 is connected to the positive input of the charge amplifier, and C_{IN}1 is connected to the negative input)

Table 20. C_{IN}0−C_{IN}1: CONFIGURATION REGISTER 2

	Bit	7	6	5	4	3	2	1	0
Address 0x27	Name	OFFCALD1	OFFCALD0	GPO1SEL1	GPO1SEL0	GPO0SEL1	GPO0SEL0	INT1EN	INT0EN
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

OFFCALD0−OFFCALD1: C_{IN}0, C_{IN}1 dynamic offset calibration. Any offset caused by changes in temperature and other factors is compensated using dynamic computation.
0: Normal operation mode
1: Dynamic offset calibration mode

21. In the differential input mode, OFFCALD0 and OFFCALD1 must be set to 0 or 1 at the same time (setting them to 01 and 10 is prohibited).

GPO0(1)SEL0−GPO0(1)SEL1: C_{IN}0, C_{IN}1 PIN GPO MODE SELECT

GPO0(1)SEL1	GPO0(1)SEL0	Mode
0	0	Normal capacitance detection mode
0	1	Standard GPO mode The values set by the GPO Control Register 1, 2 are output at all times. Capacitance detection is not performed.
1	0	LED drive mode The values set by the GPO Control Register 1, 2 are output during the measurement interval time after capacitance is detected.

22. In the differential input mode, the standard GPO mode cannot be used.

INT0EN−INT1EN: C_{IN}0, C_{IN}1 operation detection interrupt enable/disable
0: Disables operation detection interrupts.
1: Enables operation detection interrupts.

23. In the differential input mode, INT0EN and INT1EN must be set to 0 or 1 at the same time (setting them to 01 and 10 is prohibited).

C_{IN}2−C_{IN}3 Configuration Register 1 (Address 0x28) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 1.
C_{IN}2−C_{IN}3 Configuration Register 2 (Address 0x29) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 2.
C_{IN}4−C_{IN}5 Configuration Register 1 (Address 0x2A) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 1.
C_{IN}4−C_{IN}5 Configuration Register 2 (Address 0x2B) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 2.
C_{IN}6−C_{IN}7 Configuration Register 1 (Address 0x2C) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 1.
C_{IN}6−C_{IN}7 Configuration Register 2 (Address 0x2D) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 2.
C_{IN}8−C_{IN}9 Configuration Register 1 (Address 0x2E) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 1.
C_{IN}8−C_{IN}9 Configuration Register 2 (Address 0x2F) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 2.
C_{IN}10−C_{IN}11 Configuration Register 1 (Address 0x30) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 1.
C_{IN}10−C_{IN}11 Configuration Register 2 (Address 0x31) => The contents are the same as those in the C_{IN}0−C_{IN}1 Configuration Register 2.

Table 21. C_{IN}12−C_{IN}13: CONFIGURATION REGISTER 1

	Bit	7	6	5	4	3	2	1	0
Address 0x32	Name	C_{DRV}SEL	FFR	C_{DRV}BEN	C_{IN}13EN	C_{IN}12EN	C_{IN}13POL	C_{IN}12POL	C_{IN}1213diff
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

C_{DRV}SEL: C_{DRV}/INT pin function select
0: Normal capacitance drive pin
1: Interrupt output pin

FFR: Initialization register
0: Normal operation mode
1: Prohibited

C_{DRV}BEN: C_{IN}13 C_{DRV}B (inverted signal of C_{DRV}) capacitance drive enable/disable
0: Does not set C_{IN}13 as the C_{DRV}B capacitance drive pin
1: Set C_{IN}13 as the C_{DRV}B capacitance drive pin

C_{IN}12EN−C_{IN}13EN:
C_{IN}12 capacitance (touch) detection enable/external reference capacitance connection pin
C_{IN}13 capacitance (touch) detection enable and C_{DRV}B output/interrupt output select
0: Does not perform capacitance (touch) detection. (Sensor connection pin C_{IN}12 => external reference capacitance connection pin; sensor connection pin C_{IN}13 => C_{DRV}B output/interrupt output)
1: Performs capacitance (touch) detection

24. In the differential input mode, C_{IN}12EN and C_{IN}13EN must be set to 0 or 1 at the same time (setting them to 01 and 10 is prohibited).

C_{IN}12POL−C_{IN}13POL: C_{IN}12, C_{IN}13 charge amplifier input polarity (valid only when single input is selected)
0: Positive input
1: Negative input

C_{IN}1213diff: C_{IN}12, C_{IN}13 single/differential input select
0: Single input
1: Differential input (C_{IN}12 is connected to the positive input of the charge amplifier, and C_{IN}13 is connected to the negative input).

C_{DRV}BEN	C_{IN}13EN	C_{IN}12EN	C_{IN}1213Diff	C_{IN}13 Pin	C_{IN}12 Pin
1	0	0	0	C_{DRV}B output	Connected to reference capacitance
0	0	0	0	Interrupt output	Disabled
0	0	1	0	Interrupt output	Capacitance sensor input
0	1	0	0	Capacitance sensor input	Disabled
0	1	1	0	Capacitance sensor input	Capacitance sensor input
0	0	0	1	Disabled	Disabled
0	1	1	1	Capacitance sensor input	Capacitance sensor input

25. Any value combinations other than those listed above are not allowed.

Table 22. C_{IN}12−C_{IN}13: CONFIGURATION REGISTER 2

	Bit	7	6	5	4	3	2	1	0
Address 0x33	Name	OFFCALD13	OFFCALD12	GPO13SEL1	GPO13SEL0	GPO12SEL1	GPO12SEL0	INT13EN	INT12EN
	W/R	W	W	W	W	W	W	RW	RW

OFFCALD12−OFFCALD13: C_{IN}12, C_{IN}13 dynamic offset calibration. Any offset caused by changes in temperature and other factors is compensated by dynamic computation.
0: Normal operation mode
1: Dynamic offset calibration mode

26. In the differential input mode, OFFCALD12 and OFFCALD13 must be set to 0 or 1 at the same time (setting them to 01 and 10 is prohibited).

GPO12(13)SEL0−GPO12(13)SEL1: C_{IN}12, C_{IN}13 PIN GPO MODE SELECT

GPO12(13)SEL1	GPO12(13)SEL0	Mode
0	0	Normal capacitance detection mode
0	1	Standard GPO mode The values set by the GPO Control Register 1, 2 are output at all times. Capacitance detection is not performed.
1	0	LED drive mode The values set by the GPO Control Register 1, 2 are output during the measurement interval time after capacitance is detected.

27. n the differential input mode, the standard GPO mode cannot be used.

INT12EN−INT13EN: C_{IN}12, C_{IN}13 operation detection interrupt enable/disable
0: Disables operation detection interrupts
1: Enables operation detection interrupts

28. In the differential input mode, INT12EN and INT13EN must be set to 0 or 1 at the same time (setting them to 01 and 10 is prohibited).

Table 23. DATA CENTER REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x34	Name	−	−	−	−	−	−	CENTER1	CENTER0
	W/R	−	−	−	−	−	−	RW	RW

Reference values used when no touch operations are performed. Offset calibration is performed in such a way that the values specified in the Data Center Register are set.

CENTER1	CENTER0	Offset Calibration Center Value
0	0	−24576
0	1	−16384
1	0	−8192
1	1	±0

29. In the differential input mode, the offset calibration center value is fixed at ±0.

Table 24. SINGLE INT THRESHOLD REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x35	Name	−	SMTH6	SMTH5	SMTH4	SMTH3	SMTH2	SMTH1	SMTH0
	W/R	−	RW	RW	RW	RW	RW	RW	RW

This register determines the threshold value beyond which interrupt occurs in the single input mode.

The operation detection interrupt is generated when the condition in which the measurement data is greater than the threshold value in the single input mode has occurred continuously for the number of times specified in the INT Count Register. The interrupt generation flag in the INT Status Register 1, 2 is then set.

Single INT Threshold Register	Threshold Value
0x00	−32768
0x01	−32256
0x02	−31744
0x7D	+31232
0x7E	+31744
0x7F	+32256

Table 25. DIFFERENTIAL INT THRESHOLD REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x36	Name	−	−	DMPTH5	DMPTH4	DMPTH3	DMPTH2	DMPTH1	DMPTH0
	W/R	−	−	RW	RW	RW	RW	RW	RW

This register determines the threshold value beyond which positive side interrupt occurs in the differential input mode.

The operation detection interrupt is generated when the condition in which the measurement data exceeds the threshold value range in the differential input mode has occurred continuously for the number of times specified in the INT Count Register. The interrupt generation flag in the INT Status Register 1, 2 is then set.

Differential INT Threshold Register	Threshold Value
0x00	±0
0x01	−512 to +511
0x02	−1024 to +1023
0x3D	−31232 to +31231
0x3E	−31744 to +31743
0x3F	−32256 to +32255

Table 26. INT COUNT REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x37	Name	−	−	−	−	INTCNT3	INTCNT2	INTCNT1	INTCNT0
	W/R	−	−	−	−	RW	RW	RW	RW

Interrupt count setting:
An interrupt is generated when the condition in which the measured value that exceeds the Threshold Register range occurs continuously for the number of times specified in the INT Count Register.
0x00 => 1 time 0x0F => 16 times

Table 27. $C_{IN}0$ GAIN REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x38	Name	Gain0_B3	Gain0_B2	Gain0_B1	Gain0_B0	Gain0_A3	Gain0_A2	Gain0_A1	Gain0_A0
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

Gain0_A0−Gain0_A3: Gain of the first stage charge amplifier (0000 => minimum gain, 1111 => maximum gain)
Gain0_B0−Gain0_B3: Gain of the subsequent stage charge amplifier (0000 => minimum gain, 1111 => maximum gain)

$C_{IN}0$ (1−13) First stage charge amplifier gain settings
Calculation formula: $\Delta V = \Delta C/Cf \times C_{DRV}$
Where:
ΔV: Output voltage of the first stage amplifier
ΔC: Change in input capacitance
C_{DRV}: Output voltage of C_{DRV}

Gain A3	Gain A2	Gain A1	Gain A0	Cf (fF)
0	0	0	0	1600 (minimum gain setting)
0	0	0	1	1500
0	0	1	0	1400
0	0	1	1	1300
0	1	0	0	1200
0	1	0	1	1100
0	1	1	0	1000
0	1	1	1	900
1	0	0	0	800
1	0	0	1	700
1	0	1	0	600
1	0	1	1	500
1	1	0	0	400
1	1	0	1	300
1	1	1	0	200
1	1	1	1	100 (maximum gain setting)

$C_{IN}0$ (1−13) Subsequent stage amplifier gain settings

Gain B3	Gain B2	Gain B1	Gain B0	Gain (Times)
0	0	0	0	1 (minimum gain setting)
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16 (maximum gain setting)

$C_{IN}1$ Gain Register (Address 0x39) => The contents are the same as those in the $C_{IN}0$ Gain Register.
The value of $C_{IN}0$ Gain Register is valid in the differential input mode.

$C_{IN}2$ Gain Register (Address 0x3A) => The contents are the same as those in the $C_{IN}0$ Gain Register.
$C_{IN}3$ Gain Register (Address 0x3B) => The contents are the same as those in the $C_{IN}0$ Gain Register.
The value of $C_{IN}2$ Gain Register is valid in the differential input mode.

$C_{IN}4$ Gain Register (Address 0x3C) => The contents are the same as those in the $C_{IN}0$ Gain Register.
$C_{IN}5$ Gain Register (Address 0x3D) => The contents are the same as those in the $C_{IN}0$ Gain Register.
The value of $C_{IN}4$ Gain Register is valid in the differential input mode.

$C_{IN}6$ Gain Register (Address 0x3E) => The contents are the same as those in the $C_{IN}0$ Gain Register.
$C_{IN}7$ Gain Register (Address 0x3F) => The contents are the same as those in the $C_{IN}0$ Gain Register.
The value of $C_{IN}6$ Gain Register is valid in the differential input mode.

$C_{IN}8$ Gain Register (Address 0x40) => The contents are the same as those in the $C_{IN}0$ Gain Register.
$C_{IN}9$ Gain Register (Address 0x41) => The contents are the same as those in the $C_{IN}0$ Gain Register.
The value of $C_{IN}8$ Gain Register is valid in the differential input mode.

$C_{IN}10$ Gain Register (Address 0x42) => The contents are the same as those in the $C_{IN}0$ Gain Register.
$C_{IN}11$ Gain Register (Address 0x43) => The contents are the same as those in the $C_{IN}0$ Gain Register.
The value of $C_{IN}10$ Gain Register is valid in the differential input mode.

$C_{IN}12$ Gain Register (Address 0x44) => The contents are the same as those in the $C_{IN}0$ Gain Register.
$C_{IN}13$ Gain Register (Address 0x45) => The contents are the same as those in the $C_{IN}0$ Gain Register.
The value of $C_{IN}12$ Gain Register is valid in the differential input mode.

Table 28. $C_{IN}0$ CDAC OFFSET POS REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x46	Name	−	C0ADOP6	C0ADOP5	C0ADOP4	C0ADOP3	C0ADOP2	C0ADOP1	C0ADOP0
	W/R	−	RW	RW	RW	RW	RW	RW	RW

This register is used to perform offset adjustment for the parasitic capacitance of the sensor pattern using the on-chip capacitance DA converter. The contents of this register are automatically updated by the static offset calibration command.
Offset adjustment range: 62.5 fF/LSB

Table 29. $C_{IN}0$ CDAC OFFSET NEG REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x47	Name	−	C0ADON6	C0ADON5	C0ADON4	C0ADON3	C0ADON2	C0ADON1	C0ADON0
	W/R	−	RW	RW	RW	RW	RW	RW	RW

This register is used to perform offset adjustment for the parasitic capacitance of the sensor pattern using the on-chip capacitance DA converter. The contents of the register are automatically updated by the static offset calibration command.
Offset adjustment range: 62.5 fF/LSB

$C_{IN}1$ CDAC Offset Pos Register (Address 0x48) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Pos Register.
$C_{IN}1$ CDAC Offset Neg Register (Address 0x49) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Neg Register.
$C_{IN}2$ CDAC Offset Pos Register (Address 0x4A) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Pos Register.
$C_{IN}2$ CDAC Offset Neg Register (Address 0x4B) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Neg Register.
$C_{IN}3$ CDAC Offset Pos Register (Address 0x4C) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Pos Register.
$C_{IN}3$ CDAC Offset Neg Register (Address 0x4D) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Neg Register.
$C_{IN}4$ CDAC Offset Pos Register (Address 0x4E) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Pos Register.
$C_{IN}4$ CDAC Offset Neg Register (Address 0x4F) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Neg Register.
$C_{IN}5$ CDAC Offset Pos Register (Address 0x50) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Pos Register.
$C_{IN}5$ CDAC Offset Neg Register (Address 0x51) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Neg Register.
$C_{IN}6$ CDAC Offset Pos Register (Address 0x52) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Pos Register.
$C_{IN}6$ CDAC Offset Neg Register (Address 0x53) => The contents are the same as those in the $C_{IN}0$ CDAC Offset Neg Register.

C_{IN}7 CDAC Offset Pos Register (Address 0x54) => The contents are the same as those in the C_{IN}0 CDAC Offset Pos Register.

C_{IN}7 CDAC Offset Neg Register (Address 0x55) => The contents are the same as those in the C_{IN}0 CDAC Offset Neg Register.

C_{IN}8 CDAC Offset Pos Register (Address 0x56) => The contents are the same as those in the C_{IN}0 CDAC Offset Pos Register.

C_{IN}8 CDAC Offset Neg Register (Address 0x57) => The contents are the same as those in the C_{IN}0 CDAC Offset Neg Register.

C_{IN}9 CDAC Offset Pos Register (Address 0x58) => The contents are the same as those in the C_{IN}0 CDAC Offset Pos Register.

C_{IN}9 CDAC Offset Neg Register (Address 0x59) => The contents are the same as those in the C_{IN}0 CDAC Offset Neg Register.

C_{IN}10 CDAC Offset Pos Register (Address 0x5A) => The contents are the same as those in the C_{IN}0 CDAC Offset Pos Register.

C_{IN}10 CDAC Offset Neg Register (Address 0x5B) => The contents are the same as those in the C_{IN}0 CDAC Offset Neg Register.

C_{IN}11 CDAC Offset Pos Register (Address 0x5C) => The contents are the same as those in the C_{IN}0 CDAC Offset Pos Register.

C_{IN}11 CDAC Offset Neg Register (Address 0x5D) => The contents are the same as those in the C_{IN}0 CDAC Offset Neg Register.

C_{IN}12 CDAC Offset Pos Register (Address 0x5E) => The contents are the same as those in the C_{IN}0 CDAC Offset Pos Register.

C_{IN}12 CDAC Offset Neg Register (Address 0x5F) => The contents are the same as those in the C_{IN}0 CDAC Offset Neg Register.

C_{IN}13 CDAC Offset Pos Register (Address 0x60) => The contents are the same as those in the C_{IN}0 CDAC Offset Pos Register.

C_{IN}13 CDAC Offset Neg Register (Address 0x61) => The contents are the same as those in the C_{IN}0 CDAC Offset Neg Register.

Table 30. C_{IN}0 STATIC OFFSET REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x62	Name	C0SOF7	C0SOF6	C0SOF5	C0SOF4	C0SOF3	C0SOF2	C0SOF1	C0SOF0
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

The resister is used to perform offset compensation by computation for the portion which cannot be compensated by the offset adjustment that uses the on-chip capacitance D/A converter. (two's complement)

The contents of this register are automatically updated by the static offset calibration command.

C0SOF7−0	Added Value (Two's Complement)
0x7F	+16256 (0x3F80)
0x7E	+16128 (0x3F00)
0x7D	+16000 (0x3E80)
0x01	+128 (0x0080)
0x00	0 (0x0000)
0xFF	−128 (0xFFFF)
0x82	−16128 (0xC17F)
0x81	−16256 (0xC0FF)
0x80	−16384 (0xC07F)

$C_{IN}1$ Static Offset Register (Address 0x63) => The contents are the same as those in the $C_{IN}0$ Static Offset Register. The value of $C_{IN}0$ Static Offset Register is valid in the differential input mode.

$C_{IN}2$ Static Offset Register (Address 0x64) => The contents are the same as those in the $C_{IN}0$ Static Offset Register.
$C_{IN}3$ Static Offset Register (Address 0x65) => The contents are the same as those in the $C_{IN}0$ Static Offset Register. The value of $C_{IN}2$ Static Offset Register is valid in the differential input mode.

$C_{IN}4$ Static Offset Register (Address 0x66) => The contents are the same as those in the $C_{IN}0$ Static Offset Register.
$C_{IN}5$ Static Offset Register (Address 0x67) => The contents are the same as those in the $C_{IN}0$ Static Offset Register. The value of $C_{IN}4$ Static Offset Register is valid in the differential input mode.

$C_{IN}6$ Static Offset Register (Address 0x68) => The contents are the same as those in the $C_{IN}0$ Static Offset Register.
$C_{IN}7$ Static Offset Register (Address 0x69) => The contents are the same as those in the $C_{IN}0$ Static Offset Register. The value of $C_{IN}6$ Static Offset Register is valid in the differential input mode.

$C_{IN}8$ Static Offset Register (Address 0x6A) => The contents are the same as those in the $C_{IN}0$ Static Offset Register.
$C_{IN}9$ Static Offset Register (Address 0x6B) => The contents are the same as those in the $C_{IN}0$ Static Offset Register. The value of $C_{IN}8$ Static Offset Register is valid in the differential input mode.

$C_{IN}10$ Static Offset Register (Address 0x6C) => The contents are the same as those in the $C_{IN}0$ Static Offset Register.
$C_{IN}11$ Static Offset Register (Address 0x6D) => The contents are the same as those in the $C_{IN}0$ Static Offset Register. The value of $C_{IN}10$ Static Offset Register is valid in the differential input mode.

$C_{IN}12$ Static Offset Register (Address 0x6E) => The contents are the same as those in the $C_{IN}0$ Static Offset Register.
$C_{IN}13$ Static Offset Register (Address 0x6F) => The contents are the same as those in the $C_{IN}0$ Static Offset Register. The value of $C_{IN}12$ Static Offset Register is valid in the differential input mode.

Table 31. $C_{IN}0$ DYNAMIC OFFSET REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x70	Name	C0DOF7	C0DOF6	C0DOF5	C0DOF4	C0DOF3	C0DOF2	C0DOF1	C0DOF0
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

When the dynamic offset calibration enables, the $C_{IN}0$ Dynamic Offset Register value (two's complement) is added to the ΣΔ A/D converter data. The contents of this register are automatically updated by the dynamic offset calibration command.

C0DOF7−0	Added Value (Two's Complement)
0x7F	+16256 (0x3F80)
0x7E	+16128 (0x3F00)
0x7D	+16000 (0x3E80)
|	|
0x01	+128 (0x0080)
0x00	0 (0x0000)
0xFF	−128 (0xFFFF)
|	|
0x82	−16128 (0xC17F)
0x81	−16256 (0xC0FF)
0x80	−16384 (0xC07F)

$C_{IN}1$ Dynamic Offset Register (Address 0x71) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.
The value of $C_{IN}0$ Dynamic Offset Register is valid in the differential input mode.

$C_{IN}2$ Dynamic Offset Register (Address 0x72) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.

$C_{IN}3$ Dynamic Offset Register (Address 0x73) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.
The value of $C_{IN}2$ Dynamic Offset Register is valid in the differential input mode.

$C_{IN}4$ Dynamic Offset Register (Address 0x74) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.

$C_{IN}5$ Dynamic Offset Register (Address 0x75) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.
The value of $C_{IN}4$ Dynamic Offset Register is valid in the differential input mode.

$C_{IN}6$ Dynamic Offset Register (Address 0x76) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.

$C_{IN}7$ Dynamic Offset Register (Address 0x77) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.
The value of $C_{IN}6$ Dynamic Offset Register is valid in the differential input mode.

$C_{IN}8$ Dynamic Offset Register (Address 0x78) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.

$C_{IN}9$ Dynamic Offset Register (Address 0x79) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.
The value of $C_{IN}8$ Dynamic Offset Register is valid in the differential input mode.

$C_{IN}10$ Dynamic Offset Register (Address 0x7A) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.

$C_{IN}11$ Dynamic Offset Register (Address 0x7B) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.
The value of $C_{IN}10$ Dynamic Offset Register is valid in the differential input mode.

$C_{IN}12$ Dynamic Offset Register (Address 0x7C) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.

$C_{IN}13$ Dynamic Offset Register (Address 0x7D) => The contents are the same as those in the $C_{IN}0$ Dynamic Offset Register.
The value of $C_{IN}12$ Dynamic Offset Register is valid in the differential input mode.

Table 32. DYNAMIC OFFSET THRESHOLD REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x7E	Name	−	−	DOFTH5	DOFTH4	DOFTH3	DOFTH2	DOFTH1	DOFTH0
	W/R	−	−	RW	RW	RW	RW	RW	RW

Dynamic offset is automatically compensated when the following condition is established:
|Measurement data – (Data Center Register value) + (C_{IN} Dynamic Offset Register value)| ≤
|Dynamic Offset Threshold Register value|

DOFTH5−0	Value
0x00	0 (0x0000)
0x01	±256 (0x0100)
0x02	±512 (0x0200)
0x3D	±15616 (0x3D00)
0x3E	±15872 (0x3E00)
0x3F	±16128 (0x3F00)

Table 33. DYNAMIC OFFSET LPF/IVAL REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x7F	Name	DOFLPF	−	DOFIVAL5	DOFIVAL4	DOFIVAL3	DOFIVAL2	DOFIVAL1	DOFIVAL0
	W/R	RW	−	RW	RW	RW	RW	RW	RW

This register determines after how many measurements the calibration is to be performed when the dynamic offset calibration enables.

DOFIVAL5−0	Number of Times
0x00	1
0x01	2
0x02	3
0x3D	62
0x3E	63
0x3F	64

A value is added to or subtracted from the Dynamic Offset Register value so that the value of the measurement data matches the value in the Data Center Register.

DOFLPF	Value to be added to or subtracted from the Dynamic Offset Register
0	1
1	2

Table 34. DRIVE X SCAN REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x80	Name	DRVX13	DRVX12	DRVX11	DRVX10	DRVX9	DRVX8	DRVX7	DRVX6
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to configure X drive scanning when the TPDRV bit in the register 0x02 is enabled.

DRVX6−DRVX13: Configures the C_{DRV} pins assigned to $C_{IN}6$ to $C_{IN}13$
0: Disables the C_{DRV} function
1: Enables the C_{DRV} function

Table 35. DRIVE Y SCAN REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x81	Name	−	−	DRVY5	DRVY4	DRVY3	DRVY2	DRVY1	DRVY0
	W/R	−	−	RW	RW	RW	RW	RW	RW

This register is used to configure Y drive scanning when the TPDRV bit in the register 0x02 is enabled.

DRVY0−DRVY5: Configures the C_{DRV} pins assigned to $C_{IN}0$ to $C_{IN}5$
0: Disables the C_{DRV} function
1: Enables the C_{DRV} function

Table 36. RESERVED REGISTER 1

	Bit	7	6	5	4	3	2	1	0
Address 0x82	Name	−	−	−	−	−	−	RSV1_1	RSV1_0
	W/R	−	−	−	−	−	−	RW	RW

This register is reserved.

RSV1_0−RSV1_1 Reserved Register 1
Normally, 0x00 must be written into this register and used.

Table 37. C_{DRV} FREQUENCY VARIABLE REGISTER

	Bit	7	6	5	4	3	2	1	0
Address 0x83	Name	FSEL3	FSEL2	FSEL1	FSEL0	RSV2_3	RSV2_2	RSV2_1	RSV2_0
	W/R	RW	RW	RW	RW	RW	RW	RW	RW

FSEL0−FSEL3 C_{DRV} drive frequency adjustment.
Normally, 0x5 must be set. In case of the C_{DRV} drive frequency is adjusted, it is possible to adjust shown below.

FSEL0−FSEL3	Frequency Ratio (%) (Against 0x5)
0x0	−20
0x1	−17
0x2	−12
0x3	−9
0x4	−5
0x5	0
0x6	6
0x7	13
0x8	19
0x9	27

30. Reference value (T_A = 25°C, AV_{DD} = 2.8 V)

RSV2_0−RSV2_3 Reserved Register 2
Normally, 0x7 must be written into this register and used.

31. All frequency, time, voltage, degrees of amplification and other values given in the specifications except for the absolute maximum ratings, recommended operating ranges and electrical characteristics are only reference values, and no guarantees are made for these values.

Register Map

Table 38. REGISTER MAP

	Controller Register Address	256-byte EEPROM Address	Symbol	Name
GENERAL REGISTER				
1	0x00	−		Control Register
2	0x01	−		Configuration Register 1
3	0x02	−		Configuration Register 2
4	0x03	−		GPO Control Register 1
5	0x04	−		GPO Control Register 2
6	0x05	−		INT Status Register 1
7	0x06	−		INT Status Register 2
8	0x07	−		Data00 Register
9	0x08	−		Data01 Register
10	0x09	−		Data02 Register
11	0x0A	−		Data03 Register
12	0x0B	−		Data04 Register
13	0x0C	−		Data05 Register
14	0x0D	−		Data06 Register
15	0x0E	−		Data07 Register
16	0x0F	−		Data08 Register
17	0x10	−		Data09 Register
18	0x11	−		Data10 Register
19	0x12	−		Data11 Register
20	0x13	−		Data12 Register
21	0x14	−		Data13 Register
22	0x15	−		Data14 Register
23	0x16	−		Data15 Register
24	0x17	−		Data16 Register
25	0x18	−		Data17 Register
26	0x19	−		Data18 Register
27	0x1A	−		Data19 Register
28	0x1B	−		Data20 Register
29	0x1C	−		Data21 Register
30	0x1D	−		Data22 Register
31	0x1E	−		Data23 Register
32	0x1F	−		Data24 Register
33	0x20	−		Data25 Register
34	0x21	−		Data26 Register
35	0x22	−		Data27 Register
36	0x23	−		EEPROM Write Protect/Initialize Register
37	0x24	−		First Fixed Register

Table 38. REGISTER MAP (continued)

	Controller Register Address	256-byte EEPROM Address	Symbol	Name
PARAMETER REGISTERS				
38	0x25	0x00		Controller I^2C Slave Address Register
39	0x26	0x01		$C_{IN}0$−$C_{IN}1$ Configuration Register 1
40	0x27	0x02		$C_{IN}0$−$C_{IN}1$ Configuration Register 2
41	0x28	0x03		$C_{IN}2$−$C_{IN}3$ Configuration Register 1
42	0x29	0x04		$C_{IN}2$−$C_{IN}3$ Configuration Register 2
43	0x2A	0x05		$C_{IN}4$−$C_{IN}5$ Configuration Register 1
44	0x2B	0x06		$C_{IN}4$−$C_{IN}5$ Configuration Register 2
45	0x2C	0x07		$C_{IN}6$−$C_{IN}7$ Configuration Register 1
46	0x2D	0x08		$C_{IN}6$−$C_{IN}7$ Configuration Register 2
47	0x2E	0x09		$C_{IN}8$−$C_{IN}9$ Configuration Register 1
48	0x2F	0x0A		$C_{IN}8$−$C_{IN}9$ Configuration Register 2
49	0x30	0x0B		$C_{IN}10$−$C_{IN}11$ Configuration Register 1
50	0x31	0x0C		$C_{IN}10$−$C_{IN}11$ Configuration Register 2
51	0x32	0x0D		$C_{IN}12$−$C_{IN}13$ Configuration Register 1
52	0x33	0x0E		$C_{IN}12$−$C_{IN}13$ Configuration Register 2
53	0x34	0x0F		Data Center Register
54	0x35	0x10		Single INT Threshold Register
55	0x36	0x11		Differential INT Threshold Register
56	0x37	0x12		INT Count Register
57	0x38	0x13		$C_{IN}0$ Gain Register
58	0x39	0x14		$C_{IN}1$ Gain Register
59	0x3A	0x15		$C_{IN}2$ Gain Register
60	0x3B	0x16		$C_{IN}3$ Gain Register
61	0x3C	0x17		$C_{IN}4$ Gain Register
62	0x3D	0x18		$C_{IN}5$ Gain Register
63	0x3E	0x19		$C_{IN}6$ Gain Register
64	0x3F	0x1A		$C_{IN}7$ Gain Register
65	0x40	0x1B		$C_{IN}8$ Gain Register
66	0x41	0x1C		$C_{IN}9$ Gain Register
67	0x42	0x1D		$C_{IN}10$ Gain Register
68	0x43	0x1E		$C_{IN}11$ Gain Register
69	0x44	0x1F		$C_{IN}12$ Gain Register
70	0x45	0x20		$C_{IN}13$ Gain Register
71	0x46	0x21		$C_{IN}0$ CDAC Offset Pos Register
72	0x47	0x22		$C_{IN}0$ CDAC Offset Neg Register
73	0x48	0x23		$C_{IN}1$ CDAC Offset Pos Register
74	0x49	0x24		$C_{IN}1$ CDAC Offset Neg Register
75	0x4A	0x25		$C_{IN}2$ CDAC Offset Pos Register
76	0x4B	0x26		$C_{IN}2$ CDAC Offset Neg Register
77	0x4C	0x27		$C_{IN}3$ CDAC Offset Pos Register

Table 38. REGISTER MAP (continued)

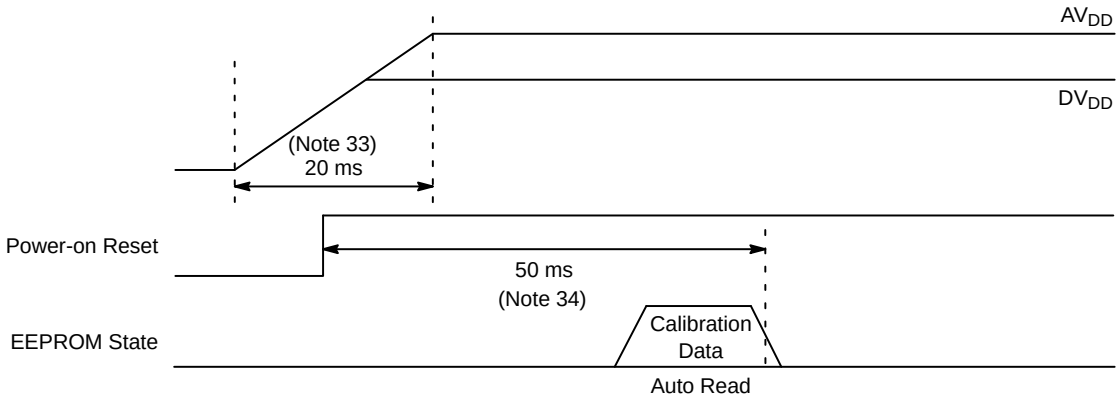
	Controller Register Address	256-byte EEPROM Address	Symbol	Name
PARAMETER REGISTERS				
78	0x4D	0x28		C_{IN}3 CDAC Offset Neg Register
79	0x4E	0x29		C_{IN}4 CDAC Offset Pos Register
80	0x4F	0x2A		C_{IN}4 CDAC Offset Neg Register
81	0x50	0x2B		C_{IN}5 CDAC Offset Pos Register
82	0x51	0x2C		C_{IN}5 CDAC Offset Neg Register
83	0x52	0x2D		C_{IN}6 CDAC Offset Pos Register
84	0x53	0x2E		C_{IN}6 CDAC Offset Neg Register
85	0x54	0x2F		C_{IN}7 CDAC Offset Pos Register
86	0x55	0x30		C_{IN}7 CDAC Offset Neg Register
87	0x56	0x31		C_{IN}8 CDAC Offset Pos Register
88	0x57	0x32		C_{IN}8 CDAC Offset Neg Register
89	0x58	0x33		C_{IN}9 CDAC Offset Pos Register
90	0x59	0x34		C_{IN}9 CDAC Offset Neg Register
91	0x5A	0x35		C_{IN}10 CDAC Offset Pos Register
92	0x5B	0x36		C_{IN}10 CDAC Offset Neg Register
93	0x5C	0x37		C_{IN}11 CDAC Offset Pos Register
94	0x5D	0x38		C_{IN}11 CDAC Offset Neg Register
95	0x5E	0x39		C_{IN}12 CDAC Offset Pos Register
96	0x5F	0x3A		C_{IN}12 CDAC Offset Neg Register
97	0x60	0x3B		C_{IN}13 CDAC Offset Pos Register
98	0x61	0x3C		C_{IN}13 CDAC Offset Neg Register
99	0x62	0x3D		C_{IN}0 Static Offset Register
100	0x63	0x3E		C_{IN}1 Static Offset Register
101	0x64	0x3F		C_{IN}2 Static Offset Register
102	0x65	0x40		C_{IN}3 Static Offset Register
103	0x66	0x41		C_{IN}4 Static Offset Register
104	0x67	0x42		C_{IN}5 Static Offset Register
105	0x68	0x43		C_{IN}6 Static Offset Register
106	0x69	0x44		C_{IN}7 Static Offset Register
107	0x6A	0x45		C_{IN}8 Static Offset Register
108	0x6B	0x46		C_{IN}9 Static Offset Register
109	0x6C	0x47		C_{IN}10 Static Offset Register
110	0x6D	0x48		C_{IN}11 Static Offset Register
111	0x6E	0x49		C_{IN}12 Static Offset Register
112	0x6F	0x4A		C_{IN}13 Static Offset Register
113	0x70	0x4B		C_{IN}0 Dynamic Offset Register
114	0x71	0x4C		C_{IN}1 Dynamic Offset Register
115	0x72	0x4D		C_{IN}2 Dynamic Offset Register
116	0x73	0x4E		C_{IN}3 Dynamic Offset Register
117	0x74	0x4F		C_{IN}4 Dynamic Offset Register

Table 38. REGISTER MAP (continued)

	Controller Register Address	256-byte EEPROM Address	Symbol	Name
PARAMETER REGISTERS				
118	0x75	0x50		$C_{IN}5$ Dynamic Offset Register
119	0x76	0x51		$C_{IN}6$ Dynamic Offset Register
120	0x77	0x52		$C_{IN}7$ Dynamic Offset Register
121	0x78	0x53		$C_{IN}8$ Dynamic Offset Register
122	0x79	0x54		$C_{IN}9$ Dynamic Offset Register
123	0x7A	0x55		$C_{IN}10$ Dynamic Offset Register
124	0x7B	0x56		$C_{IN}11$ Dynamic Offset Register
125	0x7C	0x57		$C_{IN}12$ Dynamic Offset Register
126	0x7D	0x58		$C_{IN}13$ Dynamic Offset Register
127	0x7E	0x59		Dynamic Offset Threshold Register
128	0x7F	0x5A		Dynamic Offset LPF/IVAL Register
129	0x80	0x5B		Drive X Scan Register
130	0x81	0x5C		Drive Y Scan Register
131	0x82	0x5D		Reserved Register 1
132	0x83	0x5E		C_{DRV} Frequency Variable Register
USER AREA				
–	–	0x5F to 0xFF		User Area

32. Registers with the shading are ones that are automatically updated by auto offset calibration.

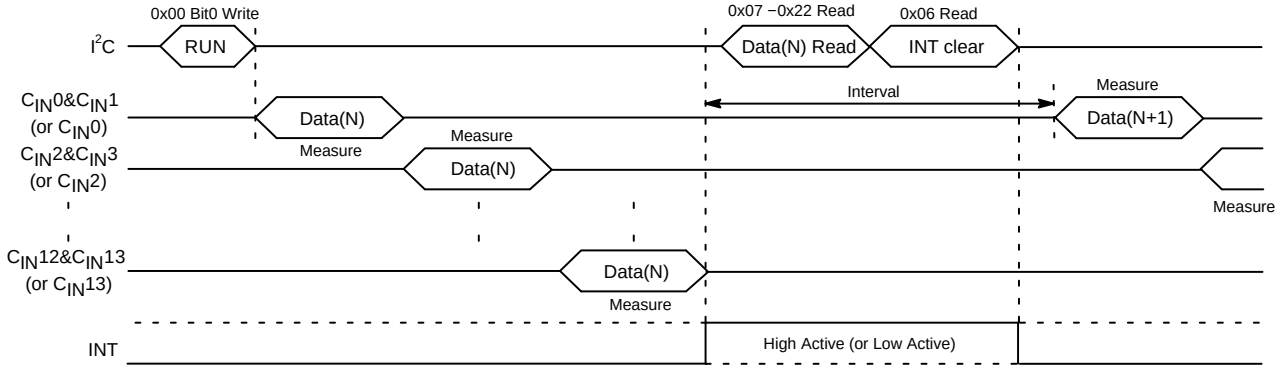
Operation Sequences



33. As shown in Figure 6, the power supply (AV_{DD}, DV_{DD}) startup must be completed within 20 ms.
34. As shown in Figure 6, a period of 50 ms or longer must be provided as the time required to complete the automatic reading of the calibration data.
35. The I^2C bus (SDA, SCL pins) needs pull-up resistors to DV_{DD}.
36. Since a static breakdown protection element is inserted between AV_{DD} and DV_{DD}, the LSI must always be used under the condition of $AV_{DD} \geq DV_{DD}$ without fail.

Figure 6. Power-on Sequence

1. The power supplies (AV_{DD}, DV_{DD}) are started up within 20 ms after the power has been turned on. (After the power-on reset circuit is activated, the reset state is released.)
2. The calibration data is automatically loaded from the EEPROM into the parameter registers (addresses 0x25 to 0x83). (Auto read function)
3. After the auto read sequence is finished, data is written into the 0x23 EEPROM Write Protect/Initialize Register in the order of 0x01 −> 0x00 −> 0x01 to initialize the LSI.



37. The measurement data must be read during measurement interval time or after the measurements have been stopped (by writing a 0 into bit 0 of address 0x00) during measurement interval time.
38. When you access a device (including this LSI) connected on the same I^2C bus, you must confirm that the measurements have been stopped or during measurement interval time.

Figure 7. Normal Mode Operating Sequence

1. The required functions are set up through the Configuration Register 1, 2 at addresses 0x01 and 0x02.
2. A 1 is written into bit 0 of the 0x00 Control Register (RUN). At the same time, the measurement intervals are also set.
3. When the $C_{IN}0$ to $C_{IN}13$ measurements are finished, an interrupt signal is generated from the INT pin.
4. By reading the 0x06 INT Status Register 2, the interrupt signal is cleared.
5. The measurements continue until a 0 is written into bit 0 of the 0x00 Control Register (standby).

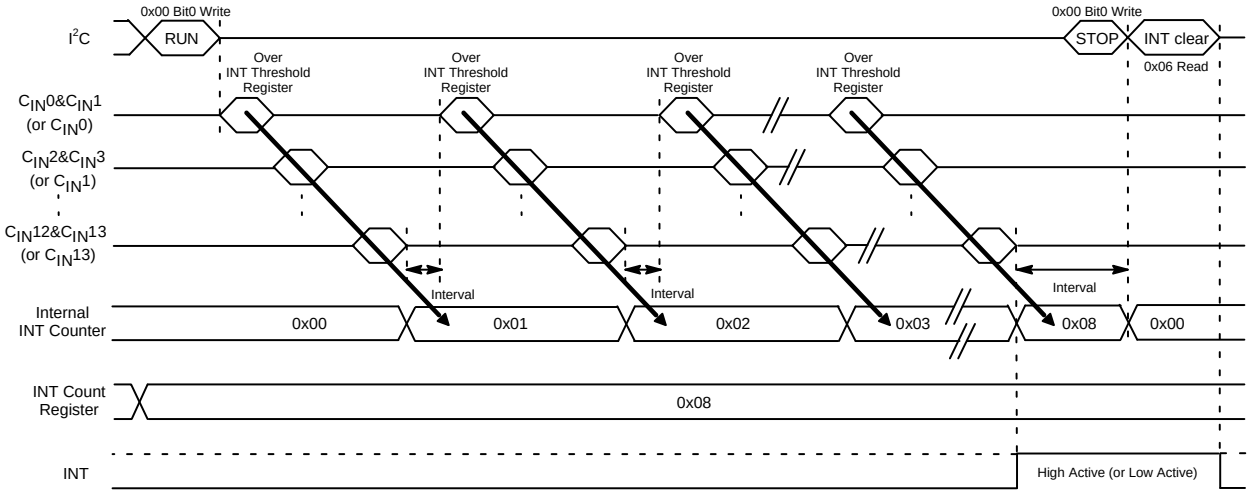


Figure 8. Operation Detection Mode Sequence

1. The operation detection threshold value is written into the Differential (or Single) INT Threshold Register at address 0x36 (or 0x35).
2. The 0x37 INT Count Register is used to specify how many consecutive operation times need to be detected to generate an interrupt. (In Figure 8, the setting is for 8 consecutive times.)
3. The required functions are set up through the Configuration Register 1, 2 at addresses 0x01 and 0x02.
4. A 1 is written into bit 0 of the 0x00 Control Register (RUN). At the same time, the measurement intervals are also set.
5. When the measurement results exceed the specified threshold value, the internal interrupt counter is incremented. (In Figure 8, it is assumed that the threshold value specified by the 0x36 (or 0x35) Differential (or Single) INT Threshold Register is exceeded.)
6. When the value of the internal interrupt counter becomes equal to the value of the INT Count Register, an interrupt signal is generated from the INT pin.
7. The measurements have been stopped (by writing a 0 into bit 0 of address 0x00) during measurement interval time.
8. By reading the 0x06 INT Status Register 2, the interrupt signal is cleared.

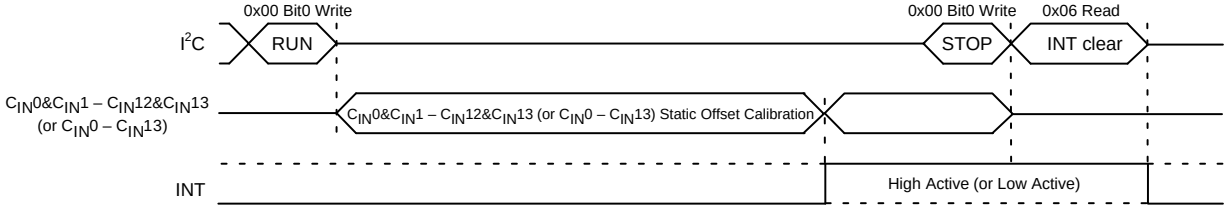
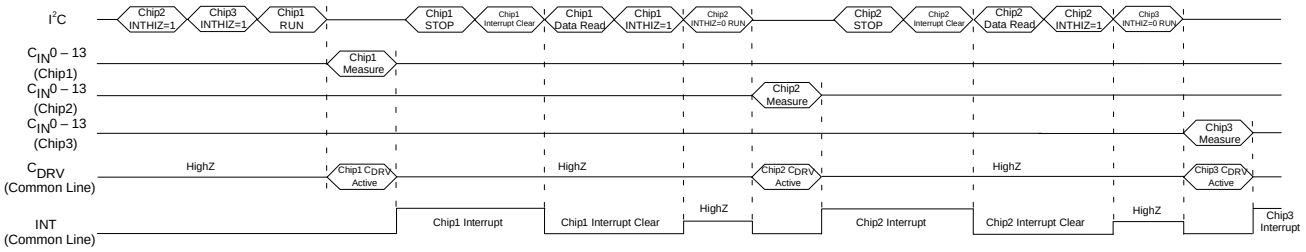


Figure 9. Static Offset Calibration Sequence

1. The required functions are set up through the Configuration Register 1, 2 at addresses 0x01 and 0x02. At this time, a 1 is written into bit 7 (static offset calibration mode).
2. A 1 is written into bit 0 of the 0x00 Control Register (to start static offset calibration).
3. When the $C_{IN}0$ to $C_{IN}13$ static offset calibration is finished, an interrupt signal is generated from the INT pin, and the calibrated values are automatically written into the 0x62 to 0x6F $C_{IN}0$ to $C_{IN}13$ Static Offset Register.
4. Calibration continues until a 0 is written into bit 0 of the 0x00 Control Register (standby).
5. By reading the 0x06 INT Status Register 2, the interrupt signal is cleared.



39. At all times except when the measurement is being performed, the common lines connected to the INT pin must be set to high or low without fail.
40. The measurement data must be read during measurement interval time or after the measurements have been stopped (by writing a 0 into bit 0 of address 0x00) during measurement interval time.
41. When you access a device (including this LSI) connected on the same I^2C bus, you must confirm that the measurements have been stopped or during measurement interval time.

Figure 10. Operation Sequence when a Multiple Number of LC71F7001PVB is Used

1. The example when 3 chips (chip 1, chip 2 and chip 3) are used is explained as follows.
2. Bit 5 of the 0x00 Control Register of chip 2 and chip 3 are set to 1 to place the INT pin in the high-impedance state.
3. The chip 1 measurements are started. After an interrupt signal is generated from chip 1, the chip 1 measurements are terminated and the chip 1 measurement data is read.
4. Bit 5 of the 0x00 Control Register of chip 1 is set to 1 to place the INT pin in the high-impedance state.
5. Bit 5 of the 0x00 Control Register of chip 2 is set to 0 (to release the INT pin from high-impedance state) and bit 0 of the same register to 1 (RUN) to start the chip 2 measurements. The chip 2 measurements are terminated after an interrupt signal is generated from chip 2. The measurement data is then read from chip 2.
6. Bit 5 of the 0x00 Control Register of chip 2 is set to 1 to place the INT pin in the high-impedance state.
7. Bit 5 of the 0x00 Control Register of chip 3 is set to 0 (to release the INT pin from high-impedance state) and bit 0 of the same register to 1 (RUN) to start chip 3 measurements. The chip 3 measurements are terminated after an interrupt signal is generated from chip 3. The measurement data is then read from chip 3.

Table 39. ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)†
LC71F7001PVBS0−TLM−H	SSOP24 (225 mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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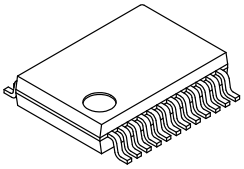
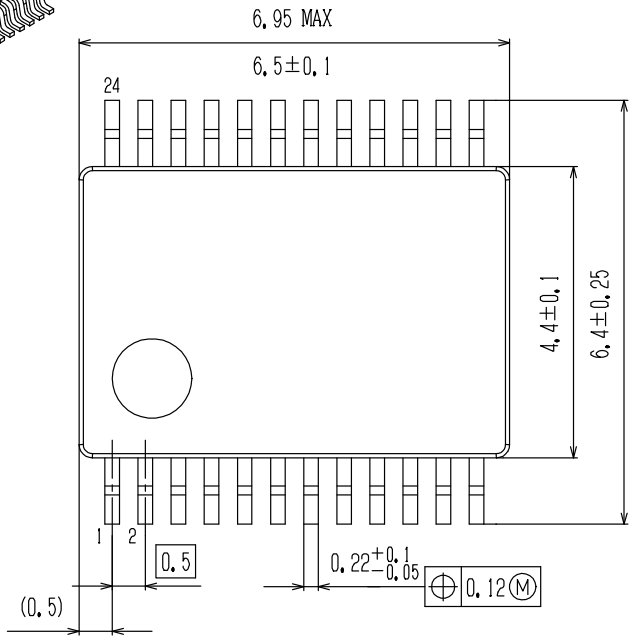
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

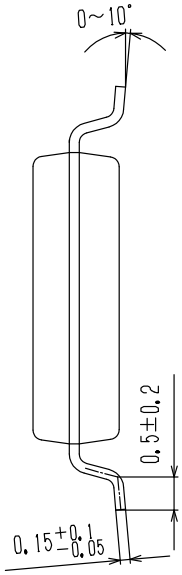
ON Semiconductor®

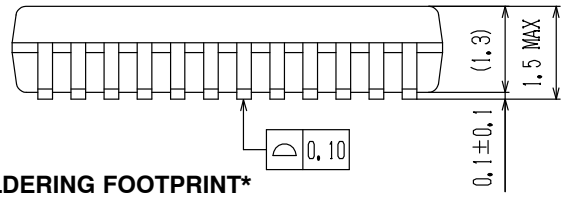
SSOP24 (225mil)
CASE 565AR
ISSUE A

DATE 23 OCT 2013

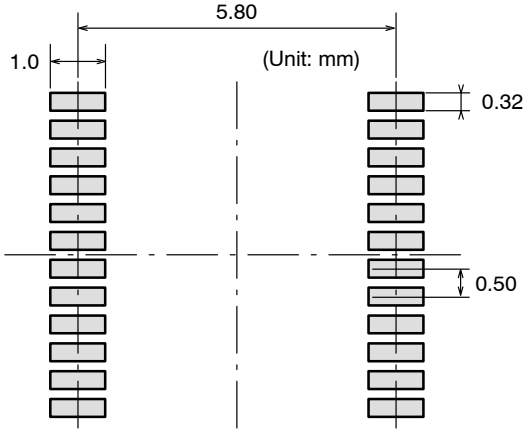








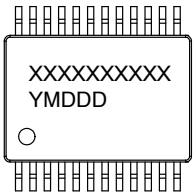
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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