

NVHL072N65S3

MOSFET – Power, **N-Channel, SUPERFET® III,** **Automotive, Easy-drive**

650 V, 44 A, 72 mΩ

Description

SuperFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SuperFET III MOSFET Easy-drive series helps manage EMI issues and allows for easier design implementation.

Features

- AEC-Q101 Qualified
- Max Junction Temperature 150°C
- Typ. $R_{DS(on)} = 61\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_G = 82\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{OSS(eff.)} = 724\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

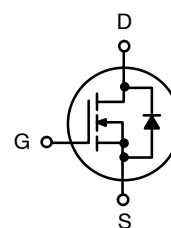
- Automotive PHEV-BEV DC-DC Converter
- Automotive Onboard Charger for PHEV-BEV



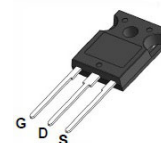
ON Semiconductor®

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BV_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	72 mΩ @ 10 V	44 A

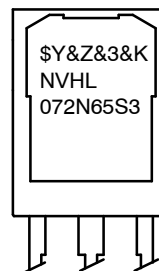


N-Channel MOSFET



**TO-247-3LD
CASE 340CX**

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
NVHL072N65S3 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NVHL072N65S3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		650	V
V _{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I _D	Drain Current	Continuous (T _C = 25°C)	44	A
		Continuous (T _C = 100°C)	28	A
I _{DM}	Pulsed Drain Current	Pulsed (Note 1)	110	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		214	mJ
E _{AR}	Repetitive Avalanche (Note 1)		3.12	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	V/ns
P _D	Power Dissipation	(T _C = 25°C)	312	W
		Derate Above 25°C	2.5	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. I_{AS} = 4.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} < 44 A, di/dt ≤ 200 A/ms, V_{DD} ≤ BVDSS, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max	0.37	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max	40	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Shipping (Qty / Packing)
NVHL072N65S3	NVHL072N65S3	TO-247-3LD	Tube	30 Units / Tube

NVHL072N65S3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	-	-	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	0.60	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	-	0.30	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _c = 125°C	-	7.30	-	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 1.0 mA	2.5	-	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 22 A, T _J = 25°C	-	61	72	mΩ
		V _{GS} = 10 V, I _D = 22 A, T _J = 100°C	-	107	-	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 44 A	-	29.7	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	-	3300	-	pF
C _{oss}	Output Capacitance		-	72.8	-	pF
C _{rss}	Reverse Transfer Capacitance		-	14.6	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	724	-	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	104	-	pF
Q _{g(tot)}	Total Gate Charge	V _{DS} = 400 V, V _{GS} = 10 V, I _D = 44 A (Note 4)	-	82.0	-	nC
Q _{gs}	Gate to Source Gate Charge		-	23.3	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	34.0	-	nC
R _G	Gate Resistance		f = 1 MHz	-	0.685	-

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 44 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	-	26.3	-	ns
t _r	Turn-On Rise Time		-	50	-	ns
t _{d(off)}	Turn-Off Delay Time		-	65.9	-	ns
t _f	Fall Time		-	32	-	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	44	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	110	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 22 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 44 A dI _F /dt = 100 A/μs	-	576	-	nS
Q _{rr}	Reverse Recovery Charge		-	14.3	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

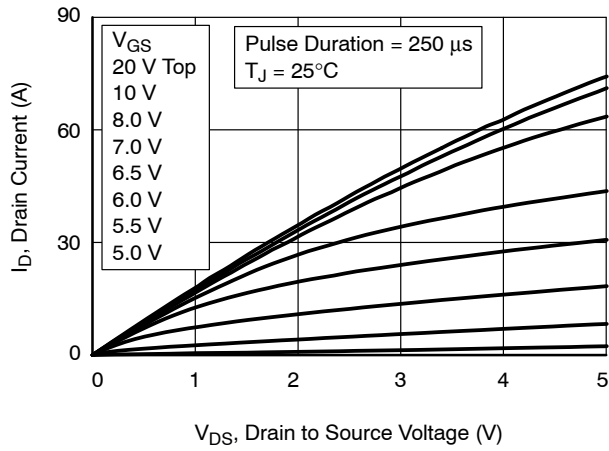


Figure 1. Saturation Characteristics

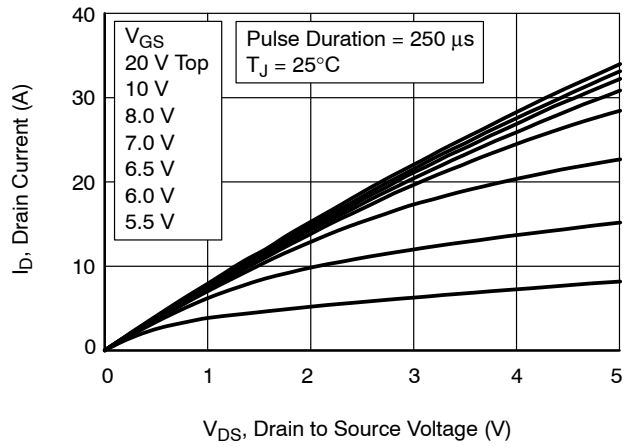


Figure 2. Saturation Characteristics

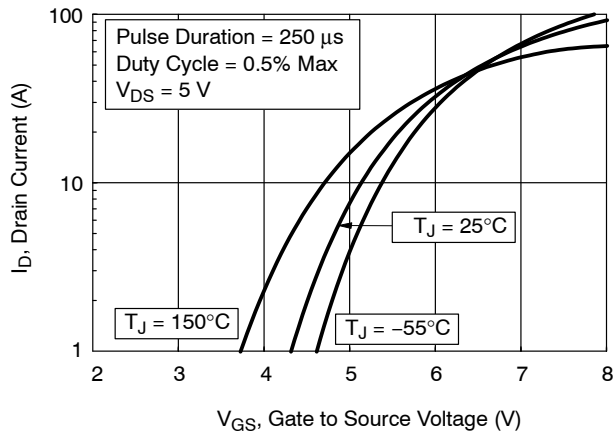


Figure 3. Transfer Characteristic

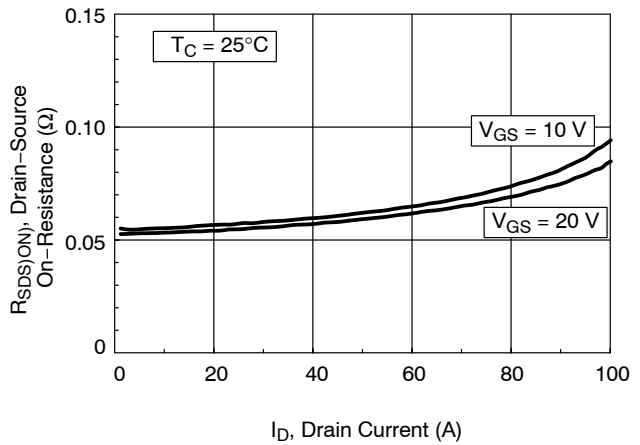


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

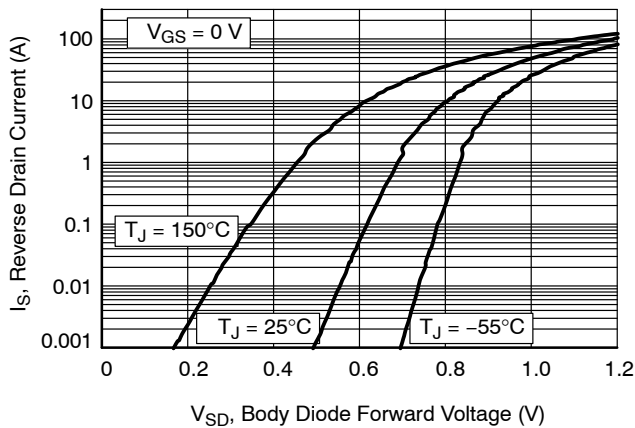


Figure 5. Forward Diode Characteristics

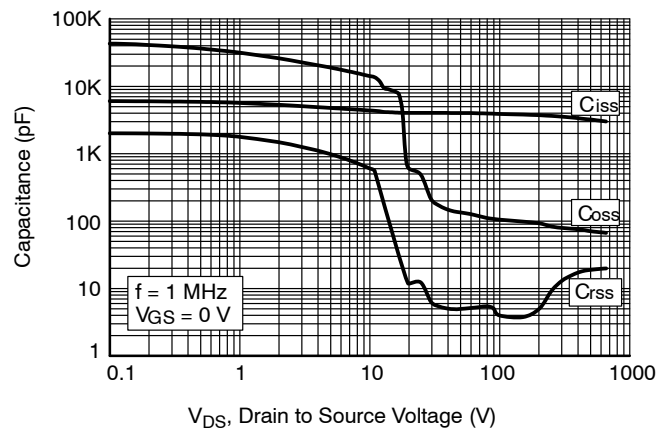


Figure 6. Capacitance vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (continued)

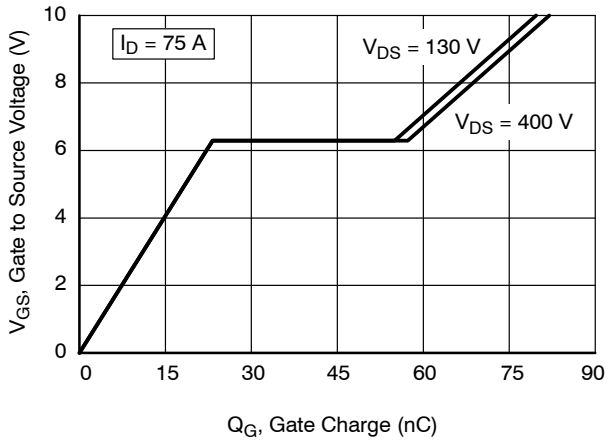


Figure 7. Gate Charge vs. Gate to Source Voltage

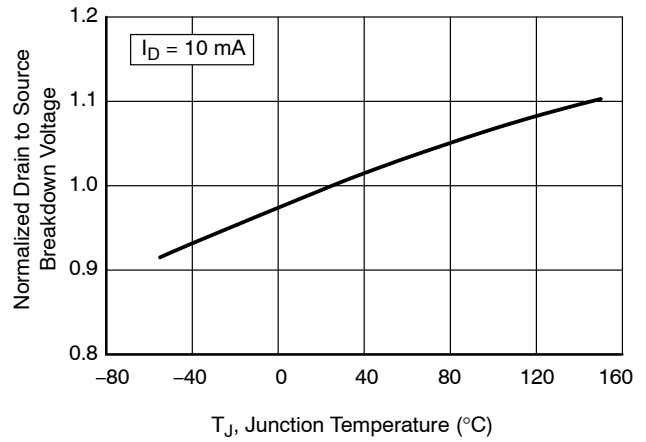


Figure 8. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

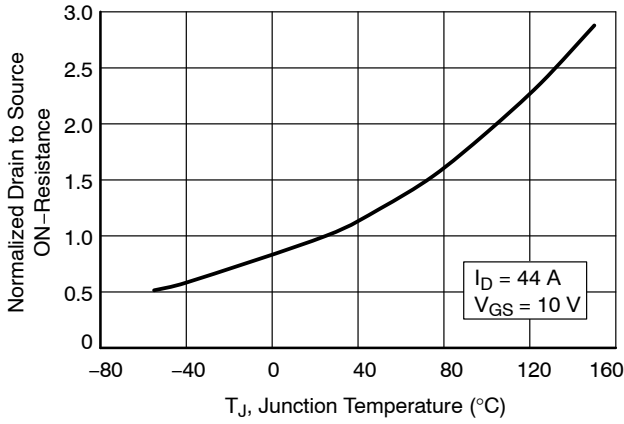


Figure 9. Normalized $R_{DS(on)}$ vs. Junction Temperature

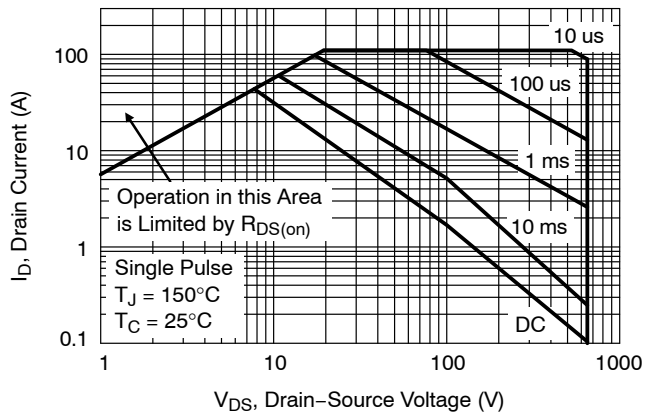


Figure 10. Forward Bias Safe Operating Area

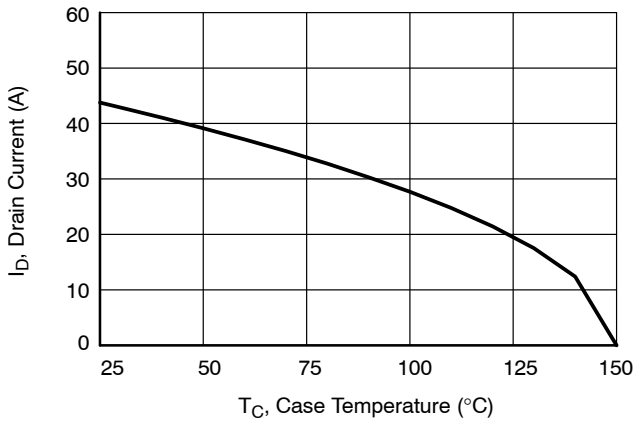


Figure 11. Maximum Continuous Drain Current vs. Case Temperature

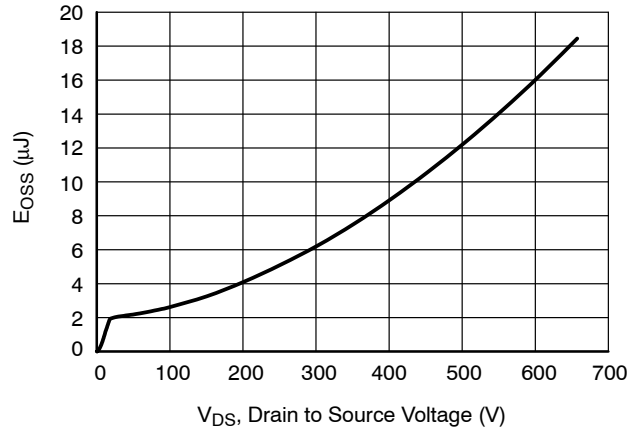


Figure 12. E_{OSS} vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (continued)

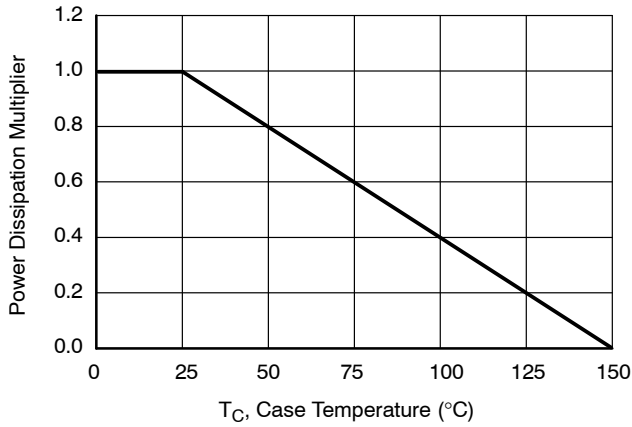


Figure 13. Normalized Power Dissipation vs. Case Temperature

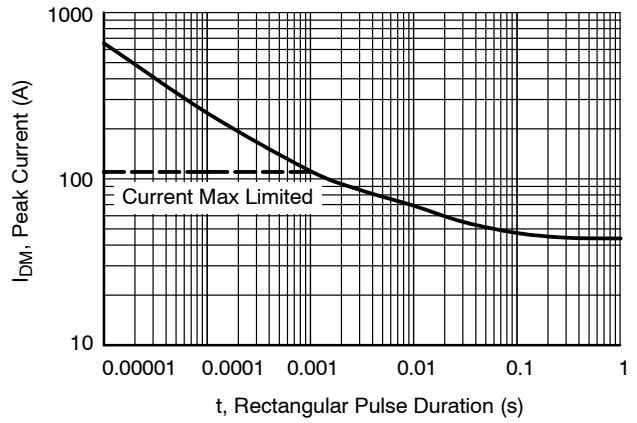


Figure 14. Peak Current Capability

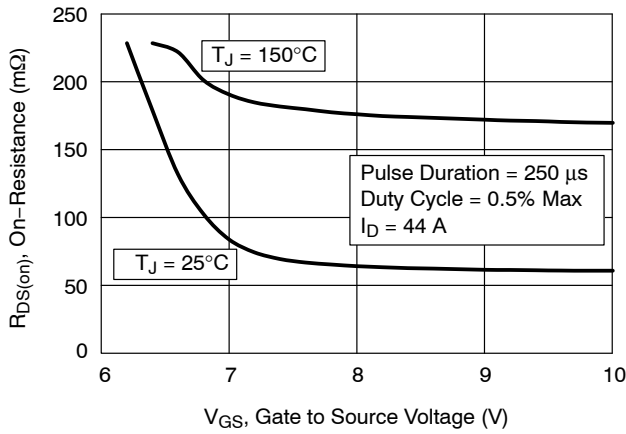


Figure 15. E_{OSS} vs. Drain to Source Voltage

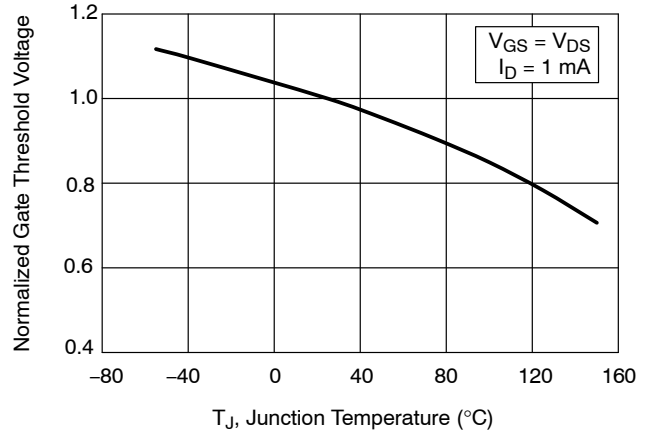


Figure 16. Normalized Gate Threshold Voltage vs. Temperature

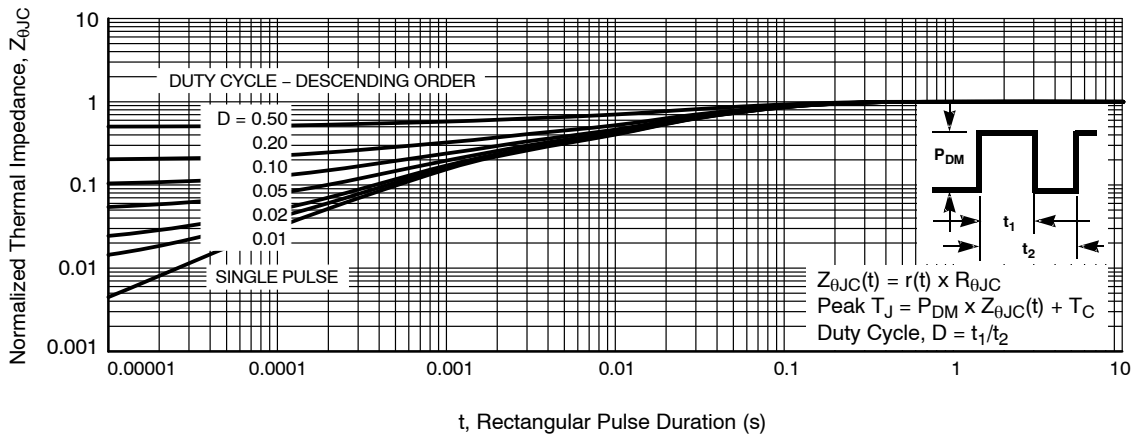


Figure 17. Normalized Maximum Transient Thermal Impedance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TO-247-3LD	PAGE 1 OF 1

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