

# NTGS5120P, NVGS5120P

## MOSFET – Power, Single, P-Channel, TSOP-6 -60 V, -2.9 A

### Features

- 60 V BVds, Low R<sub>DS(on)</sub> in TSOP-6 Package
- 4.5 V Gate Rating
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

### Applications

- High Side Load Switch
- Power Switch for Printers, Communication Equipment

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V <sub>DSS</sub>	-60	V	
Gate-to-Source Voltage		V <sub>GS</sub>	±20	V	
Continuous Drain Current (Note 1)	Steady State	I <sub>D</sub>	T <sub>A</sub> = 25°C	-2.5	A
			T <sub>A</sub> = 85°C	-2.0	
	t ≤ 5 s	T <sub>A</sub> = 25°C	-2.9		
Power Dissipation (Note 1)	Steady State	P <sub>D</sub>	T <sub>A</sub> = 25°C	1.1	W
	t ≤ 5 s		1.4		
Continuous Drain Current (Note 2)	Steady State	I <sub>D</sub>	T <sub>A</sub> = 25°C	-1.8	A
			T <sub>A</sub> = 85°C	-1.3	
Power Dissipation (Note 2)	Steady State	P <sub>D</sub>	T <sub>A</sub> = 25°C	0.6	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs	I <sub>DM</sub>	-20	A	
Operating Junction and Storage Temperature		T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

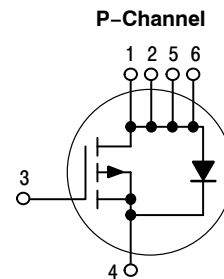
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size.



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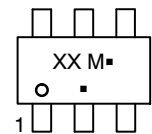
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
-60 V	111 mΩ @ -10 V	-2.9 A
	142 mΩ @ -4.5 V	



### MARKING DIAGRAM

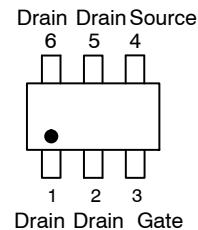


TSOP-6  
CASE 318G  
STYLE 1



XX = Device Code  
M = Date Code  
■ = Pb-Free Package  
(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NTGS5120P, NVGS5120P

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	102	°C/W
Junction-to-Ambient – $t = 5$ s (Note 3)	$R_{\theta JA}$	77.6	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	200	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)  
 4. Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ $\mu$ A	-60			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = -48$ V	$T_J = 25^\circ\text{C}$		-1.0	$\mu$ A
			$T_J = 125^\circ\text{C}$		-5.0	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			$\pm 100$	nA
		$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 200$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = -250$ $\mu$ A	-1.0		-3.0	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -2.9$ A		72	111	m $\Omega$
		$V_{GS} = -4.5$ V, $I_D = -2.5$ A		88	142	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5.0$ V, $I_D = -6.0$ A		10.1		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -30$ V		942		pF
Output Capacitance	$C_{OSS}$			72		
Reverse Transfer Capacitance	$C_{RSS}$			48		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10$ V, $V_{DS} = -30$ V; $I_D = -2.9$ A		18.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.2		
Gate-to-Source Charge	$Q_{GS}$			2.7		
Gate-to-Drain Charge	$Q_{GD}$			3.6		

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10$ V, $V_{DS} = -30$ V, $I_D = -1.0$ A, $R_G = 6.0$ $\Omega$		8.7		ns
Rise Time	$t_r$			4.9		
Turn-Off Delay Time	$t_{d(OFF)}$			38		
Fall Time	$t_f$			12.8		

### DRAIN-SOURCE DIODE CHARACTERISTICS

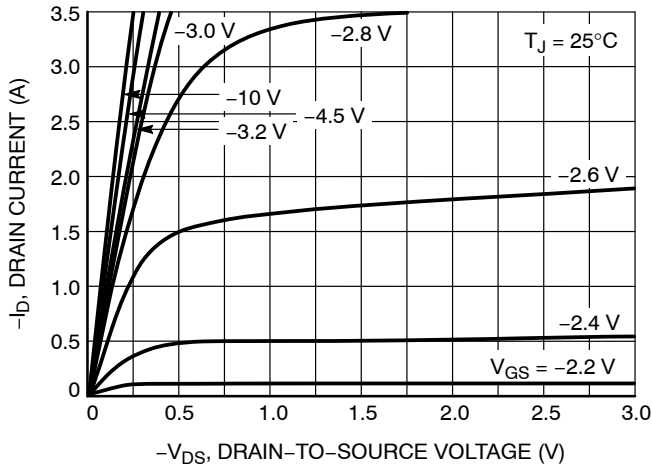
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0$ V, $I_S = -0.9$ A	$T_J = 25^\circ\text{C}$		-0.75	-1.0	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0$ V, $dI_S/dt = 100$ A/ $\mu$ s, $I_S = -0.9$ A			18.3		ns
Charge Time	$t_a$				15.5		ns
Reverse Recovery Charge	$Q_{RR}$				15.1		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

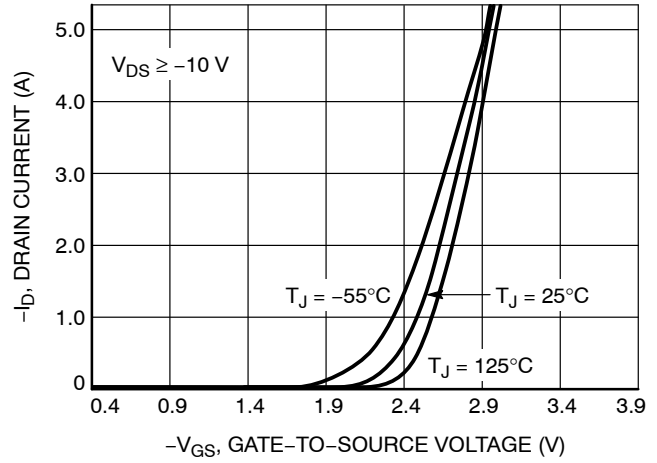
5. Pulse Test: pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2\%$   
 6. Switching characteristics are independent of operating junction temperatures

# NTGS5120P, NVGS5120P

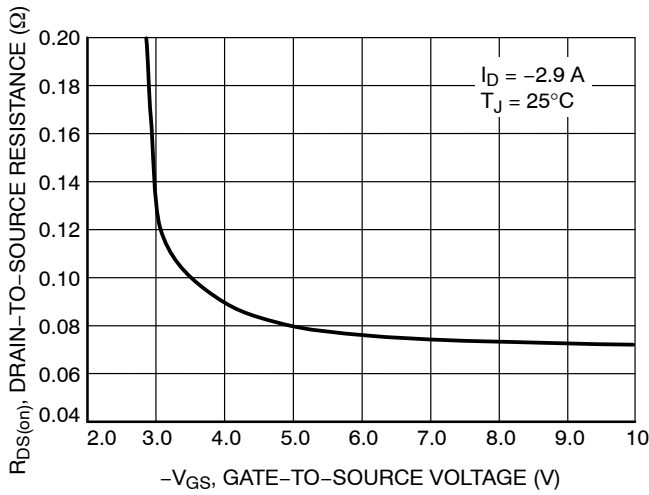
## TYPICAL CHARACTERISTICS



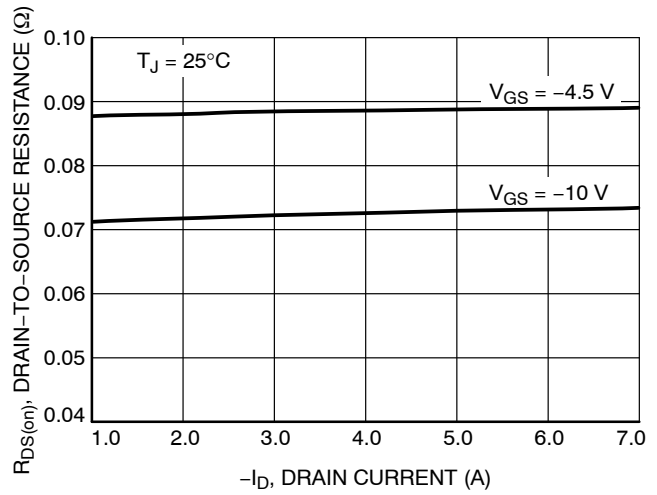
**Figure 1. On-Region Characteristics**



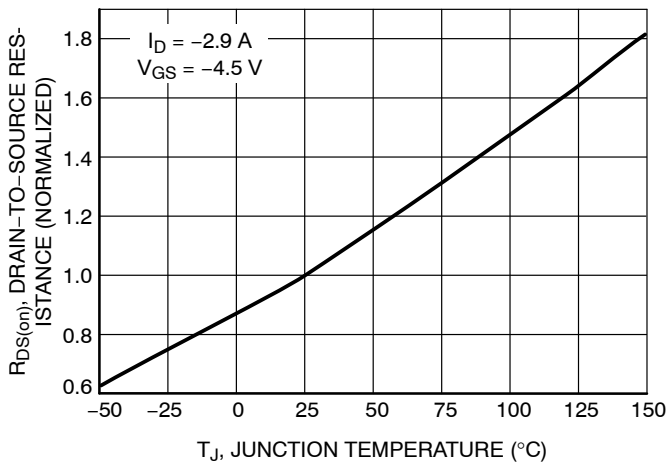
**Figure 2. Transfer Characteristics**



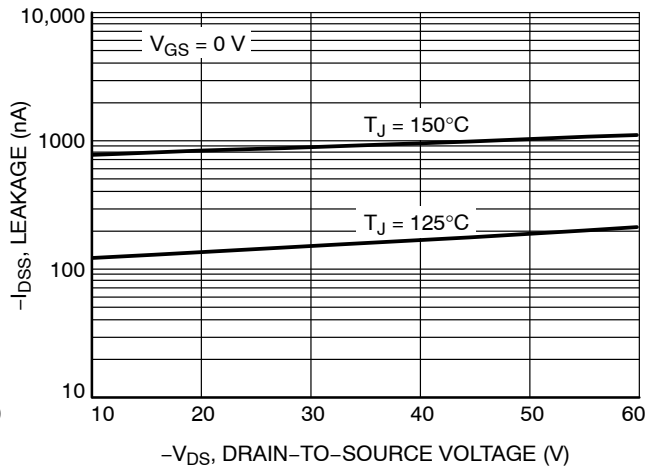
**Figure 3. On-Resistance vs. Gate Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

# NTGS5120P, NVGS5120P

## TYPICAL CHARACTERISTICS

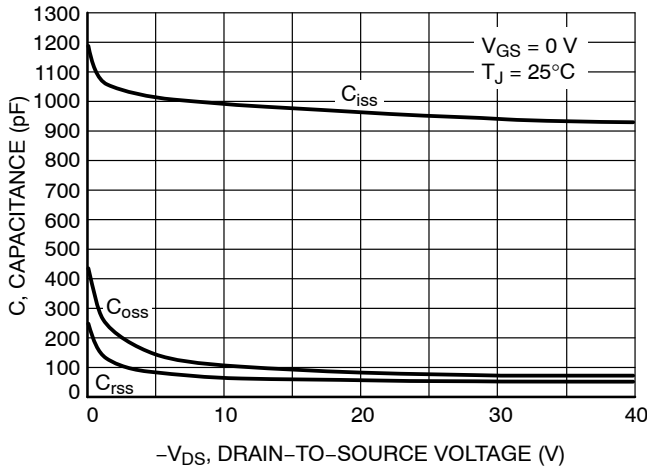


Figure 7. Capacitance Variation

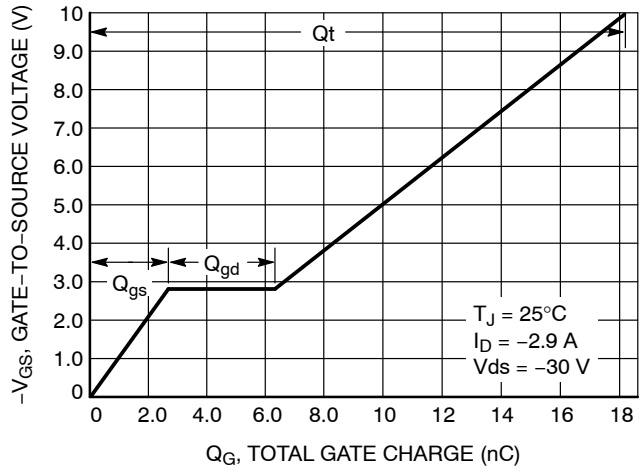


Figure 8. Gate-to-Source Voltage vs. Total Charge

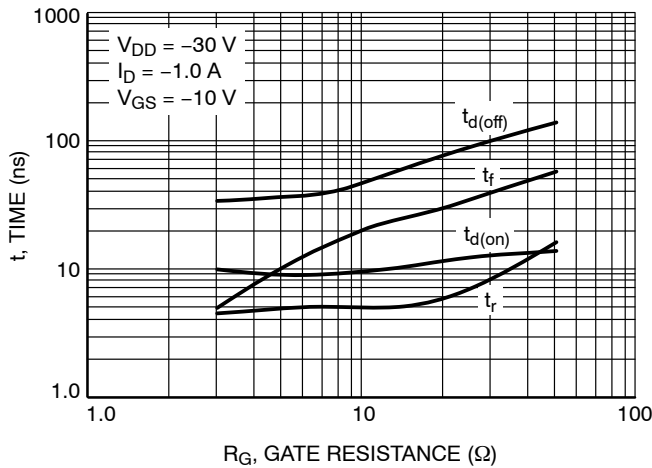


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

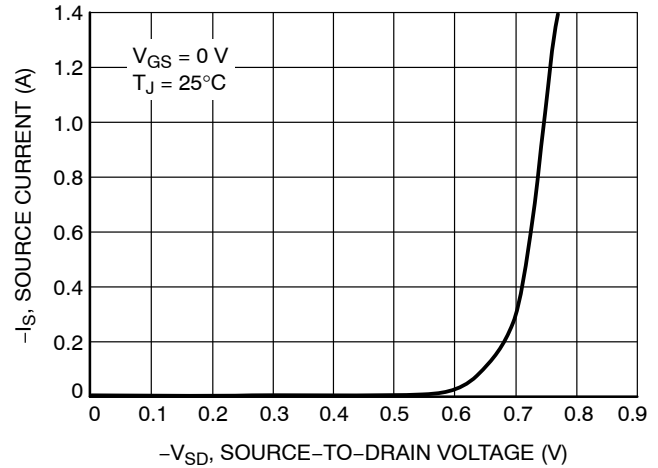


Figure 10. Diode Forward Voltage vs. Current

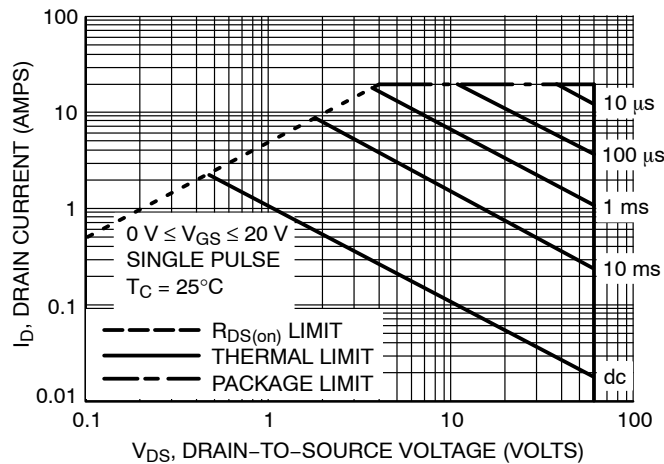


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTGS5120P, NVGS5120P

## TYPICAL CHARACTERISTICS

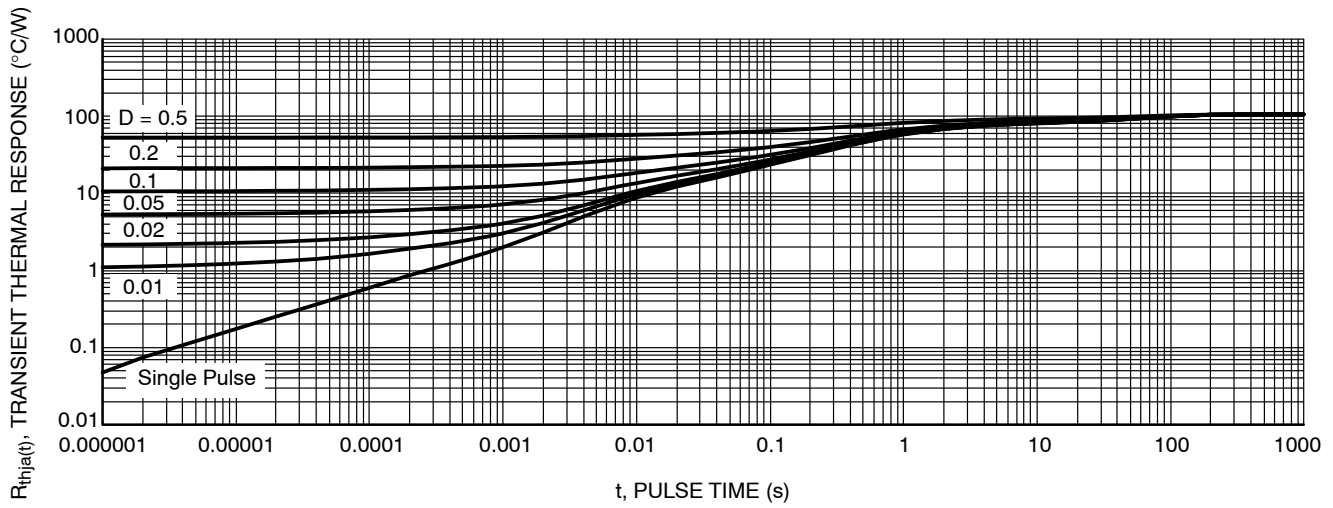


Figure 12. Thermal Response

Table 1. ORDERING INFORMATION

Part Number	Marking (XX)	Package	Shipping <sup>†</sup>
NTGS5120PT1G	P6	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NVGS5120PT1G	VP6	TSOP-6 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

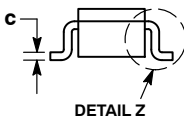
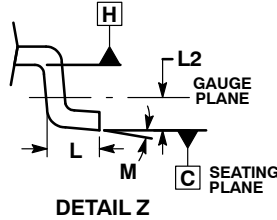
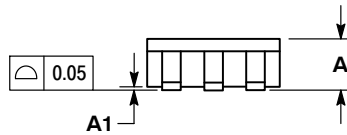
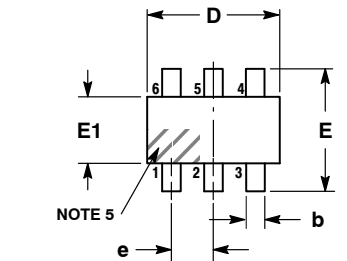
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SCALE 2:1

### TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



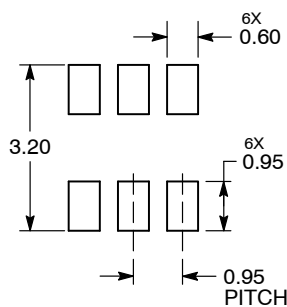
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- |  |  |   |   |   |  |
|--|--|---|---|---|--|
| <p>STYLE 1:<br/>PIN 1. DRAIN<br/>2. DRAIN<br/>3. GATE<br/>4. SOURCE<br/>5. DRAIN<br/>6. DRAIN</p>              | <p>STYLE 2:<br/>PIN 1. EMITTER 2<br/>2. BASE 1<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 2<br/>6. COLLECTOR 2</p>    | <p>STYLE 3:<br/>PIN 1. ENABLE<br/>2. N/C<br/>3. R BOOST<br/>4. Vz<br/>5. V in<br/>6. V out</p>                            | <p>STYLE 4:<br/>PIN 1. N/C<br/>2. V in<br/>3. NOT USED<br/>4. GROUND<br/>5. ENABLE<br/>6. LOAD</p>                | <p>STYLE 5:<br/>PIN 1. EMITTER 2<br/>2. BASE 2<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 1<br/>6. COLLECTOR 2</p> | <p>STYLE 6:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. EMITTER<br/>5. COLLECTOR<br/>6. COLLECTOR</p> |
| <p>STYLE 7:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. N/C<br/>5. COLLECTOR<br/>6. EMITTER</p>   | <p>STYLE 8:<br/>PIN 1. Vbus<br/>2. D(in)<br/>3. D(in)+<br/>4. D(out)+<br/>5. D(out)<br/>6. GND</p>                         | <p>STYLE 9:<br/>PIN 1. LOW VOLTAGE GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN<br/>5. DRAIN<br/>6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:<br/>PIN 1. D(OUT)+<br/>2. GND<br/>3. D(OUT)-<br/>4. D(IN)-<br/>5. VBUS<br/>6. D(IN)+</p>             | <p>STYLE 11:<br/>PIN 1. SOURCE 1<br/>2. DRAIN 2<br/>3. DRAIN 2<br/>4. SOURCE 2<br/>5. GATE 1<br/>6. DRAIN 1/GATE 2</p>  | <p>STYLE 12:<br/>PIN 1. I/O<br/>2. GROUND<br/>3. I/O<br/>4. I/O<br/>5. VCC<br/>6. I/O</p>                          |
| <p>STYLE 13:<br/>PIN 1. GATE 1<br/>2. SOURCE 2<br/>3. GATE 2<br/>4. DRAIN 2<br/>5. SOURCE 1<br/>6. DRAIN 1</p> | <p>STYLE 14:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. CATHODE/DRAIN<br/>5. CATHODE/DRAIN<br/>6. CATHODE/DRAIN</p> | <p>STYLE 15:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. DRAIN<br/>5. N/C<br/>6. CATHODE</p>                        | <p>STYLE 16:<br/>PIN 1. ANODE/CATHODE<br/>2. BASE<br/>3. EMITTER<br/>4. COLLECTOR<br/>5. ANODE<br/>6. CATHODE</p> | <p>STYLE 17:<br/>PIN 1. EMITTER<br/>2. BASE<br/>3. ANODE/CATHODE<br/>4. ANODE<br/>5. CATHODE<br/>6. COLLECTOR</p>       |  |

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM\*



- |  |   |
|--|---|
| <p>XXX = Specific Device Code<br/>A = Assembly Location<br/>Y = Year<br/>W = Work Week<br/>▪ = Pb-Free Package</p> | <p>XXX = Specific Device Code<br/>M = Date Code<br/>▪ = Pb-Free Package</p> |
|--|---|

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	TSOP-6	PAGE 1 OF 1

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