MOSFET – Power, Single, P-Channel, TSOP-6

-30 V, -4.7 A

Features

- Leading -30 V Trench Process for Low R_{DS(on)}
- Low Profile Package Suitable for Portable Applications
- Surface Mount TSOP-6 Package Saves Board Space
- Improved Efficiency for Battery Applications
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Pb-Free Package is Available

Applications

- Battery Management and Switching
- Load Switching
- Battery Protection

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit		
Drain-to-Source Voltage			V_{DSS}	-30	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Cur-	Steady	$T_A = 25^{\circ}C$	I_D	-3.7	Α
rent (Note 1)	State	T _A = 85°C		-2.7	
	t ≤ 5 s	T _A = 25°C		-4.7	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.25	W
	t ≤ 5 s			2.0	
Continuous Drain Cur-	Steady	T _A = 25°C	I _D	-2.6	Α
rent (Note 2)	State	T _A = 85°C		-1.9	
Power Dissipation (Note 2)		T _A = 25°C	P _D	0.63	W
Pulsed Drain Current	tp =	: 10 μs	I_{DM}	-15	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 150	°C
Source Current (Body Diode)			I _S	-1.7	Α
Lead Temperature for Sold (1/8" from case for 10 s)	ering Pur	poses	TL	260	°C

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	100	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	200	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

 Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

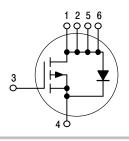


ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
-30 V	38 mΩ @ –10 V	-4.7 A
	68 mΩ @ -4.5 V	,

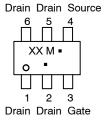
P-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



TSOP-6 CASE 318G STYLE 1



XX = Specific Device Code M = Date Code*

= Pb-Free Package
 (Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information ion page 6 of this data sheet.

2.	. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.006 in sq).				

ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V, } I_{D}$	₀ = -250 μA	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				-17		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -24 V	$T_J = 25^{\circ}C$			-1.0	μΑ
		$V_{DS} = -24 \text{ V}$	T _J = 125°C			-100	1
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V	GS = ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{E}$	_O = -250 μA	-1.0		-3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = -10 \text{ V},$	$I_D = -3.7 \text{ A}$		38	60	mΩ
		V _{GS} = -4.5 V,	, I _D = -2.7 A		68	110	
Forward Transconductance	9FS	$V_{DS} = -10 \text{ V},$	$I_D = -3.7 \text{ A}$		6.0		S
CHARGES, CAPACITANCES AND GATE RE	SISTANCE						
Input Capacitance	C _{ISS}				750		pF
Output Capacitance	C _{OSS}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = -15 \text{ V}$			140		7
Reverse Transfer Capacitance	C _{RSS}				105		1
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = -10 \text{ V}, V_{DD} = -15 \text{ V},$ $I_{D} = -3.7 \text{ A}$			15.25	32	nC
Threshold Gate Charge	Q _{G(TH)}				0.8		1
Gate-to-Source Charge	Q _{GS}				2.6		1
Gate-to-Drain Charge	Q_{GD}				3.4		1
SWITCHING CHARACTERISTICS, VGS = -1	0 V (Note 4)					•	
Turn-On Delay Time	t _{d(ON)}				9.0	17	ns
Rise Time	t _r	V _{GS} = -10 V. \	/nn = -15 V.		9.0	18	1
Turn-Off Delay Time	t _{d(OFF)}	$V_{GS} = -10 \text{ V, V}$ $I_D = -1.0 \text{ A, V}$	$R_G = 6.0 \Omega$		38	85	1
Fall Time	t _f				22	45	
SWITCHING CHARACTERISTICS, VGS = -4	I.5 V (Note 4)	<u> </u>				1	
Turn-On Delay Time	t _{d(ON)}				11	20	ns
Rise Time	t _r	V _G = -4.5 V. V	V _{DD} = -15 V.		15	28	1
Turn-Off Delay Time	t _{d(OFF)}	$V_{GS} = -4.5 \text{ V}, V_{DD} = -15 \text{ V},$ $I_{D} = -1.0 \text{ A}, R_{G} = 6.0 \Omega$			28	56	1
Fall Time	t _f				22	50	1
DRAIN - SOURCE DIODE CHARACTERIST	ics						
Characteristic	Symbol	Test Cor	ndition	Min	Τνp	Max	Unit

Characteristic	Symbol	Test Cor	ndition	Min	Тур	Max	Unit
Forward Diode Voltage	V _{DS}	V _{GS} = 0 V,	T _J = 25°C		-0.76	-1.2	V
		$V_{GS} = 0 \text{ V},$ $I_{S} = -1.0 \text{ A}$	T _J = 125°C		-0.60		1
Reverse Recovery Time	t _{RR}				17	40	ns
Charge Time	t _a	V _{GS} =	0 V		9.0		
Discharge Time	t _b	$V_{GS} = dI_S/dt = 100 A/\mu$	s, $I_S = -1.0 \text{ A}$		8.0		
Reverse Recovery Charge	Q _{RR}				8.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

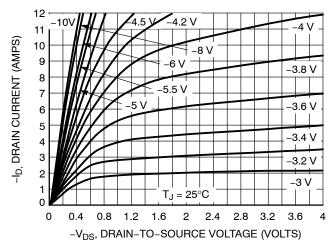
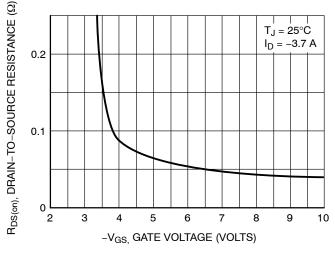


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



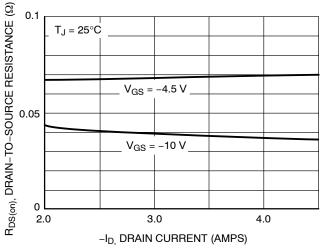
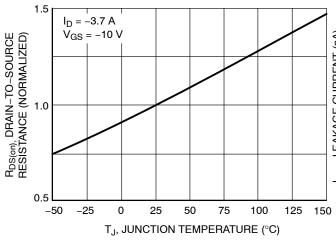


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



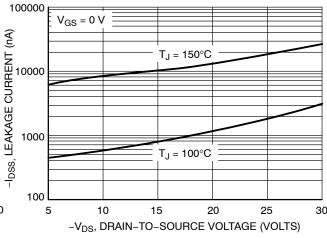
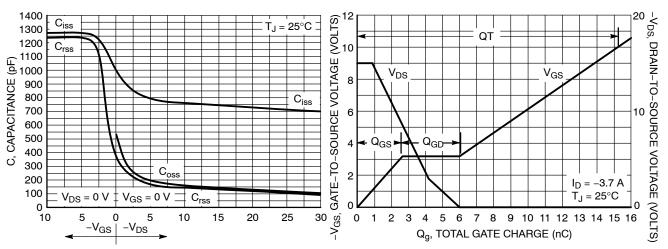


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)



-GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source Voltage vs. Total **Gate Charge**

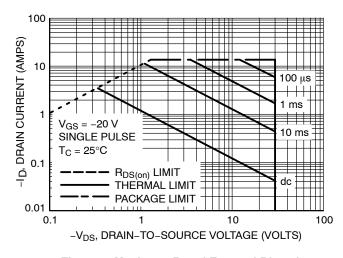


Figure 9. Maximum Rated Forward Biased Safe Operating Area

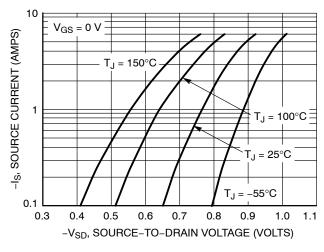


Figure 10. Diode Forward Voltage vs. Current

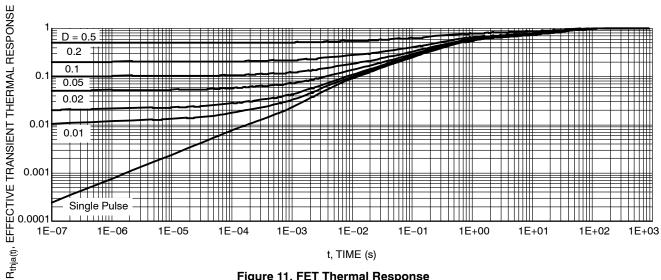


Table 1. ORDERING INFORMATION

Part Number	Marking (XX)	Package	Shipping [†]
NTGS4111PT1	TG	SC-88	3000 / Tape & Reel
NTGS4111PT1G	TG	SC-88 (Pb-Free)	3000 / Tape & Reel
NVGS4111PT1G	VTG	SC-88 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Δ1

STYLE 13: PIN 1. GATE 1

2. SOURCE 2

3. GATE 2

4. DRAIN 2

5. SOURCE 1

DRAIN 1

TSOP-6 CASE 318G-02 **ISSUE V**

12

C SEATING PLANE

DATE 12 JUN 2012

STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR

3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR

2. GROUND 3. I/O 4. I/O 5. VCC 6. I/O

STYLE 12:



- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D
- AND E1 ARE DETERMINED AT DATUM H.
 PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

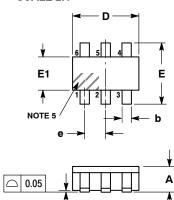
	MILLIMETERS				
DIM	MIN	NOM	MAX		
Α	0.90	1.00	1.10		
A1	0.01	0.06	0.10		
b	0.25	0.38	0.50		
С	0.10	0.18	0.26		
D	2.90	3.00	3.10		
E	2.50	2.75	3.00		
E1	1.30	1.50	1.70		
е	0.85	0.95	1.05		
Ĺ	0.20	0.40	0.60		
L2	0.25 BSC				
М	Uo.		100		

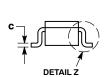
STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1

STYLE 11:

BASE 1 6. COLLECTOR 2

PIN 1. SOURCE 1





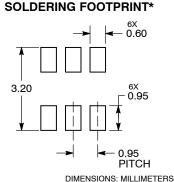
DETAIL Z

Н

STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2	STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. VZ 5. V in 6. V out	STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD
STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER	STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND	STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE	STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+

. D(in)	2. DRAIN	2. GND	2. DRAIN 2
. D(in)+	SOURCE	D(OUT)-	3. DRAIN 2
. D(oút)+	4. DRAIN	4. D(IN)-	4. SOURCE 2
. D(out)	5. DRAIN	5. VBUS	5. GATE 1
. GND ´	HIGH VOLTAGE G	GATE 6. D(IN)+	DRAIN 1/GATE 2
14:	STYLE 15:	STYLE 16:	STYLE 17:
. ANODE	PIN 1. ANODE	PIN 1. ANODE/CATHODE	PIN 1. EMITTER
. SOURCE	2. SOURCE	2. BASE	2. BASE
. GATE	3. GATE	EMITTER	ANODE/CATHODE
. CATHODE/DRAIN	4. DRAIN	4. COLLECTOR	4. ANODE
. CATHODE/DRAIN	5. N/C	5. ANODE	CATHODE
. CATHODE/DRAIN	CATHODE	CATHODE	COLLECTOR

GENERIC MARKING DIAGRAM*



STYLE 14: PIN 1. ANODE

5.

3 GATE

RECOMMENDED

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.





XXX = Specific Device Code

Α =Assembly Location Υ = Year

W = Work Week = Pb-Free Package XXX = Specific Device Code M = Date Code

= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ", may or may not be present.

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DESCRIPTION:	TSOP-6		PAGE 1 OF 1	

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