FAN53880

One Buck, One Boost and Four LDO PMIC

ON Semiconductor®

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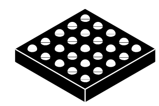
General Description

The FAN53880 is a low quiescent current PMIC for mobile power applications. The PMIC contains one buck, one boost, and four low noise LDOs.

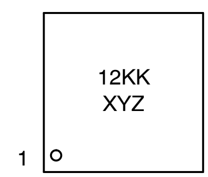
The buck and boost converters can operate within a wide supply range of 2.5 V to 5.5 V. At moderate and light loads, Pulse Frequency Modulation (PFM) reduces current consumption while maintaining excellent transient response during load swings. At higher loads, the converters automatically switch to Pulse Width Modulation (PWM) control.

The FAN53880 is available in a 25−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).



WLCSP25
CASE 567QT

MARKING DIAGRAM



12	= Alphanumeric Device Marking
KK	= Lot Run Code
X	= Alphabetical Year Code
Y	= 2−weeks Date Code
Z	= Assembly Plant Code

Features

- Programmable Start−Up/Down Sequencing
- Programmable Output Voltages
- Soft−Start (SS) Inrush Current Limiting
- Fault Protection with Interrupt Reporting
  - UVLO, OCP, OVP, UVP and OTP
- Low Current Standby and Shutdown Modes
- Buck Converter:
  - Input Voltage Range: 2.5 V to 5.5 V
  - Digitally Programmable Voltage Range: 0.6 V to 3.3 V
  - 1200 mA Output Current Capability
  - 95% Efficiency
- Boost Converter:
  - Input Voltage Range: 2.5 V to 5.5 V
  - Digitally Programmable Voltage Range: 3.0 V to 5.7 V
  - 1000 mA Output Current Capability
  - 95% Efficiency
- Four LDOs:
  - Input Voltage Range: 1.9 V to 5.5 V
  - Digitally Programmable Voltage Range: 0.8 V to 3.3 V
  - 300 mA Output Current Capability

Applications

- Smartphones and Tablets
- Compact Camera Modules
- USB On−The−Go

Application Diagram

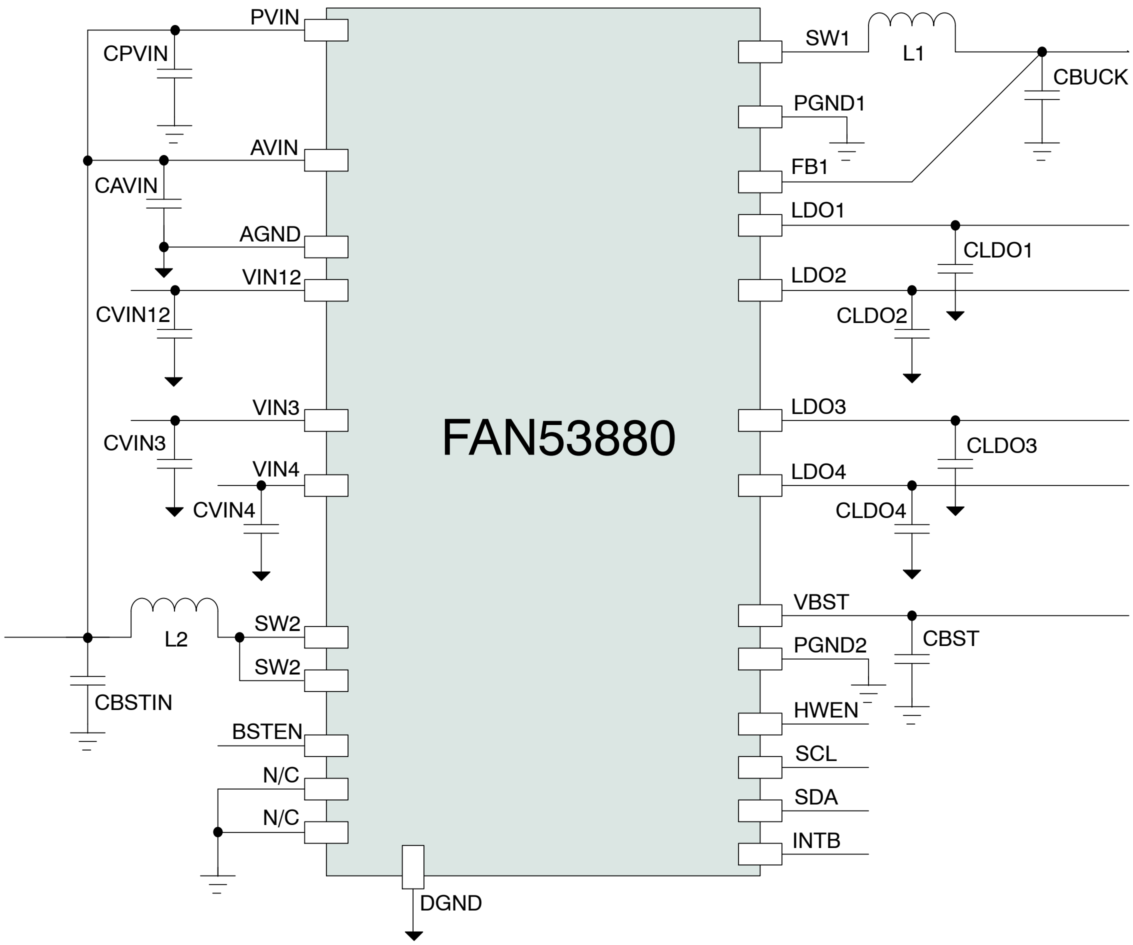


Figure 1. Application Diagram

PART NUMBERING

Table 1. ORDERING INFORMATION

Part Number	Buck V_{OUT}	LDO1,2 V_{OUT}	LDO3,4 V_{OUT}	Boost V_{OUT}	I2C Address	Temperature Range	Package	Packing Method	Device Marking
FAN53880UC001X*	1.1 V	2.8 V	1.8 V	5.0 V	7'h35	−40°C to 85°C	25−Bump WLCSP	Tape and Reel†	LT
FAN53880UC002X	1.1 V	2.8 V	1.8 V	5.0 V	7'h35	−40°C to 85°C	25−Bump WLCSP	Tape and Reel†	LW

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
*Not recommended for new designs.

PRODUCT PIN ASSIGNMENTS

Pin Configuration

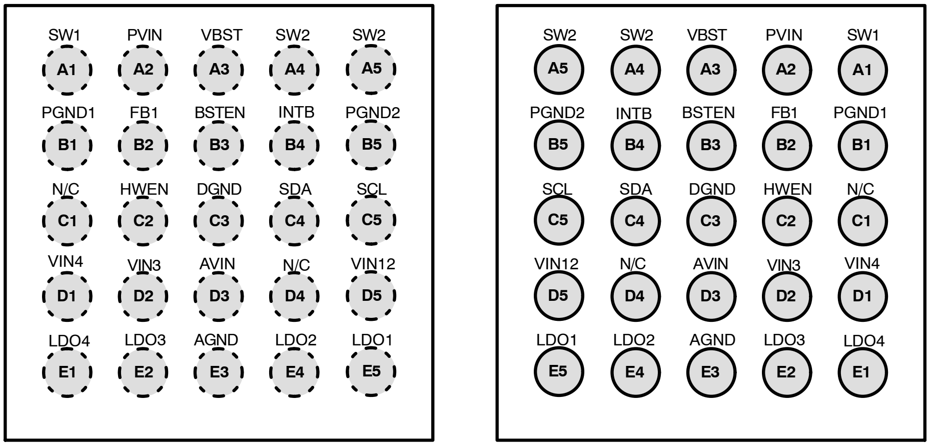


Figure 2. Pin Configuration

Pin Descriptions

Table 2. PIN DEFINITION

Pin	Pin Name	Description
A1	SW1	Switching node of the buck converter. Tie one lead of the inductor to this pin.
A2	PVIN	Input power for the buck and boost converter. Bypass this pin with C_{PVIN} close to the device pin. The voltage must be kept within 25 mV of AV_{IN}.
A3	VBST	Boost output node. Locate C_{BST} close to this pin
A4, A5	SW2	Switching node for the boost converter.
B1	PGND1	Power ground connection for the buck converter. Connect directly to ground plane.
B2	FB1	Feedback pin for the buck converter. Connect to C_{BUCK} and keep trace away from noisy circuitry.
B3	BSTEN	Enables the boost and critical circuits associated with the boost operation when asserted high. The BSTEN pin has an internal 2.8 MΩ pull−down and should always be connected to a logic high or low. Note: HWEN does not need to be high for Boost operation when BSTEN is high.
B4	INTB	I2C interrupt pin is active low indicating that an interrupt event has occurred.
B5	PGND2	Power ground connection for the Boost converter. Connect directly to ground plane.
C1	N/C	This pin is a no−connect within the device. It is recommended to tie this pin to ground, but is not necessary.
C2	HWEN	HWEN pin is used to enable basic circuits necessary for controlling the power converter outputs. The HWEN pin has an internal 5 MΩ pull−down and should always be connected to a logic high or low.
C3	DGND	Digital/Analog ground connection. Tie to inner layer power plane through via.
C4	SDA	I2C Data pin. Node should be tied high through a pull up resistor.
C5	SCL	I2C Clock pin. Node should be tied high through a pull up resistor.
D1	VIN4	Input power pin for LDO4. Place C_{VIN4} as close to this pin as possible.
D2	VIN3	Input power pin for LDO3. Place C_{VIN3} as close to this pin as possible.
D3	AVIN	Analog power pin. Route trace from battery side of the boost inductor (L2) to the AV_{IN} pin. Connect the C_{AVIN} capacitor as close as possible to the pin. To create a low pass filter, a series resistor may be added between the inductor and C_{AVIN}. The voltage must be kept within 25 mV of PV_{IN} to ensure system stability.
D4	N/C	This pin is a no−connect within the device. It is recommended to tie this pin to ground, but is not necessary.
D5	VIN12	This is the input power pin for LDO1 and LDO2. Place C_{VIN12} as close to this pin as possible.
E1	LDO4	This is the output pin for LDO4. Place C_{LDO4} as close to this pin as possible.
E2	LDO3	This is the output pin for LDO3. Place C_{LDO3} as close to this pin as possible.
E3	AGND	Analog ground is the analog circuitry ground. Tie this pin to the analog ground plane.
E4	LDO2	This is the output pin for LDO2. Place C_{LDO2} as close to this pin as possible.
E5	LDO1	This is the output pin for LDO1. Place C_{LDO1} as close to this pin as possible.

PRODUCT BLOCK DIAGRAM

Block Diagram

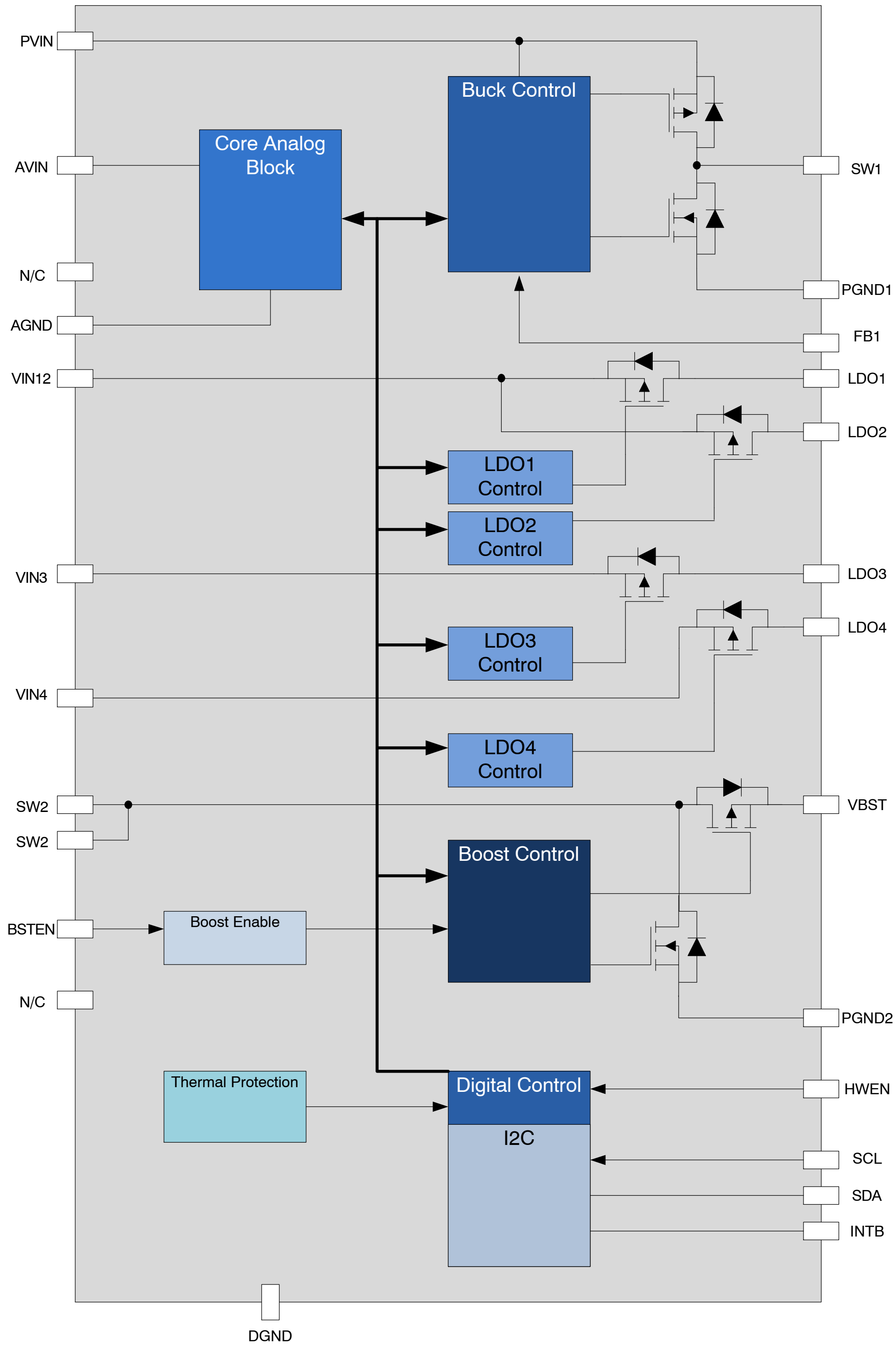


Figure 3. Block Diagram

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage	AV_{IN}, PV_{IN}, V_{IN12}, V_{IN3} and V_{IN4}	−0.3		(Note 1)	V
V_{SW1}	Voltage on SW1 Pin		−0.3		(Note 1)	V
V_{SW2}	Voltage on SW2 Pin		−0.3		(Note 1)	V
V_{CTRL}	SDA and SCL Pins		− 0.3		(Note 1)	V
V_{INTB}	INTB Pins		− 0.3		AV_{IN}	V
	other Pins		− 0.3		(Note 1)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model		2.0		kV
		Charged Device Model		500		V
T_J	Junction Temperature		−40		+150	°C
T_{STG}	Storage Temp		−40		+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Lesser of 6 V or AV_{IN} + 0.3 V.

Table 4. THERMAL PROPERTIES

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	58	°C/W

NOTE: Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with two−layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AP_{VIN}	Supply Voltage Range	AV_{IN}, PV_{IN}	2.5		5.5	V
V_{IN12}		V_{IN12}	2.5		5.5	V
V_{IN3}		V_{IN3}	1.9		5.5	V
V_{IN4}		V_{IN4}	1.9		5.5	V
P_D	Power Dissipation	PD = (125°C − 85°C) / 58°C/W = 0.69 W			0.69	W
T_A	Operating Ambient Temperature		−40		85	°C
T_J	Junction Temperature		−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at AV_{IN} = PV_{IN} = 2.5 V to 5.5 V & PV_{IN} > V_{BUCK} + 350 mV and PV_{IN} < V_{BST} − 250 mV, V_{IN12} = 2.5 V to 5.5 V & V_{IN} > $V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, V_{IN4} > $V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, AV_{IN}, PV_{IN}, V_{IN12} = 3.8 V, V_{IN3}, V_{IN4} = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, V_{LDO1} and V_{LDO2} = 2.8 V, V_{LDO3} and V_{LDO4} = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLIES UVLO						
$V_{VIN\ UVLO\_RISE}$	Under−Voltage Lockout Threshold	Rising AV_{IN} or V_{IN12}	2.30	2.35	2.45	V
$V_{VIN\ UVLO\_FALL}$		Falling AV_{IN} or V_{IN12}	2.15	2.25	2.30	V
$V_{VIN3/4\ UVLO\_RISE}$		Rising V_{IN3} and V_{IN4}	1.80	1.85	1.95	V
$V_{VIN3/4\ UVLO\_FALL}$		Falling V_{IN3} and V_{IN4}	1.70	1.75	1.80	V
BUCK EC						
POWER SUPPLIES						
IQ_{BK_PFM}	PFM Quiescent Current	Total current on PV_{IN} and AV_{IN} when AV_{IN} = PV_{IN} = VHWEN, BUCK_EN bit = 1, PFM Mode, Non Switching, No Load, all other converters disabled.		36		μA
R_{BK_DIS}	Output Discharge Resistance		80	100	120	Ω
PFM ↔ PWM THRESHOLDS						
I_{BK_PFM}	I_{OUT} where part transitions into PFM			50		mA
I_{BK_PWM}	I_{OUT} value where part transitions into PWM			120		mA
BUCK V_{OUT} ACCURACY						
VO_{BK_ACC}	PFM Output Voltage Accuracy	V_{OUT} = 0.6 V, AV_{IN} = PV_{IN} = 3.8 V, PFM Mode, I_{OUT} = 0 A	−3		3	%
		AV_{IN} = PV_{IN} = 3.8 V, No Load, PFM Mode, V_{OUT} = 1.0125 V to 3.3 V	−2		2	%
	PWM Output Voltage Accuracy	V_{OUT} = 0.6 V, AV_{IN} = PV_{IN} = 3.8 V, PWM Mode, I_{OUT} = 0 A	−3		3	%
		AV_{IN} = PV_{IN} = 3.8V, No Load, PWM Mode, V_{OUT} = 1.0125 V to 3.3 V	−2		2	%
CURRENT LIMIT						
$ILIM_{BK}$	Peak Inductor Current Limit	Programmed to support 1.2 A DC load	1600	1900	2200	mA
REGULATOR						
F_{BK_SW}	Switching Frequency	PWM, I_{OUT} = 0 A, AV_{IN} = PV_{IN} = 3.8 V, V_{OUT} = 1.1 V	2.25	2.5	2.75	MHz
$RDS_{ON\ BK\_P}$	PMOS Resistance Ball−to−Ball	AP_{VIN} = V_{GS} = 3.8 V, Temp = 25°C		0.125	0.200	Ω
$RDS_{ON\ BK\_N}$	NMOS Resistance Ball−to−Ball	AP_{VIN} = V_{GS} = 3.8 V, Temp = 25°C		0.085	0.140	Ω
VO_{BK_RNG}	Buck Output Voltage Range	When V_{OUT} + 300 mV < AV_{IN} & PV_{IN}	0.6	1.1	3.3	V
BUCK OUTPUT PROTECTION						
OVP_{BK_RS}	Rising Over Voltage Output Threshold	V_{IN} = 3.8 V, V_{OUT} = 1.1 V, V_{OUT} = 2.85 V	Vtarget x 1.17	Vtarget x 1.2	Vtarget x 1.23	V
		V_{OUT} = 0.6 V	Vtarget x 1.15	Vtarget x 1.2	Vtarget x 1.25	V
OVP_{BK_FL}	Falling Over Voltage Output Threshold	V_{OUT} = 0.6 V to 3.300V	Vtarget x 1.04	Vtarget x 1.10	Vtarget x 1.14	V
UVP_{BK_FL}	Falling Under Voltage Output Threshold	V_{OUT} = 0.6 V	Vtarget x 0.83	Vtarget x 0.90	Vtarget x 0.97	V
		V_{IN} = 3.8 V, V_{OUT} = 1.1 V, 2.85 V	Vtarget x 0.86	Vtarget x 0.90	Vtarget x 0.93	V
UVP_{BK_RS}	Rising Under Voltage Output Threshold	V_{OUT} = 0.6 V to 3.3 V	Vtarget x 0.90	Vtarget x 0.95	Vtarget x 0.99	V

Table 6. ELECTRICAL CHARACTERISTICS (continued)
Minimum and maximum values are at AV_{IN} = PV_{IN} = 2.5 V to 5.5 V & PV_{IN} > V_{BUCK} + 350 mV and PV_{IN} < V_{BST} − 250 mV, V_{IN12} = 2.5 V to 5.5 V & V_{IN} > $V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, V_{IN4} > $V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, AV_{IN}, PV_{IN}, V_{IN12} = 3.8 V, V_{IN3}, V_{IN4} = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, V_{LDO1} and V_{LDO2} = 2.8 V, V_{LDO3} and V_{LDO4} = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OVP_{BK_TMR}	Over Voltage Output Protection Timer	V_{OUT_Target} = 2.85 V, V_{OUT} held at 3.65 V, INTB going high trigger	32	40	56	µs
UVP_{BK_TMR}	Under Voltage Output Protection Timer	V_{OUT_Target} = 2.85 V, V_{OUT} held at 2.05 V, Time to Output Disabled	32	40	56	µs
BOOST EC						
POWER SUPPLIES						
IQ_{BST_PFM}	Quiescent Current	Total current on PV_{IN} and AV_{IN}, V_{OUT} = 5 V when V_{BSTEN} = AV_{IN}, VHWEN = 0, PFM Mode, Non Switching, No Load, all other converters disabled.		32	44	µA
$IQ_{BST\ PT}$	IQ in Auto Pass−Thru Mode	Total current on PV_{IN} and AV_{IN} when V_{BSTEN} = AV_{IN}, VHWEN = 0, No Load, all other converters disabled.		39	90	µA
IQ_{BST_FPT}	IQ when part is in Forced Pass−Thru Mode	Total current on PV_{IN} and AV_{IN} when AV_{IN} = PV_{IN} = V_{BSTEN} = 3.8 V, VHWEN = 0, BST_MODE bit = 1, No Load, all other converters disabled.		18		µA
R_{BST_DCHG}	Output Discharge Resistance		80	100	120	Ω
PFM ↔ PWM THRESHOLDS						
I_{BST_PFM}	PFM Mode I_{OUT} Threshold			100		mA
I_{BST_PWM}	PWM Mode I_{OUT} Threshold			130		mA
BOOST V_{OUT} ACCURACY						
VO_{BST_ACC}	PFM Output Voltage Accuracy	V_{IN} = 3.8 V, No Load, PFM Mode	−3		3	%
	PWM Output Voltage Accuracy	V_{IN} = 3.8 V, No Load, PWM Mode	−3		3	%
CURRENT LIMIT						
I_{LIMBST}	Peak Inductor Current Limit	Programmed to support 1 A DC load	3.0	3.5	4.0	A
REGULATOR						
F_{SW_BST}	PWM Switching Frequency	V_{IN} = 3.8 V	2.25	2.5	2.75	MHz
$RDS_{ON\ BST\_P}$	PMOS Resistance Ball−to−Ball	Temp = 25°C		65	120	mΩ
$RDS_{ON\ BST\_N}$	NMOS Resistance Ball−to−Ball	Temp = 25°C		50	100	mΩ
VO_{BST_RNG}	Boost Output Voltage Range	When PV_{IN} < V_{BST} and 2.5 V ≤ PV_{IN}/AV_{IN} ≤ 5.5 V	3.0	5.0	5.7	V
BOOST OUTPUT PROTECTION						
OVP_{BST_RS}	Rising Over Voltage Output Threshold	V_{AVIN} = 3.8 V, V_{OUT} = 5.0 V	Vtarget x 1.16	Vtarget x 1.2	Vtarget x 1.22	V
OVP_{BST_FL}	Falling Over Voltage Output Threshold		Vtarget x 1.07	Vtarget x 1.1	Vtarget x 1.12	V
UVP_{BST_FL}	Falling Under Voltage Output Threshold	V_{AVIN} = 3.8 V, V_{OUT} = 5.0 V	Vtarget x 0.78	Vtarget x 0.80	Vtarget x 0.82	V
UVP_{BST_RS}	Rising Under Voltage Output Threshold		Vtarget x 0.88	Vtarget x 0.90	Vtarget x 0.93	V
OVP_{BST_TMR}	Over Voltage Output Protection Timer	V_{OUT_Target} = 5.0 V, V_{OUT} held at 6.25 V, INTB going high trigger	32	40	56	µs
UVP_{BST_TMR}	Under Voltage Output Protection Timer	V_{OUT_Target} = 5.0 V, V_{OUT} held at 4.00 V, Time to Output Disabled	32	40	56	µs

Table 6. ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at $AV_{IN} = PV_{IN}$ = 2.5 V to 5.5 V & $PV_{IN} > V_{BUCK}$ + 350 mV and $PV_{IN} < V_{BST}$ − 250 mV, V_{IN12} = 2.5 V to 5.5 V & $V_{IN} > V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, $V_{IN4} > V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, AV_{IN}, PV_{IN}, V_{IN12} = 3.8 V, V_{IN3}, V_{IN4} = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, V_{LDO1} and V_{LDO2} = 2.8 V, V_{LDO3} and V_{LDO4} = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LDO1/2 EC SPECS						
QUIESCENT CURRENT						
IQ_{L12}	Quiescent Current, No Load	I_{OUT} = 0 A, Combined Current Measured at AV_{IN} and V_{IN12} when LDO1 is enabled only or LDO2 is enabled only, Buck and Boost are disabled, VHWEN = AV_{IN}		40	55	μA
VO_{L12_RNG}	LDO Output Voltage Range	When V_{OUT} + 300 mV < V_{IN12} and 2.5 V ≤ V_{IN12} ≤ 5.5 V	0.8	2.8	3.3	V
VO_{L12_ACC}	Output Voltage Accuracy	I_{OUT} = 300 mA, $AV_{IN} = V_{IN12}$ = 3.8 V, V_{OUT} = 0.8 V to 3.3 V	−2.0		+2.0	%
V_{L12_DO}	Dropout Voltage	$V_{OUT} = V_{OUT\_TARGET}$ − 100 mV, I_{OUT} = 300 mA, V_{OUT_TARGET} = 2.8 V			250	mV
IO_{MAX_L12}	Max load current	V_{OUT} + 0.3 V < V_{IN12} and V_{IN12} = 2.5 V to 4.5 V	300			mA
CURRENT LIMIT						
I_{LIM_L12}	Current Limit	V_{OUT} + 500 mV < V_{IN12} and 2.5 V ≤ V_{IN12} ≤ 4.5 V	150	180	210	mA
		V_{OUT} + 500 mV < V_{IN12} and 2.5 V ≤ V_{IN12} ≤ 4.5 V	360	420	480	mA
OUTPUT PROTECTION						
OVP_{L12_RS}	Rising Over Voltage Output Threshold	$V_{AVIN} = V_{IN1/2}$ = 3.8 V, V_{OUT} = 2.8 V	Vtarget x 1.17	Vtarget x 1.2	Vtarget x 1.23	V
OVP_{L12_FL}	Falling Over Voltage Output Threshold	$V_{AVIN} = V_{IN1/2}$ = 3.8 V, V_{OUT} = 2.8 V	Vtarget x 1.07	Vtarget x 1.1	Vtarget x 1.12	V
UVP_{L12_FL}	Falling Under Voltage Output Threshold	$V_{AVIN} = V_{IN1/2}$ = 3.8 V, V_{OUT} = 2.8 V	Vtarget x 0.77	Vtarget x 0.8	Vtarget x 0.82	V
UVP_{L12_HS}	Rising Under Voltage Output Threshold	$V_{AVIN} = V_{IN1/2}$ = 3.8 V, V_{OUT} = 2.8 V	Vtarget x 0.88	Vtarget x 0.9	Vtarget x 0.93	V
OVP_{L12_TMR}	Over Voltage Output Protection Timer	V_{OUT_Target} = 2.8 V, V_{OUT} held at 3.5 V, INTB going high trigger	32	40	56	μs
UVP_{L12_TMR}	Under Voltage Output Protection Timer	V_{OUT_Target} = 2.8 V, V_{OUT} held at 1.8 V, Time to Output Disabled	32	40	56	μs
R_{L12_DCHG}	Output Discharge Resistance		80	100	120	Ω
LDO3/4 EC SPECS						
QUIESCENT CURRENT						
IQ_{L34}	Quiescent Current, No Load	I_{OUT} = 0 A, Combined Current Measured at AV_{IN} and V_{IN3} when LDO3 is enabled or AV_{IN} and V_{IN4} when LDO4 is enabled. LDO1, LDO2, Buck and Boost are disabled, VHWEN = AV_{IN}		38	50	μA
VO_{L34_RNG}	LDO3/4 Output Voltage Range	LDO3: V_{OUT} + 0.15 < V_{IN3} and V_{IN3} = 1.95 V to 4.5 V, LDO4: V_{OUT} + 150 mV < V_{IN4} and V_{IN4} = 1.95 V to 4.5 V	0.8	1.8	3.3	V
VO_{L34_ACC}	Output Voltage Accuracy	I_{OUT} = 300 mA, AV_{IN} = 3.8 V, $V_{IN3/4}$ = 3.8 V, V_{OUT} = 0.8 V to 3.3 V	−2.5		+2.0	%
V_{L34_DO}	Dropout Voltage	$V_{OUT} = V_{OUT\_TARGET}$ − 100 mV, I_{OUT} = 300 mA, V_{OUT_TARGET} = 1.8 V			150	mV
IO_{MAX_L34}	Max load current	V_{OUT} + 150 mV < V_{IN3} and V_{IN3} = 1.95 V to 4.5 V, LDO4: V_{OUT} + 150 mV < V_{IN4} and V_{IN4} = 1.95 V to 4.5 V	300			mA

Table 6. ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at AV_{IN} = PV_{IN} = 2.5 V to 5.5 V & PV_{IN} > V_{BUCK} + 350 mV and PV_{IN} < V_{BST} − 250 mV, V_{IN12} = 2.5 V to 5.5 V & V_{IN} > $V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, V_{IN4} > $V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, AV_{IN}, PV_{IN}, V_{IN12} = 3.8 V, V_{IN3}, V_{IN4} = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, V_{LDO1} and V_{LDO2} = 2.8 V, V_{LDO3} and V_{LDO4} = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CURRENT LIMIT						
I_{LIM_L34}	Current Limit	V_{OUT} + 500 mV < V_{IN3} and V_{IN3} = 1.95 V to 4.5 V, LDO4: V_{OUT} + 500 mV < V_{IN4} and V_{IN4} = 1.95 V to 4.5 V	150	180	210	mA
		V_{OUT} + 500 mV < V_{IN3} and V_{IN3} = 1.95 V to 4.5 V, LDO4: V_{OUT} + 500 mV < V_{IN4} and V_{IN4} = 1.95 V to 4.5 V	360	420	480	mA
R_{L34_DCHG}	Output Discharge Resistance		80	100	120	Ω
OUTPUT PROTECTION						
OVP_{L34_RS}	Rising Over Voltage Output Threshold	V_{AVIN} = 3.8 V, $V_{IN3/4}$ = 1.95V, V_{OUT} = 1.8 V	Vtarget x 1.17	Vtarget x 1.2	Vtarget x 1.23	V
OVP_{L34_FL}	Falling Over Voltage Output Threshold	V_{AVIN} = 3.8 V, $V_{IN3/4}$ = 1.95V, V_{OUT} = 1.8 V	Vtarget x 1.07	Vtarget x 1.1	Vtarget x 1.12	V
UVP_{L34_FL}	Falling Under Voltage Output Threshold	V_{AVIN} = 3.8 V, $V_{IN3/4}$ = 1.95V, V_{OUT} = 1.8 V	Vtarget x 0.77	Vtarget x 0.80	Vtarget x 0.82	V
UVP_{L34_RS}	Rising Under Voltage Output Threshold	V_{AVIN} = 3.8 V, $V_{IN3/4}$ = 1.95V, V_{OUT} = 1.8 V	Vtarget x 0.88	Vtarget x 0.90	Vtarget x 0.93	V
OVP_{L34_TMR}	Over Voltage Output Protection Timer	V_{OUT_Target} = 1.8 V, V_{OUT} held at 2.25 V, INTB going high trigger	32	40	56	μs
UVP_{L34_TMR}	Under Voltage Output Protection Timer	V_{OUT_Target} = 1.8 V, V_{OUT} held at 1.35 V, Time to Output Disabled	32	40	56	μs
I/O LEVELS						
V_{IL}	HWEN Logic Low threshold				0.35	V
V_{IH}	HWEN Logic High threshold		1.2		V_{IN}	V
V_{IL}	BSTEN Logic Low threshold				0.25	V
V_{IH}	BSTEN Logic High threshold	AV_{IN} = 4.5 V;	1.05		V_{IN}	V
R_{PD}	HWEN and BSTEN Input Resistance	V_{IN} = High or Low	1	4.4		MΩ
V_{OL_INTB}	INTB	Isink = 5 mA			0.3	V
I_{INTB}		V_{INTB} = 5.5 V			0.5	μA
IQ CONDITIONS						
$I_{Q\ AVIN\_SD}$	Shutdown Supply Current	Total current on AV_{IN} when AV_{IN} = 5.0 V and all xxx_EN bits = 0, xxx_SEQ bits =000, HWEN = BSTEN = SDA = SCL = Low			5	μA
$I_{Q\ PVIN\_SD}$		Total current on PV_{IN} when PV_{IN} = 5.0 V and all xxx_EN bits = 0, xxx_SEQ bits =000, HWEN = BSTEN = SDA = SCL = Low			1.5	μA
$I_{Q\ VIN12\_SD}$		Total current on V_{IN12} when V_{IN12} = 5.0 V and all xxx_EN bits = 0, xxx_SEQ bits =000, HWEN = BSTEN = SDA = SCL = Low			1.5	μA
$I_{Q\ VIN3\_SD}$		Total current on V_{IN3} when V_{IN3} = 5.0 V and all xxx_EN bits = 0, xxx_SEQ bits =000, HWEN = BSTEN = SDA = SCL = Low			1.5	μA
$I_{Q\ VIN4\_SD}$		Total current on V_{IN4} when V_{IN4} = 5.0 V and all xxx_EN bits = 0, xxx_SEQ bits =000, HWEN = BSTEN = SDA = SCL = Low			1.5	μA

Table 6. ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at $AV_{IN} = PV_{IN}$ = 2.5 V to 5.5 V & $PV_{IN} > V_{BUCK}$ + 350 mV and $PV_{IN} < V_{BST}$ − 250 mV, V_{IN12} = 2.5 V to 5.5 V & $V_{IN} > V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, $V_{IN4} > V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, AV_{IN}, PV_{IN}, V_{IN12} = 3.8 V, V_{IN3}, V_{IN4} = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, V_{LDO1} and V_{LDO2} = 2.8 V, V_{LDO3} and V_{LDO4} = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{Q_STBY}	Standby Supply Current	Total current on PV_{IN}, AV_{IN}, V_{IN12}, V_{IN3} and V_{IN4} when = 5.0 V and all xxx_EN bits = 1 (Except BST_EN), xxx_SEQ bits =000, $AV_{IN} = PV_{IN}$ = VHWEN = V_{BSTEN}. LDO1−4 on, Buck on, Boost on		165	190	μA
I_{SLP}	Sleep Supply Current	Total current on PV_{IN}, AV_{IN}, V_{IN12}, V_{IN3} and V_{IN4} when = 5.0 V and all xxx_EN bits = 0, xxx_SEQ bits =000, $AV_{IN} = PV_{IN}$ = VHWEN, BSTEN = Low. LDO1−4 off, Buck off, Boost off, No I2C activity		12	20	μA
I²C Timing and Performance†						
V_{IL}	SDA and SCL Logic Low threshold		−0.5		0.4	V
V_{IH}	SDA and SCL Logic High threshold		1.2		5.5	V
V_{OL}	SDA Logic Low Output	3 mA Sink			0.4	V
I_{OL}	SDA Sink Current		20			mA
fSCL	SCL Clock Frequency	Fast Mode Plus			1000	kHz
tBUF	Bus−Free Time Between STOP and START Conditions	Fast Mode Plus	0.5			μs
tHD;STA	START or Repeated START Hold Time	Fast Mode Plus	260			ns
tLOW	SCL LOW Period	Fast Mode Plus	0.5			μs
tHIGH	SCL HIGH Period	Fast Mode−Plus	260			ns
tSU;STA	Repeated START Setup Time	Fast Mode−Plus	260			ns
tHD;DAT	Data Hold Time	Fast Mode Plus	0			ns
tSU;DAT	Data Setup Time	Fast Mode Plus	50			ns
tVD;DAT	Data Valid Time	Fast Mode Plus			450	ns
tVD;ACK	Data Valid Acknowledge Time	Fast Mode Plus			450	ns
tR	SDA and SCL Rise Time	Fast Mode Plus			120	ns
tF	SDA and SCL Fall Time	Fast Mode Plus, VDD = 1.8 V	6.55		120	ns
tSU;STO	Stop Condition Setup Time	Fast Mode Plus	260			ns
Ci	SDA and SCL Input Capacitance				10	pF
Cb	Capacitive Load for SDA and SCL				550	pF
t_{SP}	Pulse width of spikes which must be suppressed by input filter	SCL, SDA only	0		50	ns

Notes: Refer to Typical Characteristics waveforms/graphs for closed loop data and variation with input supply and temperature. Electrical specifications reflects open loop steady state data. System specifications reflects both steady state and dynamic close loop data associated with the recommended external components.

Guarantee Levels:
† – Guaranteed by Design Only. Not Characterized or Production Tested.

Table 7. SYSTEM CHARACTERISTICS

System Specifications are guaranteed by design and are not production tested. They reflect closed loop performance using the Recommended Layout and External Components. Minimum and Maximum values are at AV_{IN} = PV_{IN} = 2.5 V to 5.5 V & PV_{IN} > V_{BUCK} + 350 mV and PV_{IN} < V_{BST} − 250 mV, V_{IN12} = 2.5 V to 5.5 V & V_{IN} > $V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, V_{IN4} > $V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C, AV_{IN} = PV_{IN} = V_{IN12} = 3.8 V, V_{IN3} = V_{IN4} = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, V_{LDO1} = V_{LDO2} = 2.8 V, V_{LDO3} = V_{LDO4} = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOFT START						
$T_{SS\ BK}$	Soft−Start	Time from enabling to 95% of V_{OUT} Target of 1.1 V, I_{OUT} = 300 mA and 1.2 A, Auto Mode, C_{OUT} = 10 uF, PV_{IN} = 3.0 V to 4.4 V		300	480	μs
RIPPLE						
$V_{BK\ PFM\_RPL}$	Output Ripple	I_{OUT} = 20 mA, PFM Mode		30	40	mV
$V_{BK\ PWM\_RPL}$		I_{OUT} = 200 mA, PWM Mode			10	mV
REGULATION & TRANSIENT						
REG_{BK_LOAD}	Load Regulation	I_{OUT} = 1 mA to 1200 mA, PWM Mode	−1.5		1.5	%
REG_{BK_LINE}	Line Regulation	V_{IN} = 3.0 V to 4.4 V , I_{OUT} = 50 mA, 300 mA, and 1200 mA, PWM Mode	−0.5		0.5	%
$V_{BK\ TR\_LD}$	Load Transient	I_{OUT} = 240 mA <−> 960 mA, T_R = T_F = 1 us, V_{OUT} = 1.1 V, PV_{IN} = 3.8 V, Auto Mode, Trecovery < 10 us			±70	mV
I_{OUT} MAX						
IO_{MAX_BK}	I_{OUT} Max		1200			mA
EFFICIENCY						
EFF_{BK}	Efficiency	I_{OUT} = 10 mA, V_{OUT} = 2.85 V, PV_{IN} = 3.8 V	92			%
		I_{OUT} = 600 mA, V_{OUT} = 2.85 V, PV_{IN} = 3.8 V	93			%
		I_{OUT} = 1.2 A, V_{OUT} = 2.85 V, PV_{IN} = 3.8 V	90			%
		I_{OUT} = 200 mA to 600 mA, V_{OUT} = 1.1 V, PV_{IN} = 3.8 V	85			%
		I_{OUT} = 10 mA, V_{OUT} = 1.1 V, PV_{IN} = 3.8 V	84			%
		I_{OUT} = 600 mA, V_{OUT} = 1.1 V, PV_{IN} = 3.8 V	85			%
		I_{OUT} = 1.2 A, V_{OUT} = 1.1 V, PV_{IN} = 3.8 V	77			%
SOFT START						
T_{LIN_BST}	Soft Start Input Linear Current Limit			450	700	mA
T_{SS_BST}	Soft−Start	Time from enabling to 90% of V_{OUT} Target, I_{OUT} = 100 mA		280	580	μs
$T_{SS\ BST\_PS}$		PV_{IN} = 3.8 V, BST_MODE bit = 1, V_{OUT} = PV_{IN} (Start up into Forced Pass−Through Mode)		190	580	μs
RIPPLE						
$V_{BST\ PFM\_RPL}$	Output Ripple	I_{OUT} = 10 mA, V_{OUT} = 5 V, PV_{IN} = 3.8 V		40	80	mV
$V_{BST\ PWM\_RPL}$		I_{OUT} = 500 mA, V_{OUT} = 5 V, PV_{IN} = 3.8 V		20	40	mV
REGULATION & TRANSIENT						
REG_{BST_LD}	Load Regulation	I_{OUT} = 1 mA <−> 1 A, PV_{IN} = 3.8 V, V_{OUT} = 5.0 V	−1.5		+1.5	%
REG_{BST_LN}	Line Regulation	PV_{IN} = 3.0 V <−> 4.4 V , I_{OUT} = 50 mA and 1 A	−0.5		+0.5	%
$V_{BST\ TR\_LD}$	Load Transient	I_{OUT} = 200 mA <−> 800 mA, T_R = T_F = 2 us, V_{OUT} = 5.0 V, PV_{IN} = 3.8 V, Trecovery < 10 us			±150	mV
I_{OUT} MAX						
I_{O_BST}	I_{OUT} Max		1000			mA

Table 7. SYSTEM CHARACTERISTICS (continued)

System Specifications are guaranteed by design and are not production tested. They reflect closed loop performance using the Recommended Layout and External Components. Minimum and Maximum values are at $AV_{IN} = PV_{IN}$ = 2.5 V to 5.5 V & $PV_{IN} > V_{BUCK}$ + 350 mV and $PV_{IN} < V_{BST}$ − 250 mV, V_{IN12} = 2.5 V to 5.5 V & $V_{IN} > V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, $V_{IN4} > V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C, $AV_{IN} = PV_{IN} = V_{IN12}$ = 3.8 V, $V_{IN3} = V_{IN4}$ = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, $V_{LDO1} = V_{LDO2}$ = 2.8 V, $V_{LDO3} = V_{LDO4}$ = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
EFFICIENCY						
EFF_{BST}	Efficiency	PV_{IN} = 3.8 V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA	88			%
		PV_{IN} = 3.8 V, V_{OUT} = 5.0 V, I_{OUT} = 600 mA	94			%
		PV_{IN} = 3.8 V, V_{OUT} = 5.0 V, I_{OUT} = 1 A	93			%
LDO1/2 SOFT START						
T_{SS_LDO12}	Startup Time	Time from enabling to 90% of V_{OUT} (2.8 V), I_{OUT} = 10 mA, C_{OUT} = 14.7 uF		100	150	µs
PSRR & NOISE						
$PSRR_{L12\ 1KHZ}$	Power Supply Rejection Ratio	V_{IN12} = 3.4 V, I_{OUT} = 100 mA, F = 1 kHz, C_{OUT} = 2.2 uF, I_{BUCK} = 1.2 A, I_{BST} = 1 A		70		dB
$PSRR_{L12\ 100KHZ}$		V_{IN12} = 3.4 V, I_{OUT} = 100 mA, F = 100 kHz, C_{OUT} = 2.2 uF, I_{BUCK} = 1.2 A, I_{BST} = 1 A		45		dB
V_{N_L12}	LDO1/2 Output Noise	V_{IN12} = 3.4 V, V_{OUT} = 1.8 V and 2.8 V, F = 100 Hz to 100 kHz, I_{OUT} = 100 mA, C_{OUT} = 2.2 uF		35	60	uVrms
REGULATION & TRANSIENT PERFORMANCE						
REG_{L12_LD}	LDO Load Regulation	I_{OUT} = 100 uA to 300 mA, $AV_{IN} = V_{IN12}$ = 3.8 V	−0.5		+0.5	%
REG_{L12_LN}	LDO Line Regulation	$AV_{IN} = V_{IN12}$ = 3.1 V to 4.4 V and $AV_{IN}/V_{IN12} > V_{OUT}$ + 300 mV, I_{OUT} = 50 mA and 300 mA	−0.5		+0.5	%
$V_{L12\ TR\_LD}$	LDO Load Transient	I_{OUT} = 1 mA <-> 100 mA, 150 mA/us			±50	mV
SHORT CIRCUIT						
$T_{L12\ SC\_DEB}$	Short Circuit Debounce Timer			40		µs
$T_{L12\ SC\_RST}$	Period from Short Circuit Shutdown to Restart			20		ms
LDO3/4 SOFT START						
T_{SS_L34}	Soft Start Time	Time from enabling to 90% of V_{OUT} (1.8 V), I_{OUT} = 10 mA, C_{OUT} = 14.7 uF		80	150	µs
PSRR & NOISE						
$PSRR_{L34}$	Power Supply Rejection Ratio	I_{OUT} = 100 mA, F = 1 kHz, $V_{IN3/4}$ = 1.95 V, C_{OUT} = 2.2 uF, I_{BUCK} = 1.2 A, I_{BST} = 1 A		60		dB
		I_{OUT} = 100 mA, F = 10 kHz, $V_{IN3/4}$ = 1.95 V, C_{OUT} = 2.2 uF, I_{BUCK} = 1.2 A, I_{BST} = 1 A		45		dB
V_{N_L34}	LDO3/4 Output Noise	$V_{IN3/4}$ = 1.95 V, V_{OUT} = 1.8 V, F = 100 Hz to 100 kHz, I_{OUT} = 100 mA, C_{OUT} = 2.2 uF		25	60	uVrms
REGULATION & TRANSIENT PERFORMANCE						
REG_{L34_LD}	LDO Load Regulation	I_{OUT} = 100 uA to 300 mA, $AV_{IN} = V_{IN3/4}$ = 3.8 V, V_{OUT} = 1.8 V	−0.5		+0.5	%
REG_{L34_LN}	LDO Line Regulation	$AV_{IN} = V_{IN3/4}$ = 3.0 V to 4.4 V and $AV_{IN} = V_{IN3/4} > V_{OUT}$ + 150 mV, I_{OUT} = 50 mA and 300 mA	−0.5		+0.5	%
$V_{L34\ TR\_LD}$	LDO Load Transient	I_{OUT} = 1 mA <-> 100 mA, 150 mA/us			±50	mV

Table 7. SYSTEM CHARACTERISTICS (continued)

System Specifications are guaranteed by design and are not production tested. They reflect closed loop performance using the Recommended Layout and External Components. Minimum and Maximum values are at AV_{IN} = PV_{IN} = 2.5 V to 5.5 V & PV_{IN} > V_{BUCK} + 350 mV and PV_{IN} < V_{BST} − 250 mV, V_{IN12} = 2.5 V to 5.5 V & V_{IN} > $V_{LDO1/2}$ + 300 mV, V_{IN3}, V_{IN4} = 1.95 V to 5.5 V & V_{IN3}, V_{IN4} > $V_{LDO3/4}$ + 150 mV, V_{BUCK} = 0.6 V to 3.3 V, V_{BST} = 3.0 V to 5.7 V, V_{LDO1}, V_{LDO2}, V_{LDO3} and V_{LDO4} = 0.8 V to 3.3 V, T_A = −40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C, AV_{IN} = PV_{IN} = V_{IN12} = 3.8 V, V_{IN3} = V_{IN4} = 1.95 V, V_{BUCK} = 1.1 V, V_{BST} = 5.0 V, V_{LDO1} = V_{LDO2} = 2.8 V, V_{LDO3} = V_{LDO4} = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SHORT CIRCUIT						
$T_{L34\ SC\_DEB}$	Short Circuit Debouncer Timer			40		μs
$T_{L34\ SC\_RST}$	Period from Short Circuit Shutdown to Restart			20		ms
THERMAL PROTECTION						
T_{WRN}	Thermal Warning		115	125	135	°C
T_{SD}	Thermal Shutdown		130	140	150	°C

TYPICAL CHARACTERISTICS

Unless otherwise specified, $T_A = 25°C$, $AV_{IN} = PV_{IN} = V_{IN12} = 3.8$ V, $V_{IN3} = V_{IN4} = 1.95$ V, $V_{BUCK} = 1.1$ V, $V_{BST} = 5.0$ V, $V_{LDO1} = V_{LDO2} = 2.8$ V, $V_{LDO3} = V_{LDO4} = 1.8$ V, Recommended Layout and External Components.

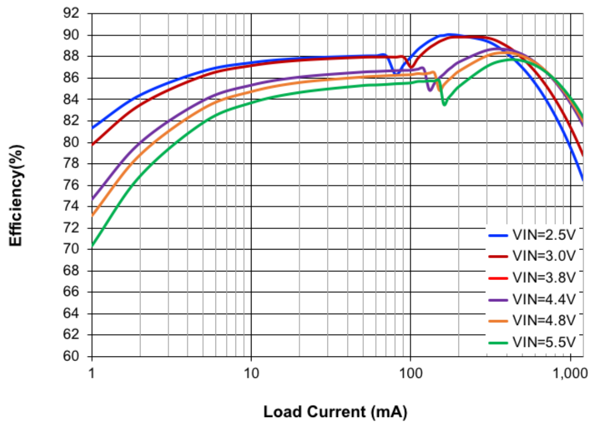


Figure 4. Buck Efficiency vs. Load Current and Input Voltage, V_{OUT} = 1.1 V, Auto Mode

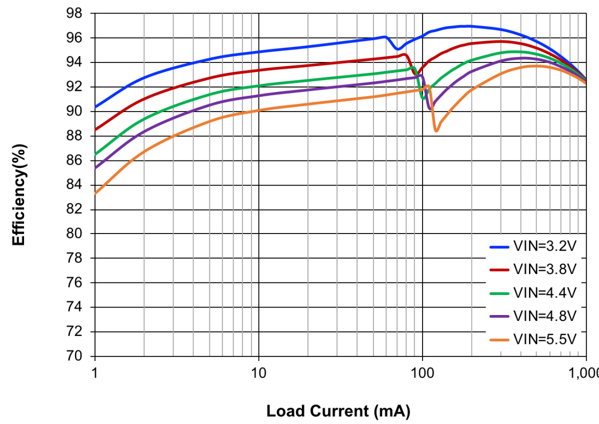


Figure 5. Buck Efficiency vs. Load Current and Input Voltage, V_{OUT} = 2.85 V, Auto Mode

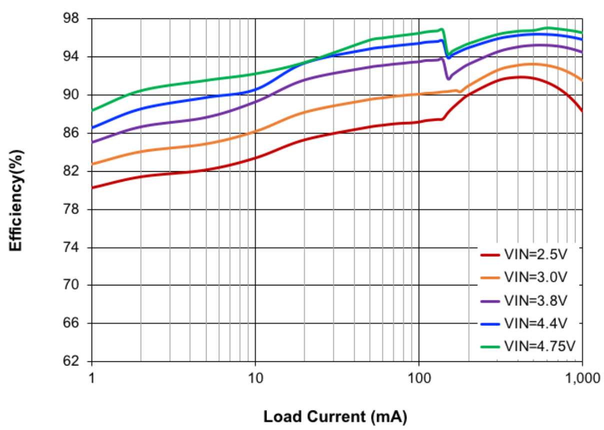


Figure 6. Boost Efficiency vs. Load Current and Input Voltage, V_{OUT} = 5.0 V, Auto Mode

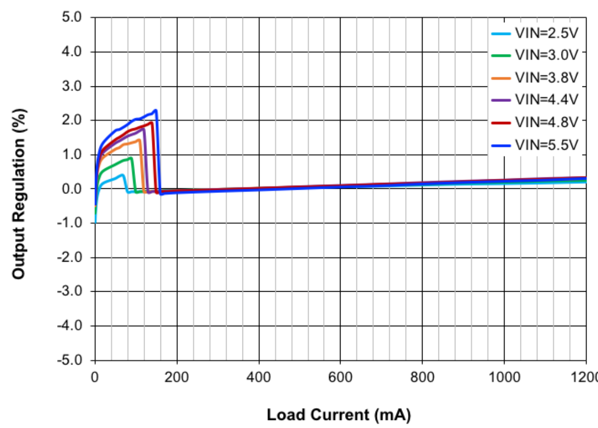


Figure 7. Buck Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 1.1 V, Auto Mode

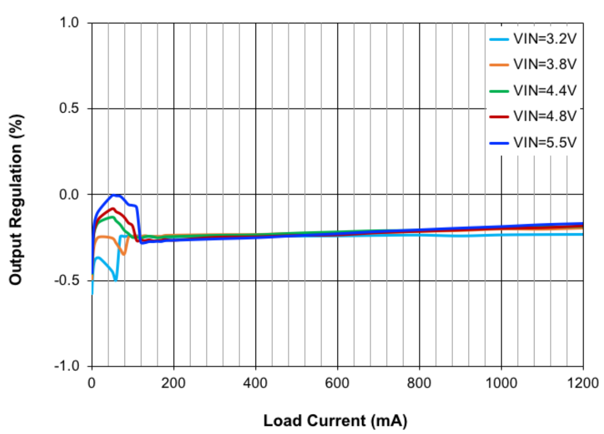


Figure 8. Buck Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 2.85 V, Auto Mode

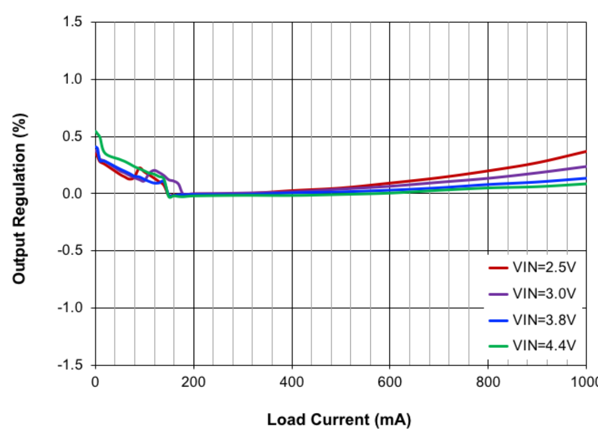


Figure 9. Boost Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 5.0 V, Auto Mode

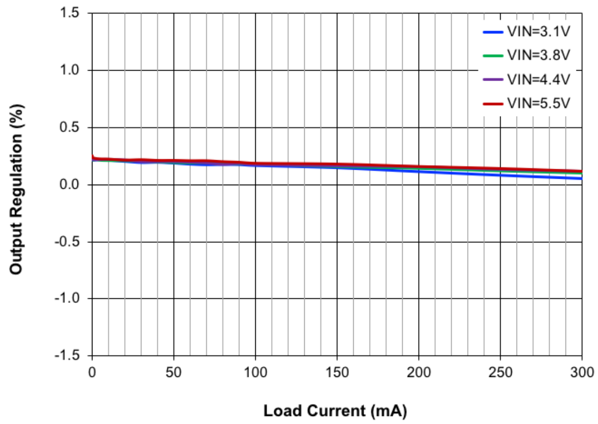


Figure 10. LDO1/2 Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 2.8 V, Auto Mode

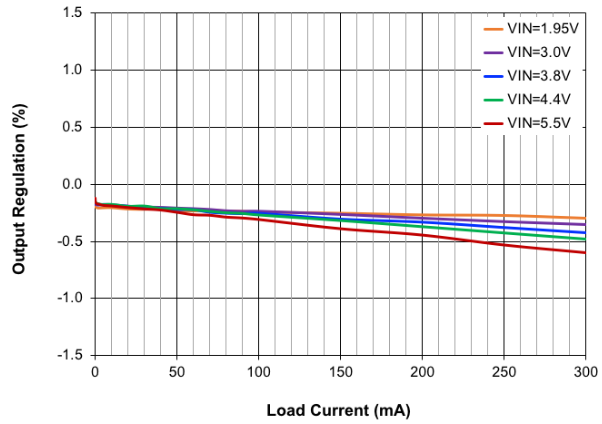


Figure 11. LDO3/4 Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 1.8 V, Auto Mode

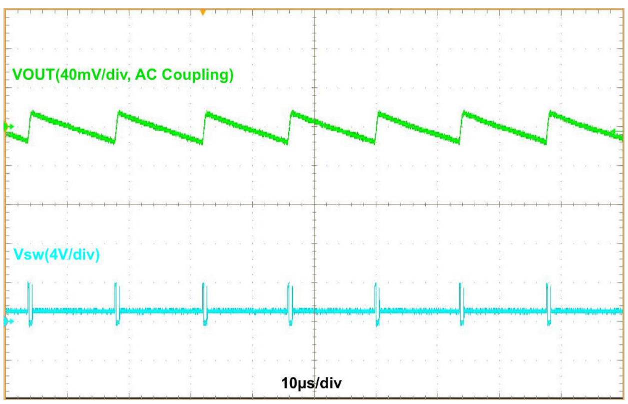


Figure 12. Buck Output Ripple in PFM Mode, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, I_{OUT} = 10 mA

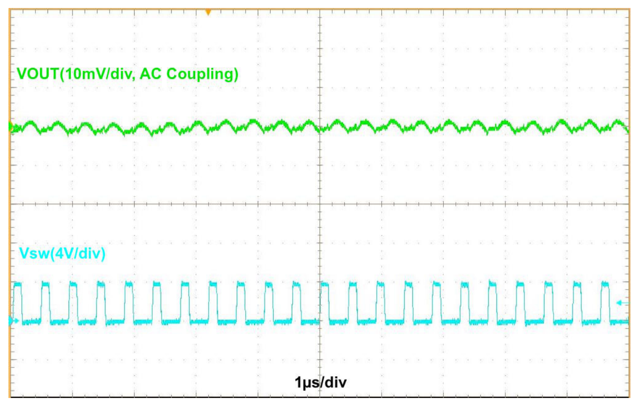


Figure 13. Buck Output Ripple in PWM Mode, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, I_{OUT} = 200 mA

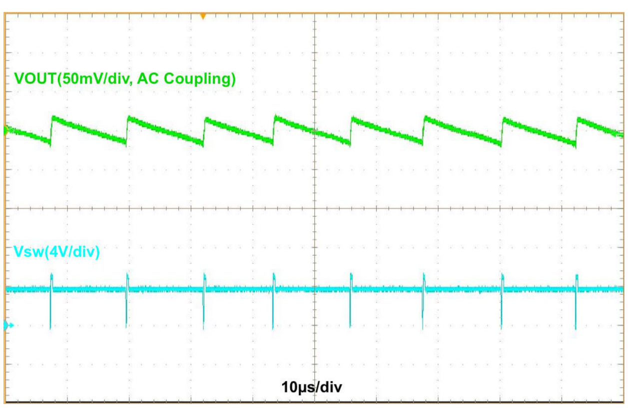


Figure 14. Boost Output Ripple in PFM Mode, V_{IN} = 3.8 V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, Auto Mode

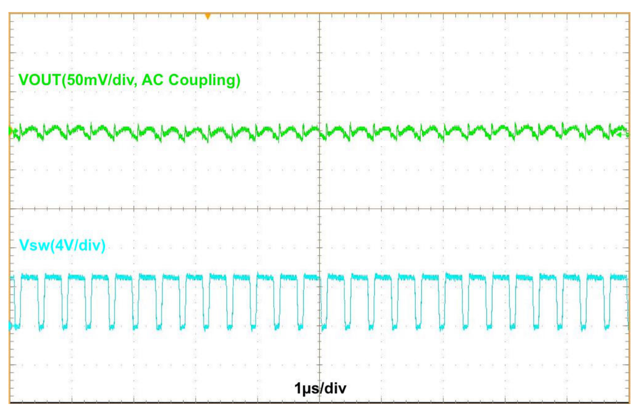


Figure 15. Boost Output Ripple in PWM Mode, V_{IN} = 3.8 V, V_{OUT} = 5.0 V, I_{OUT} = 500 mA, Auto Mode

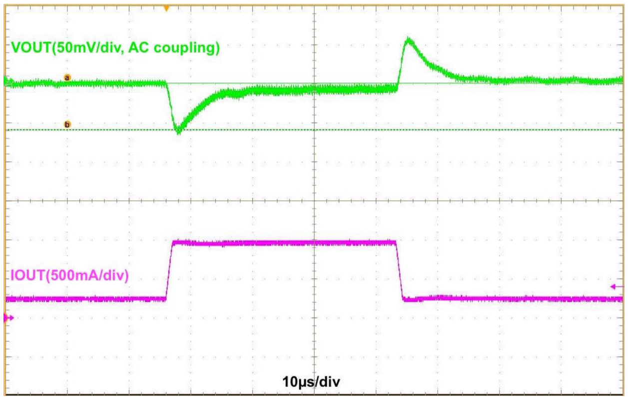


Figure 16. Buck Load Transient, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, 240 mA ⇔ 960 mA, 1 µs Edge, Auto Mode

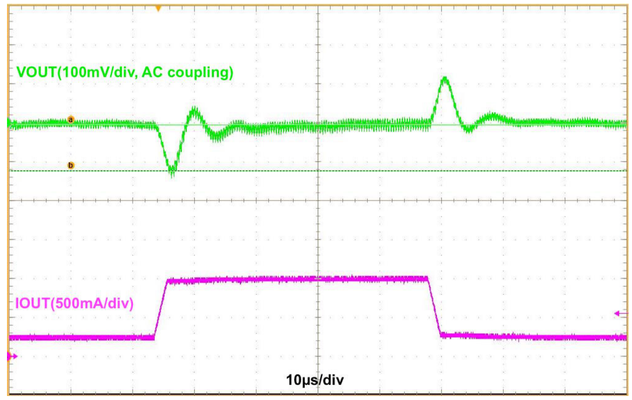


Figure 17. Boost Load Transient, V_{IN} = 3.8 V, V_{OUT} = 5.0 V, 200 mA ⇔ 800 mA, 2 µs Edge, Auto Mode

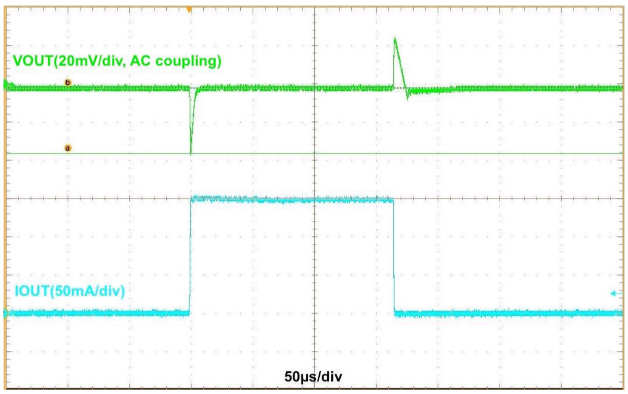


Figure 18. LDO1/2 Load Transient, V_{IN} = 3.8 V, V_{OUT} = 2.85 V, 1 mA ⇔ 150 mA, 1 µs Edge

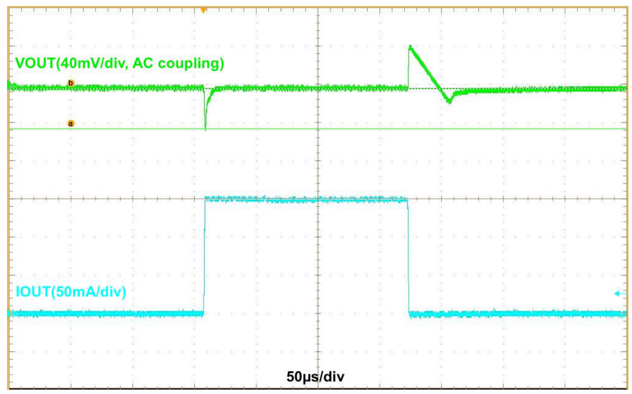


Figure 19. LDO3/4 Load Transient, V_{IN} = 1.95 V, V_{OUT} = 1.8 V, 1 mA ⇔ 150 mA, 1 µs Edge

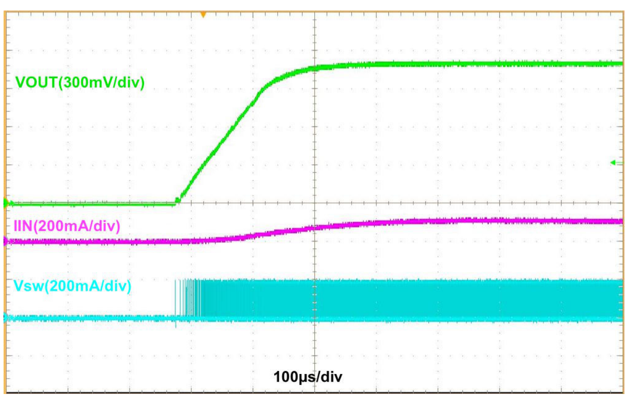


Figure 20. Buck Start−up, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, 300 mA Resistive Load, Auto Mode

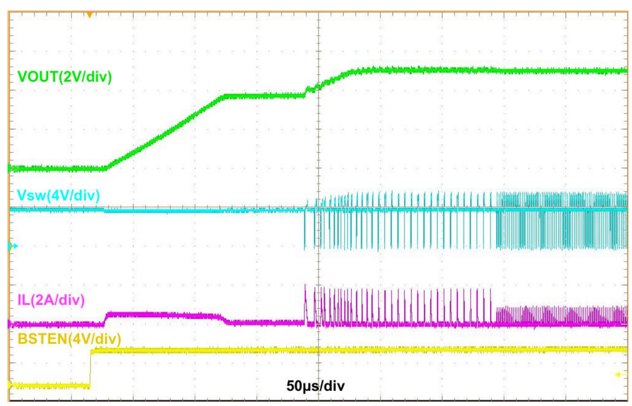


Figure 21. Boost Start−up, V_{IN} = 3.8 V, V_{OUT} = 5.0 V, 100 mA Resistive Load, Auto Mode

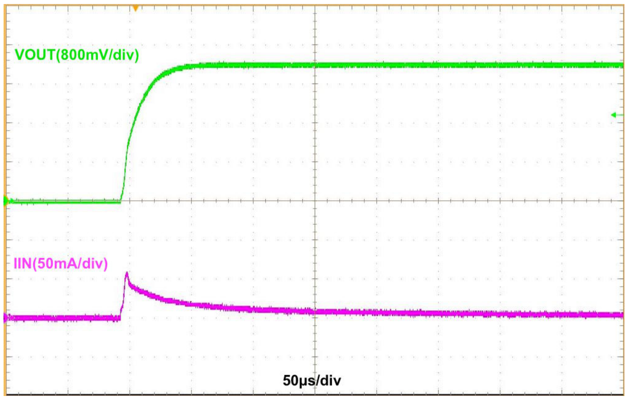


Figure 22. LDO1/2 Start−up, V_{IN} = 3.8 V, V_{OUT} = 2.8 V, No Load

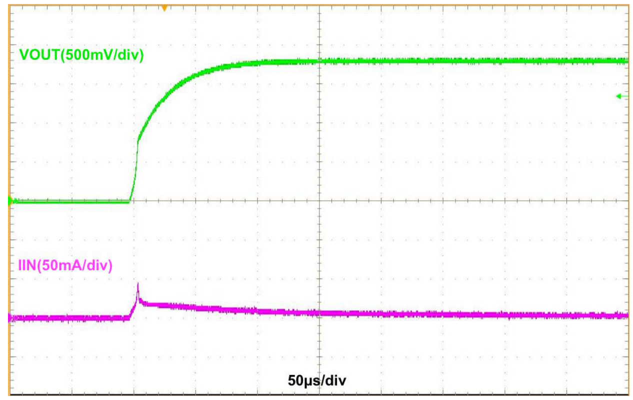


Figure 23. LDO3/4 Start−up, V_{IN} = 1.95 V, V_{OUT} = 1.8 V, No Load

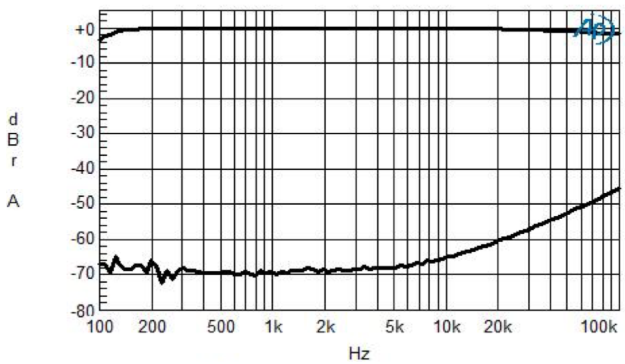


Figure 24. LDO1/2 PSRR vs. Frequency, 100 mA Load

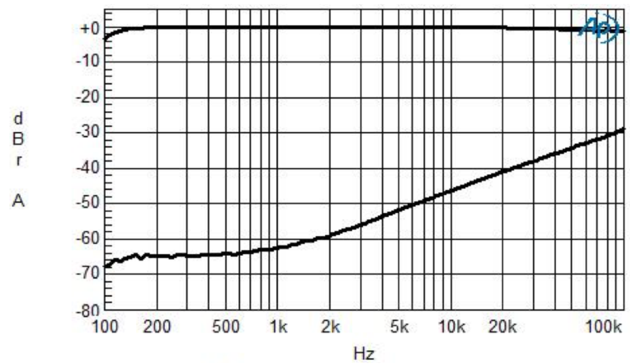


Figure 25. LDO3/4 PSRR vs. Frequency, 100 mA Load

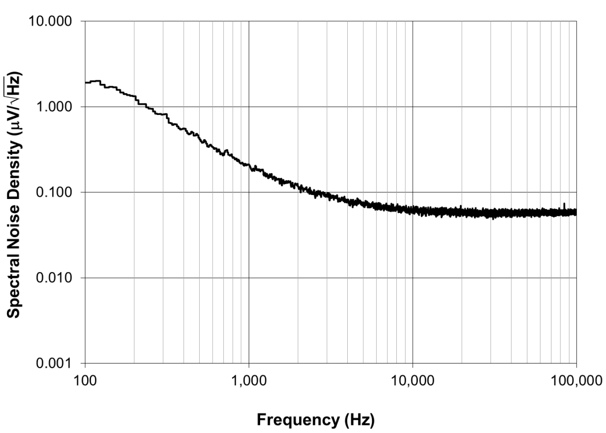


Figure 26. LDO1/2 Output Noise Voltage vs. Frequency, 100 mA Load

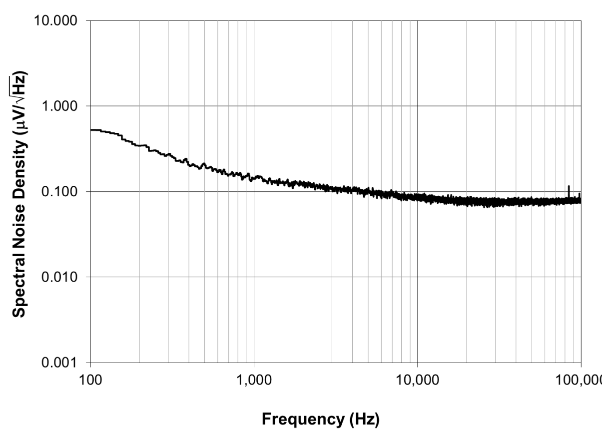


Figure 27. LDO3/4 Output Noise Voltage vs. Frequency, 100 mA Load

FUNCTIONAL SPECIFICATIONS

Device Operation

Overview

The FAN53880 is a Mini−PMIC containing:

- One 2.5 MHz, 1200 mA Buck converter
- One 2.5 MHz, 1000 mA Boost converter
- Four 300 mA low noise LDOs

Each converter can be individually enabled/disabled through I2C communication. The Boost converter also has an enable pin, BSTEN. A configurable sequencer is available for power−up and power−down of the Buck and LDOs.

Many of the ICs protection mechanisms have programmable thresholds. For fault handling, a dedicated interrupt pin, mask−able interrupt bits, and real time status bits are provided.

The Buck and Boost allow the use of small inductors and capacitors for a small overall solution size.

Refer to the figure below for an additional overview of the FAN53880 operation.

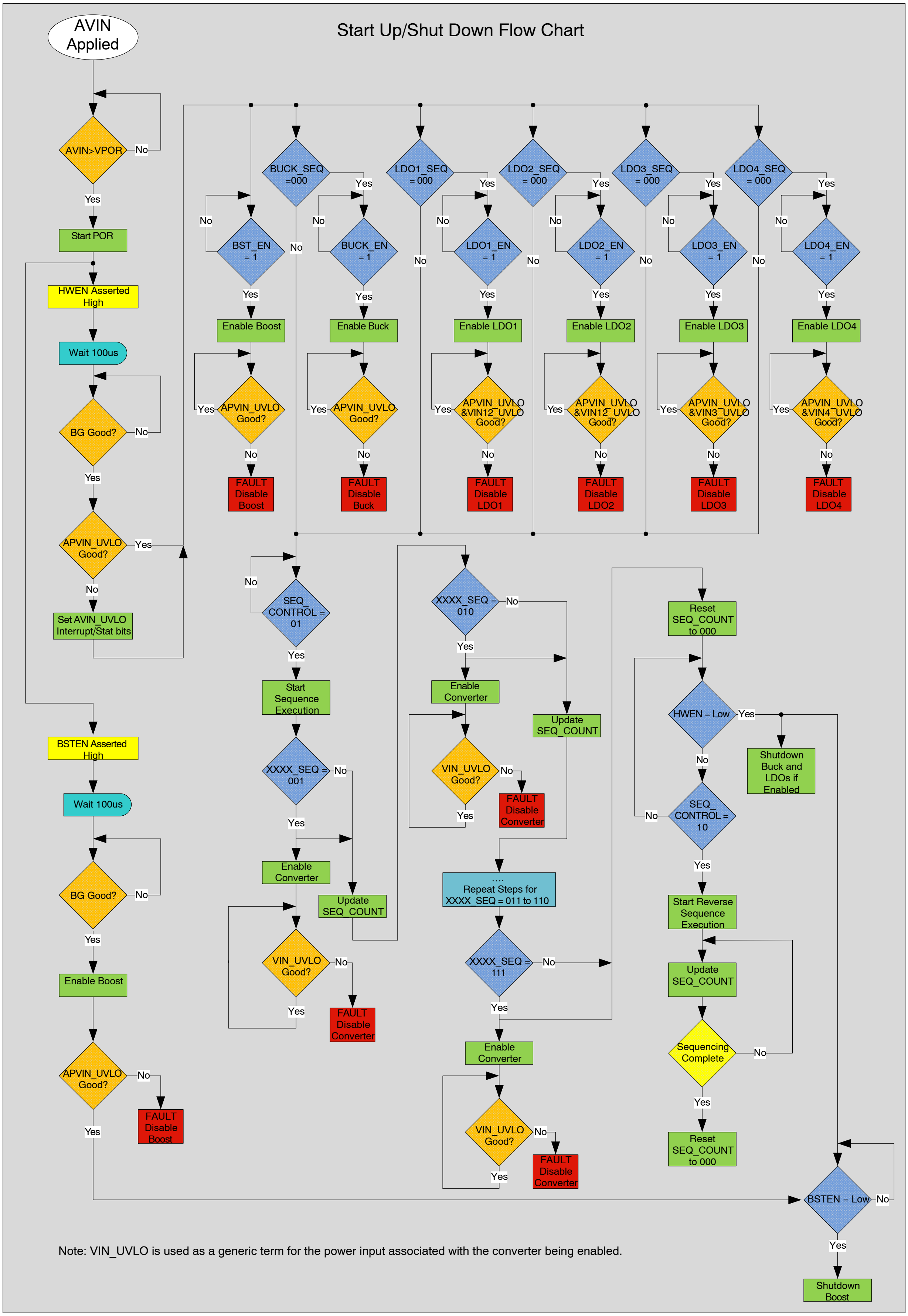


Figure 28. Start–up and Shut Down Flow Chart

Power Supplies

All converters use AV_{IN} to power their analog and control circuitry.

The Buck and Boost use PV_{IN} as their power source. PV_{IN} must remain within 25 mV of AV_{IN} for proper device operation (it's recommended to locally connect PVIN to AVIN). Because of this, the term APV_{IN} may instead be used throughout this datasheet.

LDO1 and LDO2 use V_{IN12}, LDO3 uses V_{IN3} and LDO4 uses V_{IN4} to power their outputs. These power supplies have independent UVLO thresholds with dedicated interrupts and status bits.

See Table 8 for details.

Table 8. CONVERTER DEPENDENCY OFF POWER INPUTS

Converter	AV_{IN}	PV_{IN}	V_{IN12}	V_{IN3}	V_{IN4}
BUCK	X	X			
BOOST	X	X			
LDO1/LDO2	X		X		
LDO3	X			X	
LDO4	X				X

POR

When a rising AV_{IN} reaches ~2 V a POR occurs where registers reset and are readable through I2C.

See Table 9 for details.

Table 9. PMIC OPERATION IN APVIN UVLO

AV_{IN} State	HWEN or BSTEN = High	Results	After AV_{IN} > UVLO
$AV_{IN} < V_{POR}$	No	(1)	(4)
$V_{POR} < AV_{IN} <$ UVLO	No	(2)	(5)
$AV_{IN} < V_{POR}$	Yes	(1)	(4)
$V_{POR} < AV_{IN} <$ UVLO	Yes	(3)	(6)

1. Device in shutdown, I2C registers not reliable
2. Band Gap off, I2C registers readable
3. Band Gap on, I2C registers readable
4. All registers set to their default values
5. Registers retain value prior to the fault and begin a start up after HWEN or BSTEN are high
6. Registers retain value prior to fault and do an automatic restart

UVLO Rising

When rising AV_{IN} reaches $V_{VIN\_UVLO\_RISE}$ the ICs internal circuitry is operable and an interrupt is generated. The part will be in a Sleep state if HWEN=BSTEN=LOW.

UVLO Falling

When falling AV_{IN} reaches $V_{VIN\_UVLO\_FALL}$ a Chip Fault occurs, all converters are suspended, an interrupt generated, and related Status bits set. Registers will not reset to default values unless AV_{IN} falls below POR (~2 V).

Control Pins and Enable Bits

There are two control pins, HWEN and BSTEN.

When HWEN=HIGH, the ICs internal circuitry turns on in Standby state where converters can be enabled through I2C, assuming their related power supplies are above their UVLO thresholds (refer to the Electrical Characteristics table).

Each converter has an independent enable bit, XXX_EN.

The BSTEN pin is a hardware enable option for the Boost and its basic control circuits. BSTEN functions independent of HWEN.

Enable Auto−Sequencing

A programmable sequencer is available for controlling power−up and power−down timing of the Buck and LDOs.

There are 7 time slots available and the sequencing speed (period per slot) is programmable. The FAN53880 sequences through time slots 001 to 111 during power up, and from 111 to 001 during power down when initiated with the SEQ_CONTROL bits.

When a converter is added into a sequence slot, it can no longer be enabled using the XXX_EN bits.

If a converter faults during a start−up sequence, the other converters will be started in their assigned time slot and the faulted converter will not attempt to re−enable. An interrupt is generated to inform the host of the fault and a status bit is set.

The two tables below summarize control pin, register bit, and sequence combinations.

Table 10. BUCK AND LDO ENABLE/DISABLE CONTROLS

Buck and LDO Control				
HWEN	XXX_SEQ	XXX_EN	SEQ_CONTROL Dependent	On/Off
Low	000	0	No	Off
High	000	0	No	Off
Low	>000	0	No	Off
High	>000	0	Yes	CNTL
Low	000	1	No	Off
High	000	1	No	On
Low	>000	1	No	Off
High	>000	1	Yes	CNTL

NOTE: CNTL indicates that the state of the output will be dependent on the setting of the SEQ_CONTROL bits. When HWEN is high, SEQ_CONTROL = 01 will enable any outputs based on their XXX_SEQ > 000.

Table 11. BOOST ENABLE/DISABLE CONTROLS

Boost Control			
HWEN	BSTEN	BST_ENx	On/Off
Low	Low	0	Off
High	Low	0	Off
Low	High	0	On
High	High	0	On
Low	Low	1	Off
High	Low	1	On
Low	High	1	On
High	High	1	On

NOTE: The Boost Control table above shows that the Boost operation requires either BSTEN to be high or a combination of HWEN high and one of the enable bits in register 0x0A needs to be set to 1.

Fault Protection

Fault Protection Overview

Each fault described below has a dedicated interrupt and status bit.

The FAN53880 has two levels of fault protection:

- Chip Faults
  (TSD, APV_{IN} UVLO)
  The protection suspends or shuts off all enabled converters. Recovery behavior depends on the FLT_SD_B bit setting.
- Converter Faults
  (UVP, OVP, IPK, Short Circuit, V_{IN12}/V_{IN3} /V_{IN4} UVLO)
  These protections allow the converter to remain enabled or suspends or shuts off the faulted converter, but doesn't affect operation of non−related converters. The specific fault behavior depends on the FLT_SD_B bit setting.

FLT_SD_B Bit

There are two I2C selectable fault behavior options:

- Multiple Fault Shutdown (default)
  Limits repetitive starting and faulting of a converter or chip faults to 4 failures.
- Automatic Fault Recovery
  No limit to repetitive starting and faulting of a converter or to number of chip faults.

NOTE: Sequencer fault behavior is independent of these protection schemes.

Multiple Fault Shutdown

FLT_SD_B="0" (default)
If a fault occurs, the IC will:

- Suspend the converter
- Set Interrupt and Status bits
- Increment the internal 4−fault counter
- Wait 20 ms
- Re−enable the converter if XXX_EN="1" or shut off the converter if XXX_SEQ="1"
  - Re−enable requires another SEQ_CONTROL="01" write

NOTE: UVLO and TSD faults will not re−enable the converter after 20 ms unless the fault was removed.

If any four Chip Faults occur, the IC will:

- Shut off all converters
- Reset all XXX_EN and XXX_SEQ bits to "0"
- Set Interrupt and Status bits, including the CHIP_SUSD Status bit, to "1". This bit will only clear after both HWEN and BSTEN are set LOW

If any four Converter Faults occur, the IC will:

- Shut off that converter
- Set XXX_SUSD bit to "1". This bit will only clear after that converter is successfully re−enabled
- Reset that converter's XXX_EN or XXX_SEQ bit to "0"

Re−enabling any converter after a fourth Chip Fault first requires setting the HWEN and BSTEN pins LOW. Any time HWEN and BSTEN pin is taken LOW, all fault counters are globally reset.

Automatic Fault Recovery

FLT_SD_B="1" (should only be set prior to enabling any converter).

If a fault occurs, the IC will:

- Set Interrupt and Status bits

Also:

Chip Faults

- Suspend all converters
- Any converter with XXX_EN="1" will re−enable after the APV_{IN} UVLO or TSD fault is removed
- Any converter with XXX_SEQ="1" re−enable requires another SEQ_CONTROL="01" write

Converter Faults

- Any converter with an OVP or UVP, or any LDO with an IPK or LDO short circuit fault will remain enabled. Otherwise suspend that converter and:
  - Automatically re−enable after $V_{IN12}/V_{IN3}/V_{IN4}$ UVLO fault is removed
  - Automatically re−enable 20 ms after Buck or Boost IPK fault or short circuit if XXX_EN="1", or remain off until another SEQ_CONTROL="01" write if XXX_SEQ="1"

Thermal Management

When the die temperature rises to T_{WRN}, a Thermal Warning (TSD_WRN) interrupt is issued. Also, a Status bit will be set and remain set until the die temperature drops to a nominal value of 110°C.

If the die temperature continues to rise above T_{WRN}, Thermal Shutdown (TSD) will occur. After the die temperature has fallen below T_{WRN}, recovery behavior depends on the FLT_SD_B bit setting. Refer to the Fault Protection section for details on Chip Faults.

Fault Handling

Mask−able Interrupt bits, a dedicated INTB pin, and real time status bits are provided. Each converter has independent protection debounce timers.

An interrupt is generated each time a fault occurs. All bits set in the Interrupt registers must be cleared to reset the INTB pin to HIGH.

Buck Functionality

Startup Behavior

The Buck can be enabled by two methods if and only if the HWEN pin is high:

- Setting BUCK_EN to "1"
- Setting BUCK_SEQ > "000" and SEQ_CONTROL to "01"

The Buck has internal soft−start and starts up within 400 μs (typical) when using the recommended external components.

Modes of Operation

During PWM operation, the Buck switches at a nominal fixed frequency of 2.5 MHz. In Automode at light load operation, the device will enter PFM mode. Instead, the Buck can be put into Forced PWM mode by setting the BUCK_MODE bit to "1". Also, the FAN53880 provides a bit, BUCK_LOAD, which the user can set to apply an internal artificial load to maintain a minimum switching frequency above 20 kHz.

Programmable Output Voltage

The Buck output voltage can be programmed via I2C in 12.5 mV steps.

Shutdown

When the Buck is disabled, switching will cease, the output tristated, and the output will be discharged via the load or if BUCK_DIS bit = "1", via the active discharge resistor.

Boost Functionality

Startup Behavior

The Boost can be enabled by two methods:

- Setting the BSTEN pin HIGH
- Setting the HWEN pin HIGH and setting any BOOST_ENx bit to "1"

The Boost can startup in PFM mode or automatic pass−through mode depending on the VIN to VOUT difference. When starting in PFM mode, the part has a linear mode which limits inrush currents. Once VOUT charges up to VIN, the linear mode current limit is disabled and the regulator uses one−quarter current limit to charge the output cap to the final VOUT target value. If VOUT fails to reach 90% of the VOUT target within 1 ms, a UVP fault is declared.

Modes of Operation

During PWM operation, the Boost switches at a nominal fixed frequency of 2.5 MHz. In Automode at light load operation, the device will enter PFM mode. Instead, the Boost can be put into Forced PWM mode by setting the BST_MODE bit to "1". Also, the FAN53880 provides a bit, BST_LOAD, which the user can set to apply an internal artificial load to maintain a minimum switching frequency above 20 kHz.

In normal operation, the device automatically transitions from Boost Mode to Pass−Through Mode if $V_{IN} > V_{OUT}$_target − 250 mV. In Pass−Through Mode, there is no switching and the device has a low impedance path between V_{IN} and V_{OUT}.

Programmable Output Voltage

The Boost output voltage can be programmed via I2C in 25 mV steps. When the output voltage is programmed to a lower voltage, the active pull−down is used to expedite the drop in voltage across the output capacitance.

Shutdown

When the Boost is disabled, switching will cease, the output tristated, and the output will be discharged via the load or if BOOST_DIS bit = “1”, via the active discharge resistor.

LDO Functionality

Startup Behavior

The LDO’s can be enabled by two methods if and only if the HWEN pin is high:

- Setting LDOx_EN to “1”
- Setting LDO_SEQ > “000” and SEQ_CONTROL to “01”

The Buck has internal soft−start which limits supply current to the LDOx_ILIM setting. If VOUT fails to reach UVP_{LDOxx_HYS} in T_{SS_LDOxx}, a UVP fault is declared.

Programmable Output Voltage

The LDO output voltages can be programmed via I2C in 25 mV steps.

I2C Functionality

Introduction

The FAN53880 serial interface is compatible with the Standard−Mode, Fast−Mode, and Fast−Mode Plus I^2C bus specifications. The SCL pin is an input and the SDA pin is a bi−directional open−drain output. The IC supports single register read and write transactions as well as multiple register read transactions.

Slave Address

The default I2C Slave Address is the Table 12 and Table 13. Other slave addresses can be accommodated upon request. Contact your ON Semiconductor representative if a different slave address is required.

Table 12. I2C SLAVE ADDRESS

Device	Hex	Decimal	7 bit Binary
FAN53880	7h35	53d	0110101

Table 13. FAN53880 (7 BIT) SLAVE ADDRESS BYTE

7	6	5	4	3	2	1	X
0	1	1	0	1	0	1	R/W

NOTE: READ = 1
WRITE = 0

Timing Diagrams

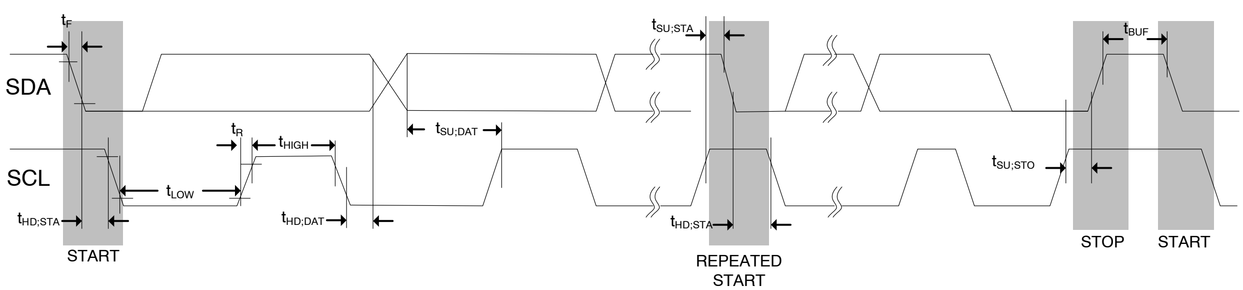


Figure 29. I2C Interface Timing for Fast−Mode Plus, Fast−Mode, and Standard−Mode

Normally, data transfer occurs when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically data transitions at or after the subsequent falling edge of SCL to provide ample setup time for the next data bit to be ready before the subsequent rising edge of SCL.

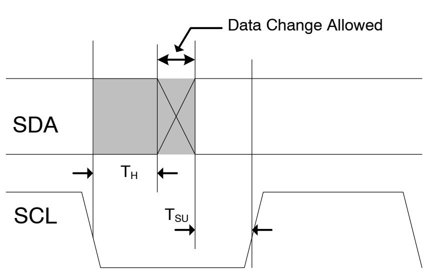


Figure 30. Data Transfer Timing

The idle state of the I^2C bus is SDA and SCL both in the HIGH state. A valid transaction begins with a START condition which occurs when SDA transitions from HIGH to LOW when SCL remains HIGH.

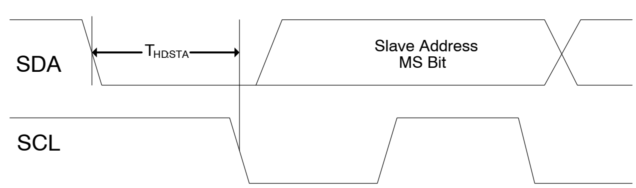


Figure 31. START Condition

A valid transaction ends with a STOP condition which occurs when SDA transitions from LOW to HIGH while SCL remains HIGH.

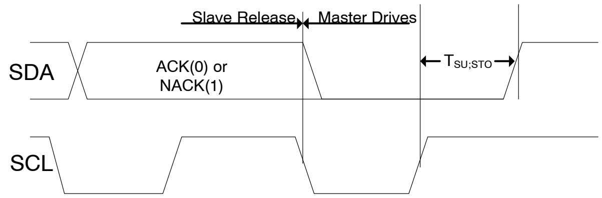


Figure 32. STOP Condition

A REPEATED START condition is functionally equivalent to a STOP condition followed immediately by a START condition. During a read from the IC, the master issues a REPEATED START after sending the register address and before re−sending the slave address. The REPEATED START is a HIGH to LOW transition on SDA while SCL is HIGH,

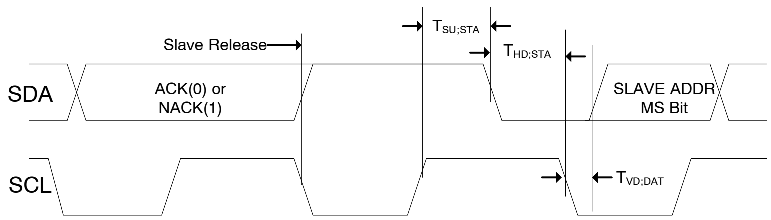


Figure 33. REPEATED START Condition

Read and Write Transactions

The FAN53880 supports the following read and write transaction protocols.

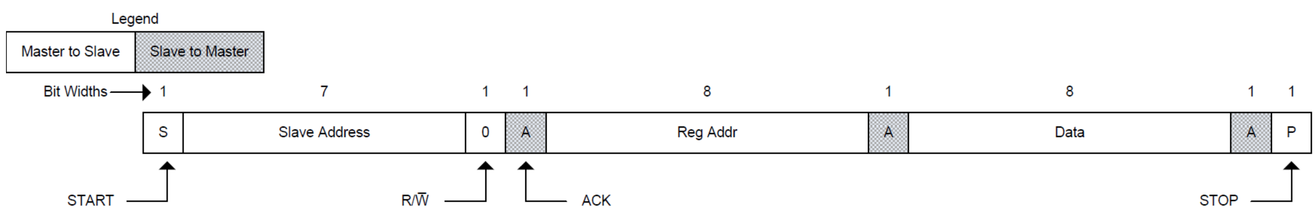


Figure 34. Single Register Write Transaction

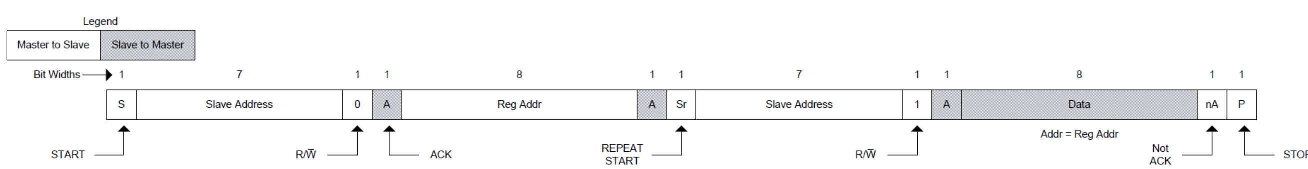


Figure 35. Single Register Read Transaction

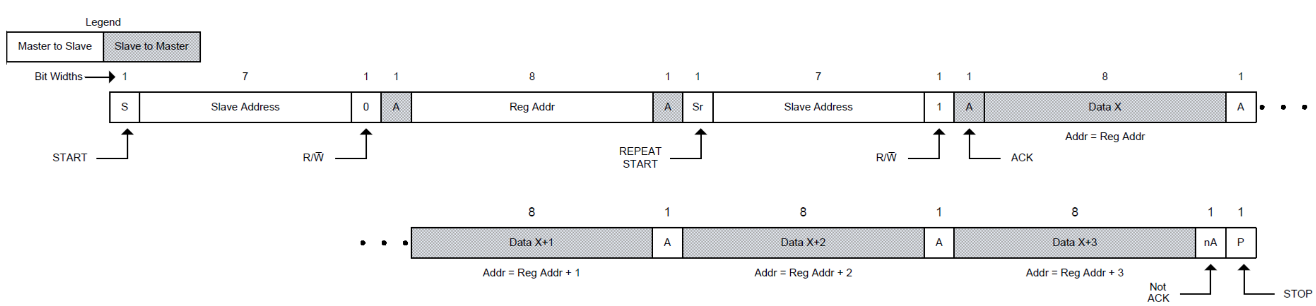


Figure 36. Multiple Register Read Transaction

REGISTER MAPPING TABLE

Table 14. REGISTER MAPPING

					Read Only	**Write Only**	**Read / Write**	**Read / Clear**	**Write / Clear**
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x00	PRODUCT ID	Product ID							
0x01	SILICON REV ID	Revision							
0x02	BUCK	BUCK_OUT							
0x03	BOOST	Reserved	BOOST_VOUT						
0x04	LDO1	LDO1_PASSTHRU	LDO1_VOUT						
0x05	LDO2	LDO2_PASSTHRU	LDO2_VOUT						
0x06	LDO3	LDO3_PASSTHRU	LDO3_VOUT						
0x07	LDO4	LDO4_PASSTHRU	LDO4_VOUT						
0x08	IOUT	0	LDO4_ILIM	0	LDO3_ILIM	0	LDO2_ILIM	0	LDO1_ILIM
0x09	ENABLE	BST_MODE	BUCK_MODE	0	BUCK_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN
0x0A	BOOST_ENABLE	BST_EN7	BST_EN6	BST_EN5	BST_EN4	BST_EN3	BST_EN2	BST_EN1	BST_EN0
0x0B	BUCK_SEQ	0					BUCK_SEQ		
0x0C	LDO12_SEQ	0		LDO2_SEQ			LDO1_SEQ		
0x0D	LDO34_SEQ	0		LDO4_SEQ			LDO3_SEQ		
0x0E	SEQUENCING	SEQ_SPEED		SEQ_CONTROL		SEQ_ON	SEQ_COUNT		
0x0F	DISCHARGE	BUCK_LOAD	BOOST_LOAD	LDO4_DIS	LDO3_DIS	LDO2_DIS	LDO1_DIS	BOOST_DIS	BUCK_DIS
0x10	RESET	0	SOFT_RESET				0		FLT_SD_B
0x11	INTERRUPT1	LDO4_OVP_INT	LDO3_OVP_INT	LDO2_OVP_INT	LDO1_OVP_INT	LDO4_UVP_INT	LDO3_UVP_INT	LDO2_UVP_INT	LDO1_UVP_INT
0x12	INTERRUPT2	BST_OVP_INT	BUCK_OVP_INT	BST_UVP_INT	BUCK_UVP_INT	LDO4_OCP_INT	LDO3_OCP_INT	LDO2_OCP_INT	LDO1_OCP_INT
0x13	INTERRUPT3	BST_IPK_INT	BUCK_IPK_INT	APVIN_UVLO_INT	LDO12_UVLO_INT	LDO3_UVLO_INT	LDO4_UVLO_INT	TSD_INT	TSD_WRN_INT
0x14	STATUS1	LDO4_OVP_STAT	LDO3_OVP_STAT	LDO2_OVP_STAT	LDO1_OVP_STAT	LDO4_UVP_STAT	LDO3_UVP_STAT	LDO2_UVP_STAT	LDO1_UVP_STAT
0x15	STATUS2	BST_OVP_STAT	BUCK_OVP_STAT	BST_UVP_STAT	BUCK_UVP_STAT	LDO4_OCP_STAT	LDO3_OCP_STAT	LDO2_OCP_STAT	LDO1_OCP_STAT
0x16	STATUS3	BST_IPK_STAT	BUCK_IPK_STAT	APVIN_UVLO_STAT	LDO12_UVLO_STAT	LDO3_UVLO_STAT	LDO4_UVLO_STAT	TSD_STAT	TSD_WRN_STAT

Table 14. REGISTER MAPPING

					Read Only	Write Only	Read / Write	Read / Clear	Write / Clear
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x17	MINT1	MASK_LD-O4_OVP	MASK_LD-O3_OVP	MASK_LDO 2_OVP	MASK_LDO 1_OVP	MASK_LDO 4_UVP	MASK_LDO 3_UVP	MASK_LD-O2_UVP	MASK_LD-O1_UVP
0x18	MINT2	MASK_BS-T_OVP	MASK_BU-CK_OVP	MASK_BST _UVP	MASK_BUC-K_UVP	MASK_LDO 4_OCP	MASK_LDO 3_OCP	MASK_LD-O2_OCP	MASK_LD-O1_OCP
0x19	MINT3	MASK_BS-T_IPK	MASK_BU-CK_IPK	MASK_APVI-N_UVLO	MASK_LDO 12_UVLO	MASK_LDO 3_UVLO	MASK_LDO 4_UVLO	MASK_TS-D	MASK_TS-D_WRN
0x1A	STATUS4	0	CHIP_SUS-D	BOOST_SU-SD	BUCK_SUS-D	LDO4_SUS-D	LDO3_SUS-D	LDO2_SU-SD	LDO1_SU-SD

REGISTER DETAILS

Table 15. REGISTER DETAILS – 0x00 PRODUCT ID

<table>
<tr><th colspan="4">0x00 PRODUCT ID</th><th colspan="2">Default = 00000001</th></tr>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="19">7:00</td><td rowspan="19">Product ID</td><td rowspan="19">00000001</td><td rowspan="19">Read</td><td colspan="2">Allows customers to identify manufacturer and version</td></tr>
<tr><td colspan="2">Product ID Table</td></tr>
<tr><td>Code</td><td>Product</td></tr>
<tr><td>0</td><td>–</td></tr>
<tr><td>1</td><td>FAN53880</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
<tr><td>100</td><td>Reserved</td></tr>
<tr><td>101</td><td>Reserved</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
<tr><td>1000</td><td>Reserved</td></tr>
<tr><td>1001</td><td>Reserved</td></tr>
<tr><td>1010</td><td>Reserved</td></tr>
<tr><td>1011</td><td>Reserved</td></tr>
<tr><td>1100</td><td>Reserved</td></tr>
<tr><td>1101</td><td>Reserved</td></tr>
<tr><td>1110</td><td>Reserved</td></tr>
<tr><td>1111</td><td>Reserved</td></tr>
</table>

Table 16. REGISTER DETAILS – 0x01 SILICON REV ID

<table>
<tr><th colspan="4">0x01 SILICON REV ID</th><th colspan="2">Default = See Description</th></tr>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">7:0</td><td rowspan="4">Revision</td><td rowspan="4">See Description</td><td rowspan="4">Read</td><td colspan="2">Provides the silicon revision</td></tr>
<tr><td>Part Number</td><td>REG 01 [7:0] Silicon Rev ID</td></tr>
<tr><td>FAN53880UC001X</td><td>00000011</td></tr>
<tr><td>FAN53880UC002X</td><td>00000100</td></tr>
</table>

Table 17. REGISTER DETAILS – 0x02 BUCK

<table>
<tr><th colspan="4">0x02 BUCK</th><th colspan="4">Default = 00000000</th></tr>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th colspan="4">Description</th></tr>
<tr><td rowspan="14">7:00</td><td rowspan="14">BUCK_OUT</td><td rowspan="14">00000000</td><td rowspan="14">R/W</td><td colspan="4">Buck programming steps are 12.5 mV with a range of 0.6 to 3.3 V. Vout = [0.0125 x (d−31)] + 0.6; Where “d” is the decimal value of the register.</td></tr>
<tr><th>Hex</th><th>V_{OUT}</th><th>Hex</th><th>V_{OUT}</th></tr>
<tr><td>0</td><td>DEFAULT</td><td>28</td><td>0.7125V</td></tr>
<tr><td>01 −1E</td><td>Reserved</td><td>29−F6</td><td>............</td></tr>
<tr><td>1F</td><td>0.6000V</td><td>F0</td><td>3.2125V</td></tr>
<tr><td>20</td><td>0.6125V</td><td>F1</td><td>3.2250V</td></tr>
<tr><td>21</td><td>0.6250V</td><td>F2</td><td>3.2375V</td></tr>
<tr><td>22</td><td>0.6375V</td><td>F3</td><td>3.2500V</td></tr>
<tr><td>23</td><td>0.6500V</td><td>F4</td><td>3.2625V</td></tr>
<tr><td>24</td><td>0.6625V</td><td>F5</td><td>3.2750V</td></tr>
<tr><td>25</td><td>0.6750V</td><td>F6</td><td>3.2875V</td></tr>
<tr><td>26</td><td>0.6875V</td><td>F7</td><td>3.3000V</td></tr>
<tr><td>27</td><td>0.7000V</td><td>F8−FF</td><td>Reserved</td></tr>
</table>

Table 18. REGISTER DETAILS – 0x03 BOOST

0x03 BOOST				Default = 00000000							
Bit	Name	Default	Type	Description							
7	BST_PASS	0	R/W								
6:0	BOOST_VOUT	0000000	R/W	The boost output voltage is programmable in the 25 mV steps. Equation: V_{OUT} = 3.000 + (d−4)*0.025V; where “d” is the decimal value.							
				Hex	V_{OUT}	Hex	V_{OUT}	Hex	V_{OUT}	Hex	V_{OUT}
				0	DEFAULT	20	3.700V	40	4.500V	60	5.300V
				1	Reserved	21	3.725V	41	4.525V	61	5.325V
				2	Reserved	22	3.750V	42	4.550V	62	5.350V
				3	Reserved	23	3.775V	43	4.575V	63	5.375V
				4	3.000V	24	3.800V	44	4.600V	64	5.400V
				5	3.025V	25	3.825V	45	4.625V	65	5.425V
				6	3.050V	26	3.850V	46	4.650V	66	5.450V
				7	3.075V	27	3.875V	47	4.675V	67	5.475V
				8	3.100V	28	3.900V	48	4.700V	68	5.500V
				9	3.125V	29	3.925V	49	4.725V	69	5.525V
				0A	3.150V	2A	3.950V	4A	4.750V	6A	5.550V
				0B	3.175V	2B	3.975V	4B	4.775V	6B	5.575V
				0C	3.200V	2C	4.000V	4C	4.800V	6C	5.600V
				0D	3.225V	2D	4.025V	4D	4.825V	6D	5.625V
				0E	3.250V	2E	4.050V	4E	4.850V	6E	5.650V
				0F	3.275V	2F	4.075V	4F	4.875V	6F	5.675V
				10	3.300V	30	4.100V	50	4.900V	70	5.700V
				11	3.325V	31	4.125V	51	4.925V	71–7F	Reserved
				12	3.350V	32	4.150V	52	4.950V		
				13	3.375V	33	4.175V	53	4.975V		
				14	3.400V	34	4.200V	54	5.000V		
				15	3.425V	35	4.225V	55	5.025V		
				16	3.450V	36	4.250V	56	5.050V		
				17	3.475V	37	4.275V	57	5.075V		
				18	3.500V	38	4.300V	58	5.100V		
				19	3.525V	39	4.325V	59	5.125V		
				1A	3.550V	3A	4.350V	5A	5.150V		
				1B	3.575V	3B	4.375V	5B	5.175V		
				1C	3.600V	3C	4.400V	5C	5.200V		
				1D	3.625V	3D	4.425V	5D	5.225V		
				1E	3.650V	3E	4.450V	5E	5.250V		
				1F	3.675V	3F	4.475V	5F	5.275V		

Table 19. REGISTER DETAILS – 0x04 LDO1

0x04 LDO1				Default = 00000000			
Bit	**Name**	**Default**	**Type**	**Description**			
6:0	LDO1_VOUT	0000000	R/W	Sets LDO1 regulation target voltage.			
				Equation: Vout = 0.800V + [(d−15)*25mV]; Where d is the decimal value of the register			
				Hex	**V_{OUT}**	**Hex**	**V_{OUT}**
				0	DEFAULT	40	2.025V
				1	Reserved	41	2.050V
				2	Reserved	42	2.075V
				3	Reserved	43	2.100V
				4	Reserved	44	2.125V
				5	Reserved	45	2.150V
				6	Reserved	46	2.175V
				7	Reserved	47	2.200V
				8	Reserved	48	2.225V
				9	Reserved	49	2.250V
				0A	Reserved	4A	2.275V
				0B	Reserved	4B	2.300V
				0C	Reserved	4C	2.325V
				0D	Reserved	4D	2.350V
				0E	Reserved	4E	2.375V
				0F	0.800V	4F	2.400V
				10	0.825V	50	2.425V
				11	0.850V	51	2.450V
				12	0.875V	52	2.475V
				13	0.900V	53	2.500V
				14	0.925V	54	2.525V
				15	0.950V	55	2.550V
				16	0.975V	56	2.575V
				17	1.000V	57	2.600V
				18	1.025V	58	2.625V
				19	1.050V	59	2.650V
				1A	1.075V	5A	2.675V
				1B	1.100V	5B	2.700V
				1C	1.125V	5C	2.725V
				1D	1.150V	5D	2.750V
				1E	1.175V	5E	2.775V
				1F	1.200V	5F	2.800V
				20	1.225V	60	2.825V
				21	1.250V	61	2.850V
				22	1.275V	62	2.875V
				23	1.300V	63	2.900V
				24	1.325V	64	2.925V

Table 19. REGISTER DETAILS – 0x04 LDO1

0x04 LDO1				Default = 00000000			
Bit	Name	Default	Type	Description			
				25	1.350V	65	2.950V
				26	1.375V	66	2.975V
				27	1.400V	67	3.000V
				28	1.425V	68	3.025V
				29	1.450V	69	3.050V
				2A	1.475V	6A	3.075V
				2B	1.500V	6B	3.100V
				2C	1.525V	6C	3.125V
				2D	1.550V	6D	3.150V
				2E	1.575V	6E	3.175V
				2F	1.600V	6F	3.200V
				30	1.625V	70	3.225V
				31	1.650V	71	3.250V
				32	1.675V	72	3.275V
				33	1.700V	73	3.300V
				34	1.725V	74	Reserved
				35	1.750V	75	Reserved
				36	1.775V	76	Reserved
				37	1.800V	77	Reserved
				38	1.825V	78	Reserved
				39	1.850V	79	Reserved
				3A	1.875V	7A	Reserved
				3B	1.900V	7B	Reserved
				3C	1.925V	7C	Reserved
				3D	1.950V	7D	Reserved
				3E	1.975V	7E	Reserved
				3F	2.000V	7F	Reserved

Table 20. REGISTER DETAILS − 0x05 LDO2

0x05 LDO2				Default = 00000000			
Bit	**Name**	**Default**	**Type**	**Description**			
7	UNUSED						
6:0	LDO2_VOUT	0000000	R/W	Sets LDO2 regulation target voltage.			
				Equation: Vout = 0.800V + [(d−15)*25mV]; Where d is the decimal value of the register			
				Hex	**V_{OUT}**	**Hex**	**V_{OUT}**
				0	DEFAULT	40	2.025V
				1	Reserved	41	2.050V
				2	Reserved	42	2.075V
				3	Reserved	43	2.100V
				4	Reserved	44	2.125V
				5	Reserved	45	2.150V
				6	Reserved	46	2.175V
				7	Reserved	47	2.200V
				8	Reserved	48	2.225V
				9	Reserved	49	2.250V
				0A	Reserved	4A	2.275V
				0B	Reserved	4B	2.300V
				0C	Reserved	4C	2.325V
				0D	Reserved	4D	2.350V
				0E	Reserved	4E	2.375V
				0F	0.800V	4F	2.400V
				10	0.825V	50	2.425V
				11	0.850V	51	2.450V
				12	0.875V	52	2.475V
				13	0.900V	53	2.500V
				14	0.925V	54	2.525V
				15	0.950V	55	2.550V
				16	0.975V	56	2.575V
				17	1.000V	57	2.600V
				18	1.025V	58	2.625V
				19	1.050V	59	2.650V
				1A	1.075V	5A	2.675V
				1B	1.100V	5B	2.700V
				1C	1.125V	5C	2.725V
				1D	1.150V	5D	2.750V
				1E	1.175V	5E	2.75V
				1F	1.200V	5F	2.800V
				20	1.225V	60	2.825V
				21	1.250V	61	2.850V
				22	1.275V	62	2.875V
				23	1.300V	63	2.900V

Table 20. REGISTER DETAILS – 0x05 LDO2

0x05 LDO2				Default = 00000000			
Bit	**Name**	**Default**	**Type**	**Description**			
				24	1.325V	64	2.925V
				25	1.350V	65	2.950V
				26	1.375V	66	2.975V
				27	1.400V	67	3.000V
				28	1.425V	68	3.025V
				29	1.450V	69	3.050V
				2A	1.475V	6A	3.075V
				2B	1.500V	6B	3.100V
				2C	1.525V	6C	3.125V
				2D	1.550V	6D	3.150V
				2E	1.575V	6E	3.175V
				2F	1.600V	6F	3.200V
				30	1.625V	70	3.225V
				31	1.650V	71	3.250V
				32	1.675V	72	3.275V
				33	1.700V	73	3.300V
				34	1.725V	74	Reserved
				35	1.750V	75	Reserved
				36	1.775V	76	Reserved
				37	1.800V	77	Reserved
				38	1.825V	78	Reserved
				39	1.850V	79	Reserved
				3A	1.875V	7A	Reserved
				3B	1.900V	7B	Reserved
				3C	1.925V	7C	Reserved
				3D	1.950V	7D	Reserved
				3E	1.975V	7E	Reserved
				3F	2.000V	7F	Reserved

Table 21. REGISTER DETAILS – 0x06 LDO3

0x06 LDO3				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7	UNUSED			
6:0	LDO3_VOUT	0000000	R/W	Sets LDO3 regulation target voltage.
				Equation: Vout = 0.800V + [(d−15)*25mV]; Where d is the decimal value of the register

Hex	V_{OUT}	Hex	V_{OUT}
0	DEFAULT	40	2.025V
1	Reserved	41	2.050V
2	Reserved	42	2.075V
3	Reserved	43	2.100V
4	Reserved	44	2.125V
5	Reserved	45	2.150V
6	Reserved	46	2.175V
7	Reserved	47	2.200V
8	Reserved	48	2.225V
9	Reserved	49	2.250V
0A	Reserved	4A	2.275V
0B	Reserved	4B	2.300V
0C	Reserved	4C	2.325V
0D	Reserved	4D	2.350V
0E	Reserved	4E	2.375V
0F	0.800V	4F	2.400V
10	0.825V	50	2.425V
11	0.850V	51	2.450V
12	0.875V	52	2.475V
13	0.900V	53	2.500V
14	0.925V	54	2.525V
15	0.950V	55	2.550V
16	0.975V	56	2.575V
17	1.000V	57	2.600V
18	1.025V	58	2.625V
19	1.050V	59	2.650V
1A	1.075V	5A	2.675V
1B	1.100V	5B	2.700V
1C	1.125V	5C	2.725V
1D	1.150V	5D	2.750V
1E	1.175V	5E	2.75V
1F	1.200V	5F	2.800V
20	1.225V	60	2.825V
21	1.250V	61	2.850V
22	1.275V	62	2.875V
23	1.300V	63	2.900V

Table 21. REGISTER DETAILS – 0x06 LDO3

0x06 LDO3				Default = 00000000			
Bit	Name	Default	Type	Description			
				24	1.325V	64	2.925V
				25	1.350V	65	2.950V
				26	1.375V	66	2.975V
				27	1.400V	67	3.000V
				28	1.425V	68	3.025V
				29	1.450V	69	3.050V
				2A	1.475V	6A	3.075V
				2B	1.500V	6B	3.100V
				2C	1.525V	6C	3.125V
				2D	1.550V	6D	3.150V
				2E	1.575V	6E	3.175V
				2F	1.600V	6F	3.200V
				30	1.625V	70	3.225V
				31	1.650V	71	3.250V
				32	1.675V	72	3.275V
				33	1.700V	73	3.300V
				34	1.725V	74	Reserved
				35	1.750V	75	Reserved
				36	1.775V	76	Reserved
				37	1.800V	77	Reserved
				38	1.825V	78	Reserved
				39	1.850V	79	Reserved
				3A	1.875V	7A	Reserved
				3B	1.900V	7B	Reserved
				3C	1.925V	7C	Reserved
				3D	1.950V	7D	Reserved
				3E	1.975V	7E	Reserved
				3F	2.000V	7F	Reserved

Table 22. REGISTER DETAILS − 0x07 LDO4

0x07 LDO4				Default = 00000000			
Bit	**Name**	**Default**	**Type**	**Description**			
7	UNUSED						
6:0	LDO4_VOUT	0000000	R/W	Sets LDO4 regulation target voltage.			
				Equation: Vout = 0.800V + [(d−15)*25mV]; Where d is the decimal value of the register			
				Hex	**V_{OUT}**	**Hex**	**V_{OUT}**
				0	DEFAULT	40	2.025V
				1	Reserved	41	2.050V
				2	Reserved	42	2.075V
				3	Reserved	43	2.100V
				4	Reserved	44	2.125V
				5	Reserved	45	2.150V
				6	Reserved	46	2.175V
				7	Reserved	47	2.200V
				8	Reserved	48	2.225V
				9	Reserved	49	2.250V
				0A	Reserved	4A	2.275V
				0B	Reserved	4B	2.300V
				0C	Reserved	4C	2.325V
				0D	Reserved	4D	2.350V
				0E	Reserved	4E	2.375V
				0F	0.800V	4F	2.400V
				10	0.825V	50	2.425V
				11	0.850V	51	2.450V
				12	0.875V	52	2.475V
				13	0.900V	53	2.500V
				14	0.925V	54	2.525V
				15	0.950V	55	2.550V
				16	0.975V	56	2.575V
				17	1.000V	57	2.600V
				18	1.025V	58	2.625V
				19	1.050V	59	2.650V
				1A	1.075V	5A	2.675V
				1B	1.100V	5B	2.700V
				1C	1.125V	5C	2.725V
				1D	1.150V	5D	2.750V
				1E	1.175V	5E	2.75V
				1F	1.200V	5F	2.800V
				20	1.225V	60	2.825V
				21	1.250V	61	2.850V
				22	1.275V	62	2.875V
				23	1.300V	63	2.900V

Table 22. REGISTER DETAILS – 0x07 LDO4

0x07 LDO4				Default = 00000000			
Bit	**Name**	**Default**	**Type**	**Description**			
				24	1.325V	64	2.925V
				25	1.350V	65	2.950V
				26	1.375V	66	2.975V
				27	1.400V	67	3.000V
				28	1.425V	68	3.025V
				29	1.450V	69	3.050V
				2A	1.475V	6A	3.075V
				2B	1.500V	6B	3.100V
				2C	1.525V	6C	3.125V
				2D	1.550V	6D	3.150V
				2E	1.575V	6E	3.175V
				2F	1.600V	6F	3.200V
				30	1.625V	70	3.225V
				31	1.650V	71	3.250V
				32	1.675V	72	3.275V
				33	1.700V	73	3.300V
				34	1.725V	74	Reserved
				35	1.750V	75	Reserved
				36	1.775V	76	Reserved
				37	1.800V	77	Reserved
				38	1.825V	78	Reserved
				39	1.850V	79	Reserved
				3A	1.875V	7A	Reserved
				3B	1.900V	7B	Reserved
				3C	1.925V	7C	Reserved
				3D	1.950V	7D	Reserved
				3E	1.975V	7E	Reserved
				3F	2.000V	7F	Reserved

Table 23. REGISTER DETAILS – 0x08 IOUT

0x08 IOUT				Default = 01010101	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO4_ILIM	1	R/W	Reset condition: –	
				Code	**Current Limit**
				0	150 mA (minimum)
				1	360 mA (minimum)
5	UNUSED				
4	LDO3_ILIM	1	R/W	**Code**	**Current Limit**
				0	150 mA (minimum)
				1	360 mA (minimum)
3	UNUSED				
2	LDO2_ILIM	1	R/W	**Code**	**Current Limit**
				0	150 mA (minimum)
				1	360 mA (minimum)
1	UNUSED				
0	LDO1_ILIM	1	R/W	**Code**	**Current Limit**
				0	150 mA (minimum)
				1	360 mA (minimum)

Table 24. REGISTER DETAILS – 0x09 ENABLE

0x09 ENABLE				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	BST_MODE	0	R/W	**Code**	**Effect**
				0	Automatically select between PFM and PWM Modes
				1	Forced PWM mode.
6	BUCK_MODE	0	R/W	**Code**	**Effect**
				0	Auto selection between PFM and PWM modes
				1	Forced PWM mode
5	UNUSED				
4	BUCK_EN	0	R/W	Enable bit for the BUCK. This bit only controls the state of the BUCK if BUCK_SEQ = 000.	
				Code	**Status of Buck**
				0	Disabled
				1	Enabled
3	LDO4_EN	0	R/W	Enable bit for LDO4. This bit only controls the state of the LDO if LDO4_SEQ = 000.	
				Code	**Status of LDO4**
				0	Disabled
				1	Enabled

Table 24. REGISTER DETAILS – 0x09 ENABLE

0x09 ENABLE				Default = 00000000	
Bit	Name	Default	Type	Description	
2	LDO3_EN	0	R/W	Enable bit for LDO3. This bit only controls the state of the LDO if LDO3_SEQ = 000.	
				Code	**Status of LDO3**
				0	Disabled
				1	Enabled
1	LDO2_EN	0	R/W	Enable bit for LDO2. This bit only controls the state of the LDO if LDO2_SEQ = 000.	
				Code	**Status of LDO2**
				0	Disabled
				1	Enabled
0	LDO1_EN	0	R/W	Enable bit for LDO1. This bit only controls the state of the LDO if LDO1_SEQ = 000.	
				Code	**Status of LDO1**
				0	Disabled
				1	Enabled

Table 25. REGISTER DETAILS – 0x0A BOOST_ENABLE

0x0A BOOST_ENABLE				Default = 00000000	
Bit	Name	Default	Type	Description	
7	BST_EN7	0	R/W	BST_EN7 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Disabled
				1	Enabled
6	BST_EN6	0	R/W	BST_EN6 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Disabled
				1	Enabled
5	BST_EN5	0	R/W	BST_EN5 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Disabled
				1	Enabled
4	BST_EN4	0	R/W	BST_EN4 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Disabled
				1	Enabled
3	BST_EN3	0	R/W	BST_EN3 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Diabled
				1	Enabled

Table 25. REGISTER DETAILS – 0x0A BOOST_ENABLE

0x0A BOOST_ENABLE				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
2	BST_EN2	0	R/W	BST_EN2 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Disabled
				1	Enabled
1	BST_EN1	0	R/W	BST_EN1 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Disabled
				1	Enabled
0	BST_EN0	0	R/W	BST_EN0 bit is for enabling the boost converter.	
				Code	**Effect**
				0	Disabled
				1	Ensabled

Table 26. REGISTER DETAILS – 0x0B BUCK_SEQ

0x0B BUCK_SEQ				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:3	UNUSED				
2:0	BUCK_SEQ	000	R/W	The buck sequencing is selected by setting bits [2:0]	
				Code	**Effect**
				000	Controlled through I2C by setting the buck_en bit.
				001	Selects slot 1 for the buck to be enabled in at power up.
				010	Selects slot 2 for the buck to be enabled in at power up.
				011	Selects slot 3 for the buck to be enabled in at power up.
				100	Selects slot 4 for the buck to be enabled in at power up.
				101	Selects slot 5 for the buck to be enabled in at power up.
				110	Selects slot 6 for the buck to be enabled in at power up.
				111	Selects slot 7 for the buck to be enabled in at power up.

Table 27. REGISTER DETAILS – 0x0C LDO12_SEQ

0x0C LDO12_SEQ				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:6	UNUSED				
5:3	LDO2_SEQ	000	R/W	The LDO2 sequencing is selected by setting bits [2:0]	
				Code	**Effect**
				000	Controlled through I2C by setting the LDO2_EN bit.
				001	Selects slot 1 for the LDO2 to be enabled in at power up.
				010	Selects slot 2 for the LDO2 to be enabled in at power up.
				011	Selects slot 3 for the LDO2 to be enabled in at power up.
				100	Selects slot 4 for the LDO2 to be enabled in at power up.
				101	Selects slot 5 for the LDO2 to be enabled in at power up.
				110	Selects slot 6 for the LDO2 to be enabled in at power up.
				111	Selects slot 7 for the LDO2 to be enabled in at power up.
2:0	LDO1_SEQ	000	R/W	The LDO1 sequencing is selected by setting bits [2:0]	
				Code	**Effect**
				000	Controlled through I2C by setting the LDO1_EN bit.
				001	Selects slot 1 for the LDO1 to be enabled in at power up.
				010	Selects slot 2 for the LDO1 to be enabled in at power up.
				011	Selects slot 3 for the LDO1 to be enabled in at power up.
				100	Selects slot 4 for the LDO1 to be enabled in at power up.
				101	Selects slot 5 for the LDO1 to be enabled in at power up.
				110	Selects slot 6 for the LDO1 to be enabled in at power up.
				111	Selects slot 7 for the LDO1 to be enabled in at power up.

Table 28. REGISTER DETAILS – 0x0D LDO34_SEQ

0x0D LDO34_SEQ				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:6	UNUSED				
5:3	LDO4_SEQ	000	R/W	The LDO4 sequencing is selected by setting bits [2:0]	
				Code	**Effect**
				000	Controlled through I2C by setting the LDO4_EN bit.
				001	Selects slot 1 for the LDO4 to be enabled in at power up.
				010	Selects slot 2 for the LDO4 to be enabled in at power up.
				011	Selects slot 3 for the LDO4 to be enabled in at power up.
				100	Selects slot 4 for the LDO4to be enabled in at power up.
				101	Selects slot 5 for the LDO4 to be enabled in at power up.
				110	Selects slot 6 for the LDO4 to be enabled in at power up.
				111	Selects slot 7 for the LDO4 to be enabled in at power up.
2:0	LDO3_SEQ	000	R/W	The LDO3 sequencing is selected by setting bits [2:0]	
				Code	**Effect**
				000	Controlled through I2C by setting the LDO3_EN bit.
				001	Selects slot 1 for the LDO3 to be enabled in at power up.
				010	Selects slot 2 for the LDO3 to be enabled in at power up.
				011	Selects slot 3 for the LDO3 to be enabled in at power up.
				100	Selects slot 4 for the LDO3 to be enabled in at power up.
				101	Selects slot 5 for the LDO3 to be enabled in at power up.
				110	Selects slot 6 for the LDO3 to be enabled in at power up.
				111	Selects slot 7 for the LDO3 to be enabled in at power up.

Table 29. REGISTER DETAILS – 0x0E SEQUENCING

0x0E SEQUENCING				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:6	SEQ_SPEED	00	R/W	**Code**	**Period per Slot**
				00	500 μs
				01	1.0 ms
				10	1.5 ms
				11	2.0 ms
5:4	SEQ_CONTROL	00	W1CLR	**Code**	**Effect**
				00	Default
				01	Starts a converter power up sequence.
				10	Starts a converter shutdown sequence.
				11	Bit configuration is ignored
				Note: The bits will always clear immediately when written to and always readback 00.	
3	SEQ_ON	0	Read	**Code**	**Effect**
				0	Indicates that the sequencing is not in process
				1	Indicates that the sequencing is executing and somewhere between the start of slot 1 and the end of slot 7. The bit remains a 1 until slot 7 has completed at start−up or slot 1 has finished at shutdown, regardless of what slots are used.
				This bit is a read only status bit to indicate the sequencing is on.	
2:0	SEQ_COUNT	000	Read	**Code**	**Slot**
				000	Indicates sequencing has completed or not started.
				001	Indicates was in slot 1 during register read
				010	Indicates was in slot 2 during register read
				011	Indicates was in slot 3 during register read
				100	Indicates was in slot 4 during register read
				101	Indicates was in slot 5 during register read
				110	Indicates was in slot 6 during register read
				111	Indicates was in slot 7 during register read
				These register bits provide the status of the sequencing.	

Table 30. REGISTER DETAILS – 0x0F DISCHARGE

0x0F DISCHARGE				Default = 00111111	
Bit	**Name**	**Default**	**Type**	**Description**	
7	BUCK_LOAD	0	R/W	**Code**	**Effect**
				0	Buck internal load is removed from output.
				1	Buck internal load is applied to the output during PFM operation.
6	BOOST_LOAD	0	R/W	**Code**	**Effect**
				0	Boost internal load is removed from output.
				1	Boost internal load is applied to the output during PFM operation.
5	LDO4_DIS	1	R/W	**Code**	**Effect**
				0	LDO4 Active Discharge feature is disabled. Pull down will not be activated when LDO4 is disabled by any event.
				1	LDO4 Active Discharge feature is enabled. Pull down will be activated when LDO4 is disabled by HWEN going low or LDO4_EN = 0 or a Sequenced shutdown or in an OVP event.
4	LDO3_DIS	1	R/W	**Code**	**Effect**
				0	LDO3 Active Discharge feature is disabled. Pull down will not be activated when LDO3 is disabled by any event.
				1	LDO3 Active Discharge feature is enabled. Pull down will be activated when LDO3 is disabled by HWEN going low or LDO3_EN = 0 or a Sequenced shutdown or in an OVP event.
3	LDO2_DIS	1	R/W	**Code**	**Effect**
				0	LDO2 Active Discharge feature is disabled. Pull down will not be activated when LDO2 is disabled by any event.
				1	LDO2 Active Discharge feature is enabled. Pull down will be activated when LDO2 is disabled by HWEN going low or LDO2_EN = 0 or a Sequenced shutdown or in an OVP event.
2	LDO1_DIS	1	R/W	**Code**	**Effect**
				0	LDO1 Active Discharge feature is disabled. Pull down will not be activated when LDO1 is disabled by any event.
				1	LDO1 Active Discharge feature is enabled. Pull down will be activated when LDO1 is disabled by HWEN going low or LDO1_EN = 0 or a Sequenced shutdown or in an OVP event.
1	BOOST_DIS	1	R/W	**Code**	**Effect**
				0	Boost Active Discharge feature is disabled. Pull down will not be activated when Boost is disabled by any event.
				1	Boost Active Discharge is enabled and output is discharged by internal resistor when the Boost is disabled by BSTEN going low or BST_EN0 = 0 or in an OVP event.
0	BUCK_DIS	1	R/W	**Code**	**Effect**
				0	Buck Active Discharge feature is disabled. Pull down will not be activated when Buck is disabled by any event.
				1	Buck Active Discharge feature is enabled. Pull down will be activated when Buck is disabled by HWEN going low or BUCK_EN = 0 or a Sequenced shutdown or in an OVP event.

Table 31. REGISTER DETAILS – 0x10 RESET

<table>
<tr><th colspan="4">0x10 RESET</th><th colspan="2">Default = 00000000</th></tr>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>UNUSED</td><td></td><td></td><td colspan="2"></td></tr>
<tr><td rowspan="4">6:3</td><td rowspan="4">SOFT_RESET</td><td rowspan="4">0000</td><td rowspan="4">Write</td><td colspan="2">Reset condition: 0</td></tr>
<tr><td>Code</td><td>Effect</td></tr>
<tr><td>1011</td><td>Writing a “1011” begins a soft reset of the device I2C registers to their default values. This bit is cleared upon execution of the Reset function.</td></tr>
<tr><td></td><td>Any other value than “1011” will be ignored.</td></tr>
<tr><td>2:1</td><td>UNUSED</td><td></td><td></td><td colspan="2"></td></tr>
<tr><td rowspan="4">0</td><td rowspan="4">FLT_SD_B</td><td rowspan="4">0</td><td rowspan="4">R/W</td><td>Code</td><td>Effect</td></tr>
<tr><td>0</td><td>Converter is shutdown if an OVP, UVP or OCP event occurs.</td></tr>
<tr><td>1</td><td>Converter is not shutdown if an OVP, UVP or OCP event occurs.</td></tr>
<tr><td colspan="2">Notes:
– If this bit function is desired, FLT_SD_B should be set to “1” prior to enabling any converters after a Power−On−Reset
– If a hard short occurs on either the buck or boost output, the converter will shutdown to protect itself even if the FLT_SD_B bit is set to “1”.</td></tr>
</table>

Table 32. REGISTER DETAILS − 0x11 INTERRUPT1

0x11 INTERRUPT1				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	LDO4_OVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Voltage event detected on LDO4 output or the voltage has fallen below the OVP_Falling threshold.
6	LDO3_OVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over Voltage event detected on LDO3 output or the voltage has fallen below the OVP_Falling threshold.
5	LDO2_OVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Voltage event detected on LDO2 output or the voltage has fallen below the OVP_Falling threshold.
4	LDO1_OVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Voltage event detected on LDO1 output or the voltage has fallen below the OVP_Falling threshold.
3	LDO4_UVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Under−Voltage event detected on LDO4 output or the voltage has risen above the UVP_Rising threshold.
2	LDO3_UVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Under−Voltage event detected on the output of LDO3 or the voltage has risen above the UVP_Rising threshold.
1	LDO2_UVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Under−Voltage event detected on LDO2 output or the voltage has risen above the UVP_Rising threshold.
0	LDO1_UVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Under−Voltage event detected on LDO1 output or the voltage has risen above the UVP_Rising threshold.

Table 33. REGISTER DETAILS – 0x12 INTERRUPT2

0x12 INTERRUPT2				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	BST_OVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Voltage event detected on the Boost output or the voltage has fallen below the OVP_Falling threshold.
6	BUCK_OVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Voltage event detected on the Buck output or the voltage has fallen below the OVP_Falling threshold.
5	BST_UVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Under−Voltage event detected on on the Boost output or the voltage has risen above the UVP_Rising threshold.
4	BUCK_UVP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Under−Voltage event detected on on the Buck output or the voltage has risen above the UVP_Rising threshold.
3	LDO4_OCP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Current event detected on LDO4 output or that a successful restart has occurred after an OCP event.
2	LDO3_OCP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Current event detected on LDO3 output or that a successful restart has occurred after an OCP event.
1	LDO2_OCP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Current event detected on LDO2 output or that a successful restart has occurred after an OCP event.
0	LDO1_OCP_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Over−Current event detected on LDO1 output or that a successful restart has occurred after an OCP event.

Table 34. REGISTER DETAILS – 0x13 INTERRUPT3

0x13 INTERRUPT3				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	BST_IPK_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Boost Peak Current limit reached or the Boost successfully completed a restart after a Peak Current fault.
6	BUCK_IPK_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Buck Peak Current reached or the Buck successfully completed a restart after a Peak Current fault.
5	APVIN_UVLO_INT	0	R/CLR	**Code**	**Effect**
				0	Normal operation
				1	Indicates that the AV_{IN} and/or PV_{IN} power fell below the UVLO input threshold or that the supplies have risen above the rising thresholds after a UVLO fault.
				Reading the the associated status bit provides present state of the input voltage.	
4	LDO12_UVLO_INT	0	R/CLR	**Code**	**Effect**
				0	Normal operation
				1	Indicates V_{IN12} fell below the UVLO threshold while LDO1 and/or LDO2 are enabled or that the supply has risen above the rising thresholds after a UVLO fault.
				Reading the the associated status bit provides present state of the input voltage.	
3	LDO3_UVLO_INT	0	R/CLR	**Code**	Effect
				0	Normal Operation
				1	Indicates that the V_{IN3} fell below the UVLO threshold while LDO3 was enabled or that the supply has risen above the rising thresholds after a UVLO fault.
				Reading the the associated status bit provides present state of the input voltage.	
2	LDO4_UVLO_INT	0	R/CLR	**Code**	**Effect**
				0	Normal Operation
				1	Indicates V_{IN4} fell below the UVLO threshold while LDO4 where enabled or that the supply has risen above the rising thresholds after a UVLO fault.
				Reading the the associated status bit provides present state of the input voltage.	
1	TSD_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	A Thermal Shutdown event detected or that the temperature has fallen below the hysteresis level.
0	TSD_WRN_INT	0	R/CLR	**Code**	**Effect**
				0	Clear
				1	Thermal Shutdown Warning threshold was surpassed or that the temperature has fallen below the hysteresis level.

Table 35. REGISTER DETAILS – 0x14 STATUS1

0x14 STATUS1				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	LDO4_OVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over–Voltage condition exists on LDO4 output
6	LDO3_OVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over–Voltage condition exists on LDO3 output.
5	LDO2_OVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over–Voltage condition exists on LDO2 output
4	LDO1_OVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over–Voltage condition exists on LDO1 output
3	LDO4_UVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Under–Voltage condition exists on LDO4 output.
2	LDO3_UVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Under–Voltage condition exists on the output of LDO3
1	LDO2_UVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Under–Voltage condition exists on LDO2 output
0	LDO1_UVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Under–Voltage condition exists on LDO1 output

Table 36. REGISTER DETAILS – 0x15 STATUS2

0x15 STATUS2				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	BST_OVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over–Voltage condition exists on the Boost output.
6	BUCK_OVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over–Voltage condition exists on the Buck output.
5	BST_UVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Under–Voltage condition exists on the Boost output.

Table 36. REGISTER DETAILS − 0x15 STATUS2

4	BUCK_UVP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Under−Voltage condition exists on the Buck output.
3	LDO4_OCP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over−Current condition exists on LDO4 output
2	LDO3_OCP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over−Current condition exists on LDO3 output
1	LDO2_OCP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over−Current condition exists on LDO2 output
0	LDO1_OCP_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	An Over−Current condition exists on LDO1 output

Table 37. REGISTER DETAILS – 0x16 STATUS3

0x16 STATUS3				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	BST_IPK_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	Boost is hitting the Peak Current limit.
6	BUCK_IPK_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	The Buck is hitting the Peak Current limit
5	APVIN_UVLO_STAT	0	Read	Reset condition: 0	
				Code	**Effect**
				0	Normal Operation
				1	Indicates AV_{IN} and/or PV_{IN} are below the UVLO threshold.
4	LDO12_UVLO_STAT	0	Read	**Code**	**Effect**
				0	Normal Operation
				1	indicates V_{IN12} is below the UVLO threshold while LDO1 and/or LDO2 have been enabled.
3	LDO3_UVLO_STAT	0	Read	**Code**	**Effect**
				0	Normal Operation
				1	Indicates V_{IN3} power rail is below the UVLO threshold while LDO3 is enabled.
2	LDO4_UVLO_STAT	0	Read	**Code**	**Effect**
				0	Normal Operation
				1	Indicates V_{IN4} is below the UVLO threshold while LDO4 is been commanded to be enabled.
1	TSD_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	The device is in thermal shutdown (TSD)
0	TSD_WRN_STAT	0	Read	**Code**	**Effect**
				0	Clear
				1	The temperature is above the Thermal Shutdown Warning threshold and shutdown is impending.

Table 38. REGISTER DETAILS – 0x17 MINT1

0x17 MINT1				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	MASK_LDO4_OVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO4 Over−Voltage interrupt occurs.
6	MASK_LDO3_OVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO3 Over−Voltage interrupt occurs.

Table 38. REGISTER DETAILS – 0x17 MINT1

0x17 MINT1				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
5	MASK_LDO2_OVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO2 Over–Voltage interrupt occurs.
4	MASK_LDO1_OVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO1 Over–Voltage interrupt occurs.
3	MASK_LDO4_UVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO4 Under–Voltage interrupt occurs.
2	MASK_LDO3_UVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO3 Under–Voltage interrupt occurs.
1	MASK_LDO2_UVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO2 Under–Voltage interrupt occurs.
0	MASK_LDO1_UVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO1 Under–Voltage interrupt occurs.

Table 39. REGISTER DETAILS – 0x18 MINT2

0x18 MINT2				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	MASK_BST_OVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when Boost Over–Voltage interrupt occurs.
6	MASK_BUCK_OVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when Buck Over–Voltage interrupt occurs.
5	MASK_BST_UVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when Boost Under–Voltage interrupt occurs.
4	MASK_BUCK_UVP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when Buck Under–Voltage interrupt occurs.

Table 39. REGISTER DETAILS − 0x18 MINT2

0x18 MINT2				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
3	MASK_LDO4_OCP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO4 Over−Current interrupt occurs.
2	MASK_LDO3_OCP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO3 Over−Current interrupt occurs.
1	MASK_LDO2_OCP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO2 Over−Current interrupt occurs.
0	MASK_LDO1_OCP	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when LDO1 Over−Current interrupt occurs.

Table 40. REGISTER DETAILS − 0x19 MINT3

0x19 MINT3				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	MASK_BST_IPK	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when Boost Peak Current limit interrupt occurs.
6	MASK_BUCK_IPK	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when Buck Peak Current limit interrupt occurs.
5	MASK_APVIN_UVLO	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when AV_{IN}/PV_{IN} Input Power Under Voltage interrupt occurs.
4	MASK_LDO12_UVLO	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when V_{IN12} Input Power Under Voltage interrupt occurs.
3	MASK_LDO3_UVLO	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when V_{IN3} Input Power Under Voltage interrupt occurs.
2	MASK_LDO4_UVLO	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when V_{IN4} Input Power Under Voltage interrupt occurs.

Table 40. REGISTER DETAILS – 0x19 MINT3

0x19 MINT3				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
1	MASK_TSD	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB pin is not pulled low when a Thermal Shutdown interrupt occurs.
0	MASK_TSD_WRN	0	R/W	**Code**	**Effect**
				0	No masking of interrupt.
				1	INTB Pin is not pulled low when a Thermal Shutdown Warning interrupt occurs.

Table 41. REGISTER DETAILS – 0x1A STATUS4

0x1A STATUS4				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	CHIP_SUSD	0	Read	**Code**	**Effect**
				0	Chip normal state
				1	The entire chip has been suspended due to a global fault condition.
5	BOOST_SUSD	0	Read	**Code**	**Effect**
				0	Boost normal state
				1	Boost converter has been suspended due to a fault condition.
4	BUCK_SUSD	0	Read	**Code**	**Effect**
				0	Buck in normal state.
				1	Buck converter has been suspended due to a fault condition.
3	LDO4_SUSD	0	Read	**Code**	**Effect**
				0	LDO4 in normal state.
				1	LDO4 converter has been suspended due to a fault condition.
2	LDO3_SUSD	0	Read	**Code**	**Effect**
				0	LDO3 in a normal state
				1	LDO3 converter has been suspended due to a fault condition.
1	LDO2_SUSD	0	Read	**Code**	**Effect**
				0	LDO2 in normal state
				1	LDO2 converter has been suspended due to a fault condition.
0	LDO1_SUSD	0	Read	**Code**	**Effect**
				0	LDO1 is in normal state
				1	LDO1 converter has been suspended due to a fault condition.

APPLICATION CIRCUIT

Application Circuit Diagram

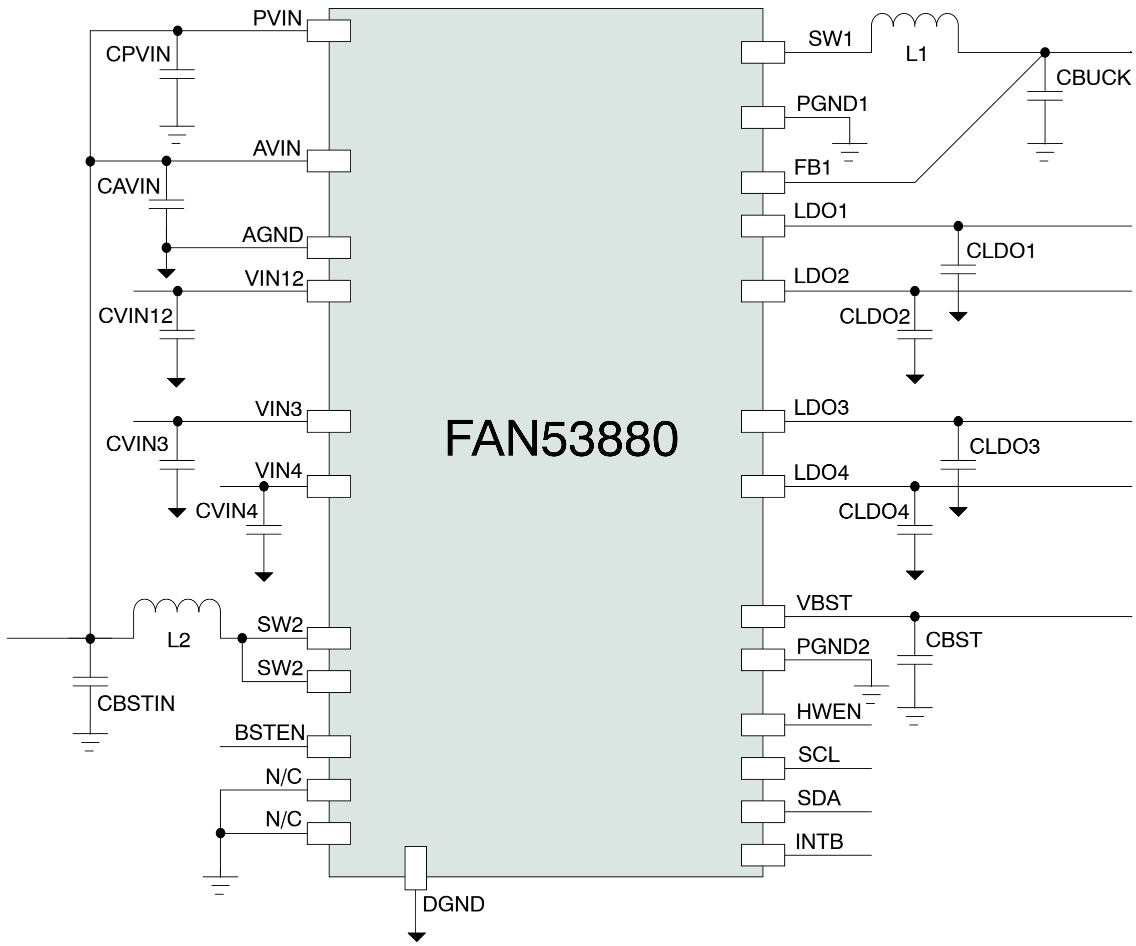


Figure 37. Application Diagram

Application Circuit Components

Table 42. RECOMMENDED EXTERNAL COMPONENTS

Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
C_{PVIN}	TDK	C1005X5R0J106M050BC	10 μF	0402/1005 (1.0mm x 0.5mm)	6.3 V
C_{BUCK}	TDK	C1005X5R0J106M050BC	10 μF	0402/1005 (1.0mm x 0.5mm)	6.3 V
C_{BSTIN}	TDK	C1005X5R0J106M050BC	10 μF	0402/1005 (1.0mm x 0.5mm)	6.3 V
C_{BST}	Murata	GRM188R61A226ME15D	22 μF	0603/1608 (1.6mm x 0.8mm)	10 V
C_{VIN12}, C_{VIN3}, C_{VIN4}	Murata	GRM033R60J225ME47D	2.2 μF	0201/0603 (0.6mm x 0.3mm)	6.3 V
C_{LDO1}, C_{LDO2}, C_{LDO3}, C_{LDO4}	Murata	GRM033R60J225ME47D	2.2 μF	0201/0603 (0.6mm x 0.3mm)	6.3 V
C_{AVIN}	TDK	C1005X5R0J475M	4.7 μF	0402/1005 (1.0mm x 0.5mm)	6.3 V
L1	Taiyo Yuden	MEKK2016T1R0M	1.0 μH, I_{SAT}= 4.0 A, R_{DC}= 50 mΩ	0806/2016 (2.0mm x 1.6mm x 1.0mm)	
L2	Taiyo Yuden	MEKK2012HR47M	0.47 μH, I_{SAT}= 5.3 A, R_{DC}= 25 mΩ	0805/2012 (2.0mm x 1.2mm x 1.0mm)	

Recommended Alternative Components

Table 43. ALTERNATIVE COMPONENTS

Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
C_{PVIN}	Taiyo Yuden	JMK105CBJ106MV	10 μF	0402/1005 (1.0mm x 0.5mm)	6.3 V
C_{BUCK}	Taiyo Yuden	JMK105CBJ106MV	10 μF	0402/1005 (1.0mm x 0.5mm)	6.3 V
C_{BSTIN}	Taiyo Yuden	JMK105CBJ106MV	10 μF	0402/1005 (1.0mm x 0.5mm)	6.3 V
C_{BST}	Semco	CL10A226MP8NUXE	22 μF	0603/1608 (1.6mm x 0.8mm)	10 V
C_{LDO1}, C_{LDO2}, C_{LDO3}, C_{LDO4}	Semco	CLO3A225MQCRNC	2.2 μF	0201/0603 (0.6mm x 0.3mm)	6.3 V
L1	TDK	TFM201610GHM−1R0MTAA	1.0 μH, I_{SAT}= 3.8 A, R_{DC}= 50 mΩ	2016 (2.0mm x 1.6mm x 1.0mm)	

APPLICATION GUIDELINES

Buck Input Capacitor Considerations

A minimum capacitance of 2.2 μF with ceramic dielectric, input capacitor should be placed as close as possible between the V_{IN} pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce the ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as V_{IN} increases due to DC bias effects.

Buck Output Capacitor Considerations

FAN53880 uses a 22 μF, 0402 (1005 metric) for an output capacitor. The effective capacitance of ceramic capacitors decrease as the bias voltage across the capacitor increases. Increasing the output capacitor has no effect on loop stability and therefore to overcome the effects of bias voltage across C_{OUT}, the capacitor value can be increased to reduce the output voltage ripple and/or to improve transient response. Output voltage ripple is defined as:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right]$$

Buck Inductor Considerations

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects average current limit, the PWM−to−PFM transition point, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \right)$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current, given by:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2}$$

The FAN53880 is optimized for operation with L = 1.0uH. The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. It is recommended to select an inductor where its saturation current is above the $I_{LIM(PK)}$ value. Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but because ΔI increases, the RMS current increases, as do the core and skin effect losses.

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \right)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs, as well as the inductor DCR. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Table 44.

Inductor Value	$I_{MAX(LOAD)}$	ΔV_{OUT}	Transient Response
Increase	Increase	Decrease	Degraded
Decrease	Decrease	Increase	Improved

Boost Input Capacitor Considerations

The 10 μF ceramic 0402 (1005 metric) input capacitor should be placed as close as possible between the V_{IN} pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed (on Eval board) between C_{IN} and the power source lead to reduce the ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as V_{IN} increases due to DC bias effects.

Boost Output Capacitor

Output voltage ripple is inversely proportional to C_{BST}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{BST}. The maximum V_{RIPPLE} occurs when V_{IN} is minimum and I_{LOAD} is maximum.

It is recommended to use the capacitor shown in either the Recommended External Components or the Alternate Components table. If a different component is chosen, it is important that it's effective capacitance is equal to or greater than that of the Recommended Component. For better ripple performance, additional output capacitance can be added.

Boost Inductor Considerations

The FAN53880 employs a peak current limiting, so peak inductor current can reach 4 A for a short duration during overload conditions. Saturation effects causes the inductor current ripple to become higher under high loading, as only the peak of the inductor current ripple is controlled.

LDO Input Capacitor Considerations

If long wires are used to bring power to an evaluation board, additional "bulk" capacitance (electrolytic or tantalum) should be placed (on Eval board) between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as V_{IN} increases due to DC bias effects. Adding additional capacitance to the minimum recommended ensures reliable operation.

LDO Output Capacitor Considerations

FAN53880 LDO's are tuned for high load capacitance of 2.2 to 26 μF. Total capacitance on the LDO output that is outside this window may result in instability or as a minimum, the LDO not meeting the performance listed in the Electrical and System Characteristics tables. For instance: Adding additional capacitance can slow the soft start when the LDO is enabled but also improves transient response. The effective capacitance of ceramic capacitors decrease as the bias voltage across the capacitor increases.

Recommended Layout

All Layer Layout

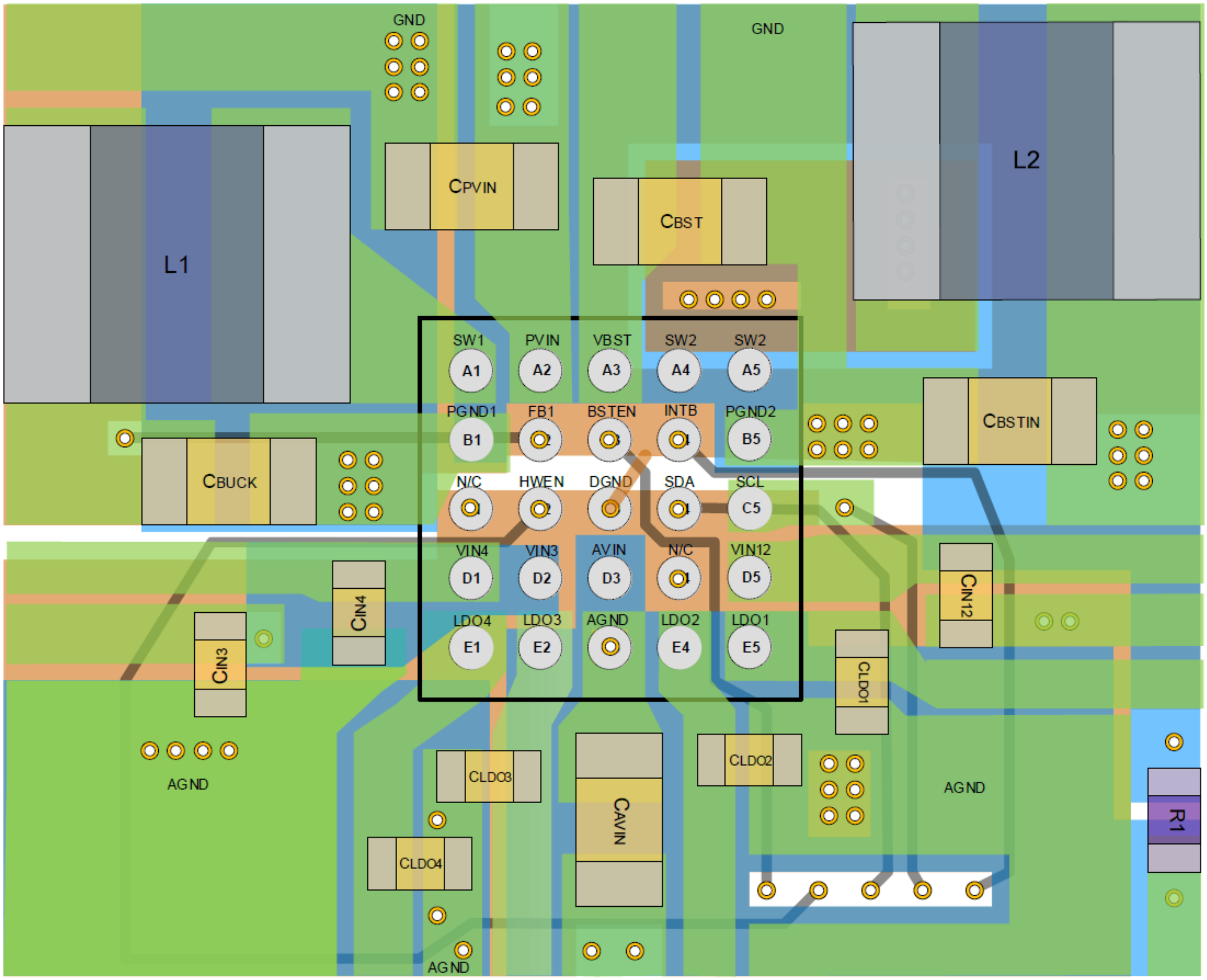


Figure 38. All Layer Layout

Layer 1

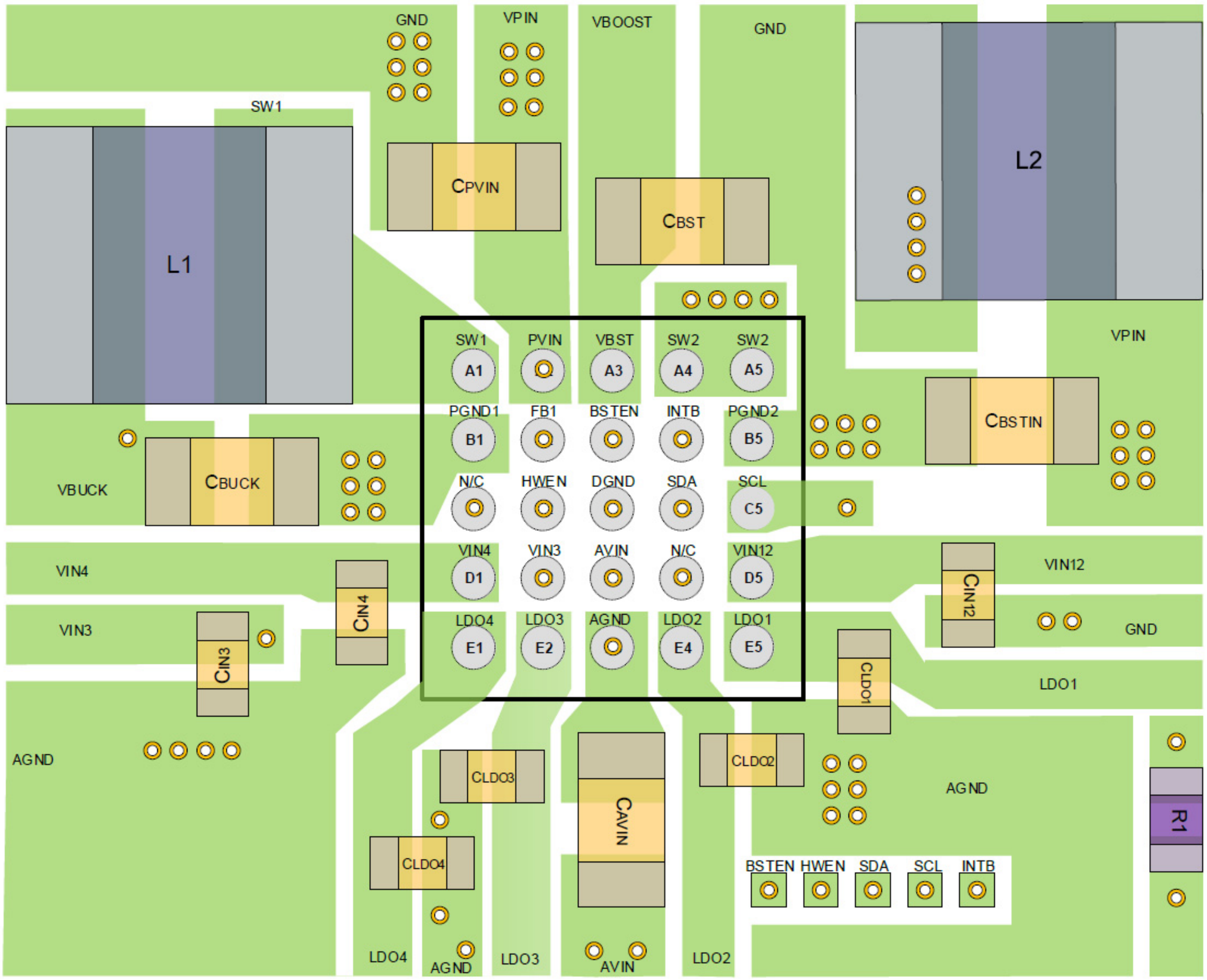


Figure 39. Layer 1

Layer 2, Ground Plane

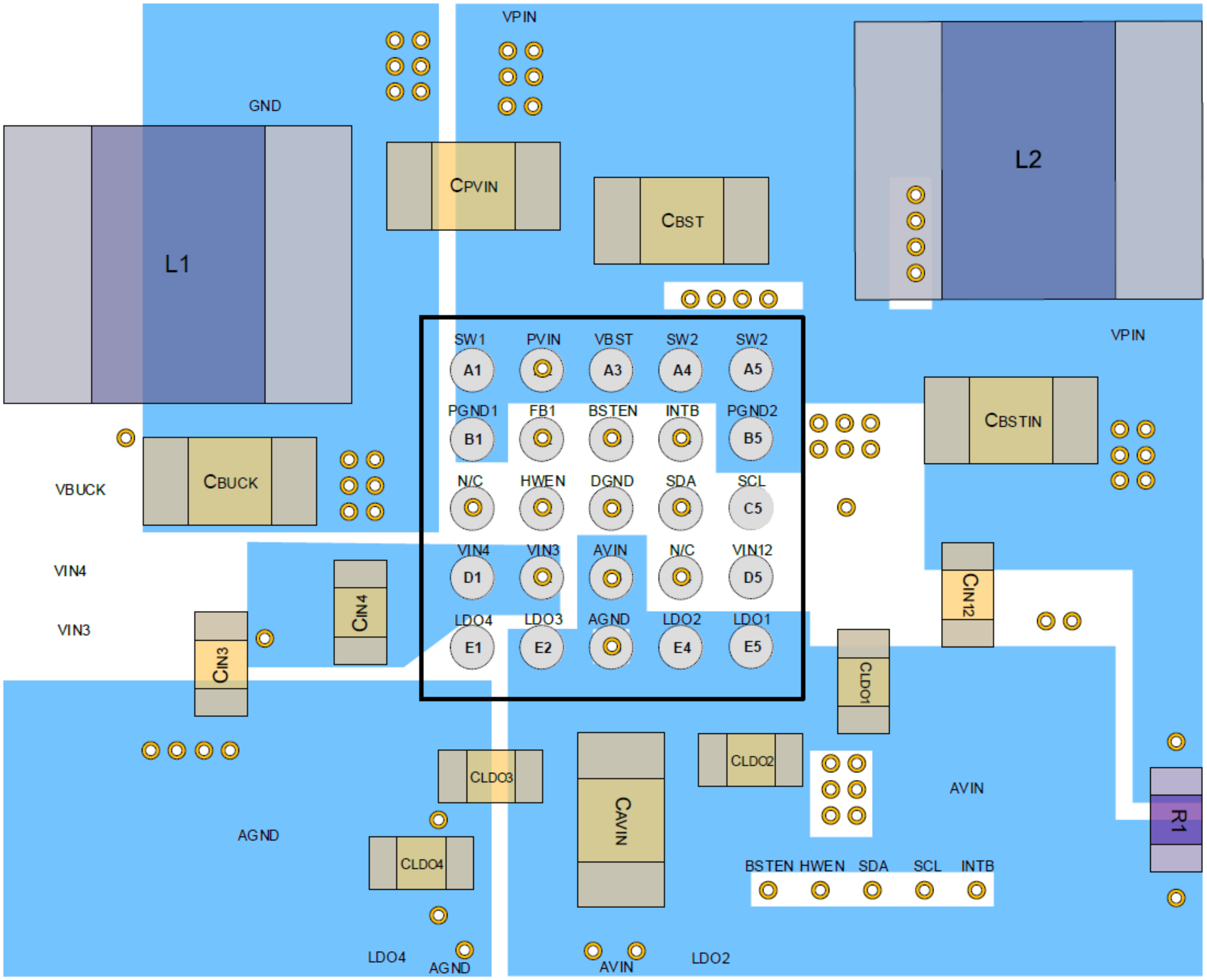


Figure 40. Layer 2, Ground Plane

Layer 3, Signal Plane

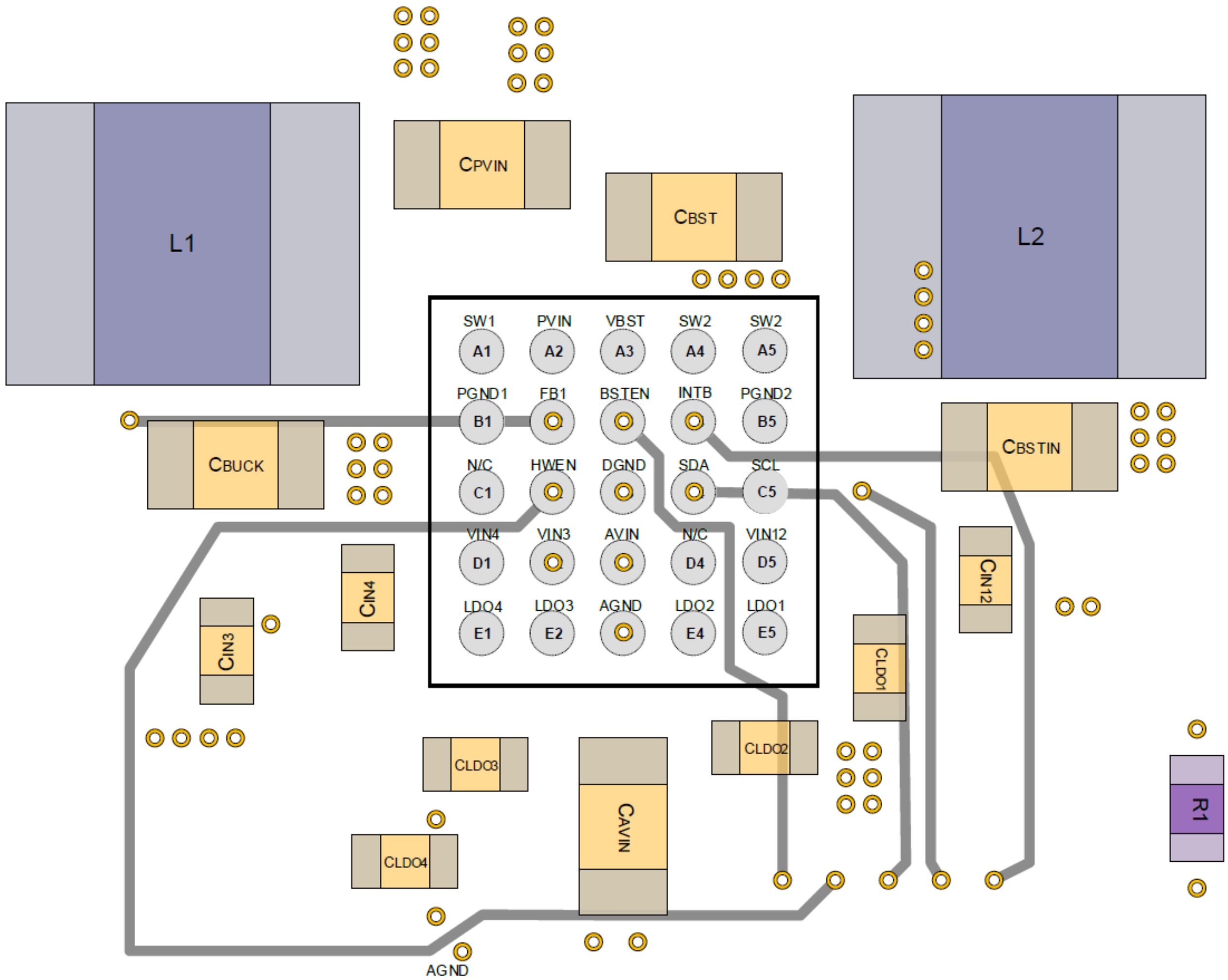


Figure 41. Layer 3, Signal Plane

Layer 4, Power Plane

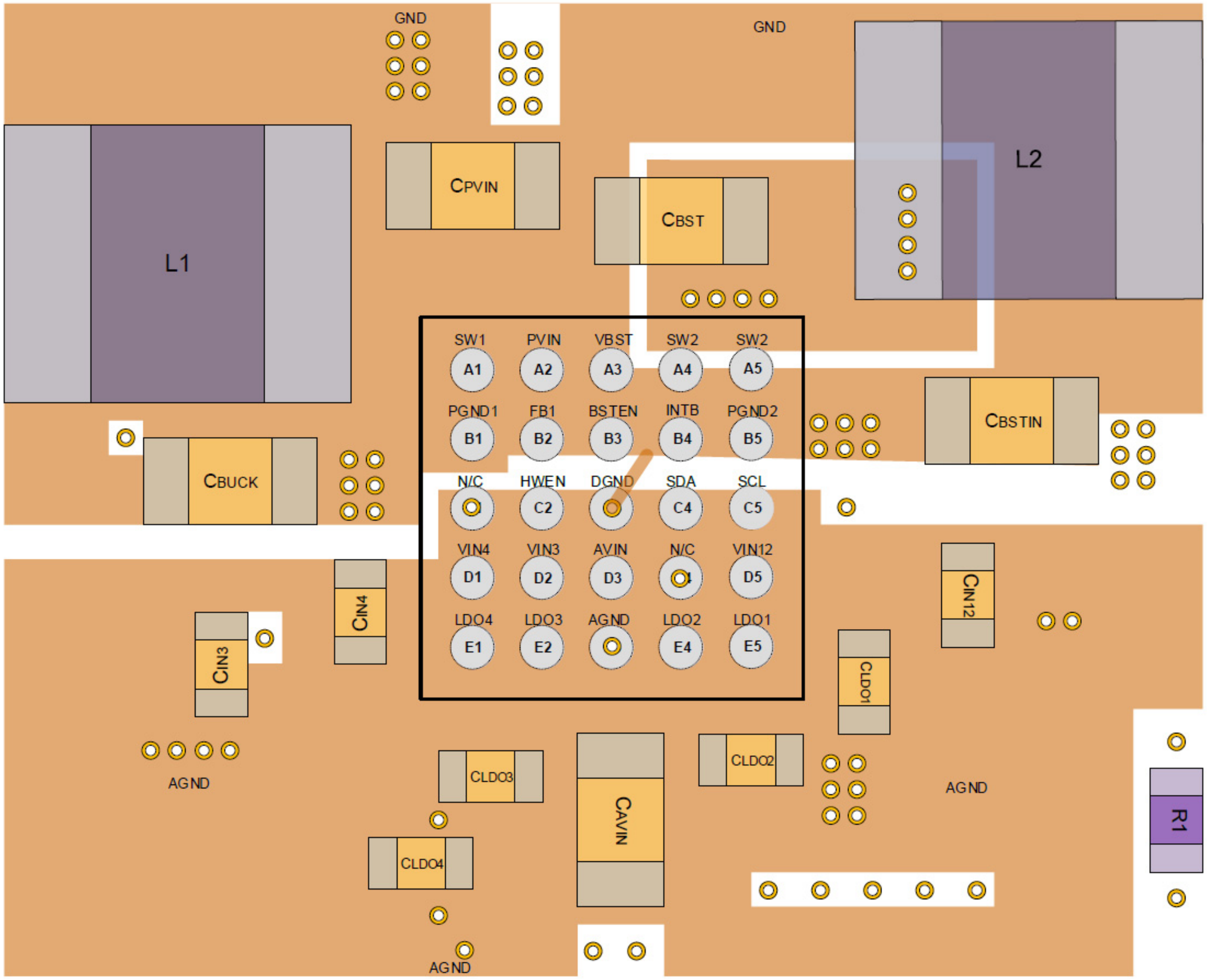


Figure 42. Layer 4, Power Plane

Layout Considerations

To minimize spikes for the buck at V_{OUT}, C_{OUT} must be placed as close as possible to PGND1 and VOUT, as shown in the recommended layout. For the boost, CIN should be located as close to PGND2 as possible to minimize the spikes and noise generated by the switching node LX2.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

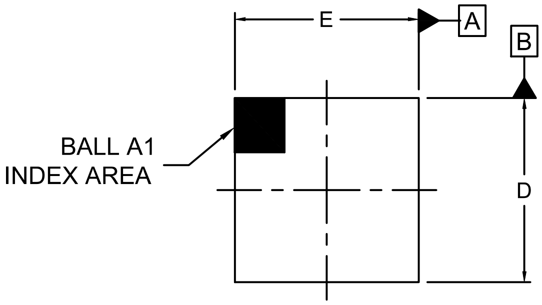
PACKAGE DIMENSIONS

WLCSP25 2.16x2.16x0.586
CASE 567QT
ISSUE A

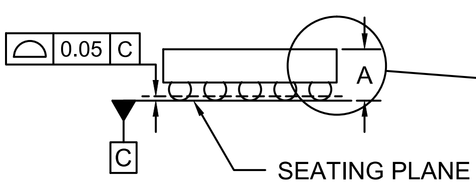
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

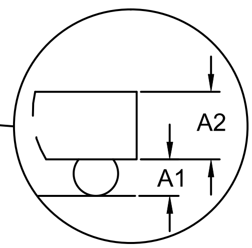
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.547	0.586	0.625
A1	0.188	0.208	0.228
A2	0.360	0.378	0.396
b	0.24	0.26	0.28
D	2.13	2.16	2.19
E	2.13	2.16	2.19
e	0.40 BSC		
x	0.265	0.280	0.295
y	0.265	0.280	0.295



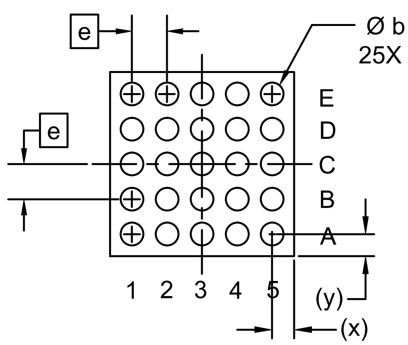
TOP VIEW



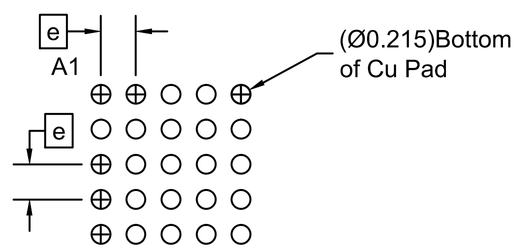
SIDE VIEW



DETAIL A



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT
(NSMD PAD TYPE)

Table 45. PRODUCT SPECIFIC DIMENSIONS

Product	D (mm)	E (mm)	X (mm)	Y (mm)
FAN53880	2.16	2.16	0.08	0.08

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
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Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative