

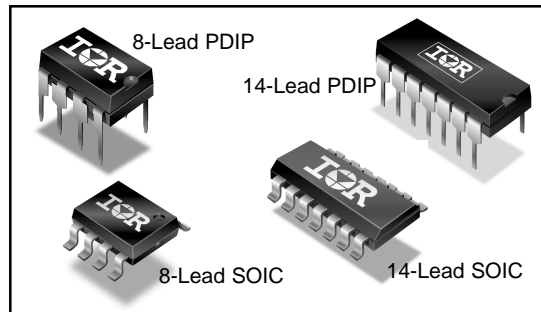
IRS2106/IRS21064(S)PbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IRS2106)
- RoHS compliant

Packages



Description

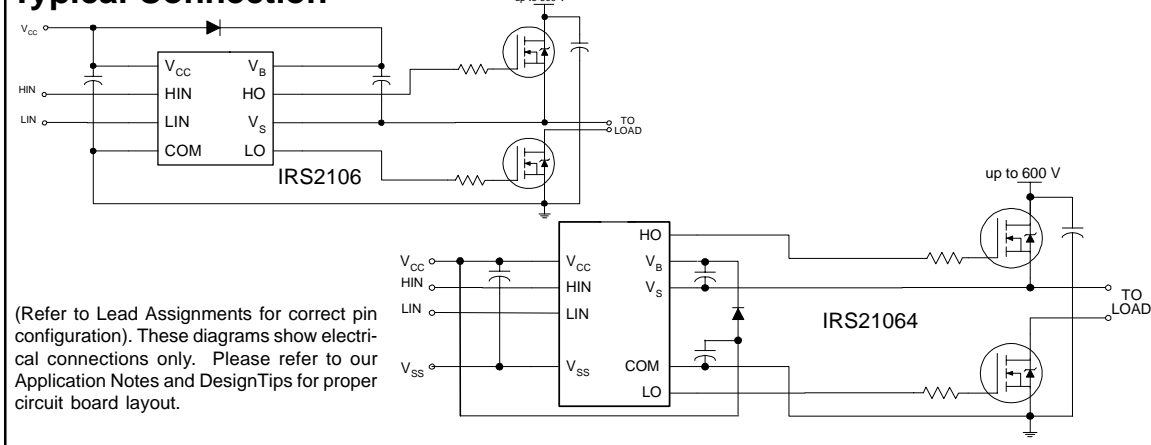
The IRS2106/IRS21064 are high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic.

The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

Feature Comparison

| Part | Input logic | Cross-conduction prevention logic | Deadtime (ns) | Ground Pins | ton/toff (ns) |
|-----------|-------------|-----------------------------------|-------------------------|-------------|---------------|
| 2106/2301 | HIN/LIN | no | none | COM | 220/200 |
| 21064 | | | | Vss/COM | |
| 2108 | HIN/LIN | yes | Internal 540 | COM | 220/200 |
| 21084 | | | Programmable 540 - 5000 | Vss/COM | |
| 2109/2302 | IN/SD | yes | Internal 540 | COM | 750/200 |
| 21094 | | | Programmable 540 - 5000 | Vss/COM | |
| 2304 | HIN/LIN | yes | Internal 100 | COM | 160/140 |

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units | |
|---------------------|---|-----------------------|-----------------------|-------|------|
| V _B | High-side floating absolute voltage | -0.3 | 625 | V | |
| V _S | High-side floating supply offset voltage | V _B - 25 | V _B + 0.3 | | |
| V _{HO} | High-side floating output voltage | V _S - 0.3 | V _B + 0.3 | | |
| V _{CC} | Low-side and logic fixed supply voltage | -0.3 | 25 | | |
| V _{LO} | Low-side output voltage | -0.3 | V _{CC} + 0.3 | | |
| V _{IN} | Logic input voltage | V _{SS} - 0.3 | V _{CC} + 0.3 | | |
| V _{SS} | Logic ground (IRS21064 only) | V _{CC} - 25 | V _{CC} + 0.3 | | |
| dV _S /dt | Allowable offset supply voltage transient | — | 50 | V/ns | |
| P _D | Package power dissipation @ T _A ≤ +25 °C | (8 lead PDIP) | — | 1.0 | W |
| | | (8 lead SOIC) | — | 0.625 | |
| | | (14 lead PDIP) | — | 1.6 | |
| | | (14 lead SOIC) | — | 1.0 | |
| R _{thJA} | Thermal resistance, junction to ambient | (8 lead PDIP) | — | 125 | °C/W |
| | | (8 lead SOIC) | — | 200 | |
| | | (14 lead PDIP) | — | 75 | |
| | | (14 lead SOIC) | — | 120 | |
| T _J | Junction temperature | — | 150 | °C | |
| T _S | Storage temperature | -50 | 150 | | |
| T _L | Lead temperature (soldering, 10 seconds) | — | 300 | | |

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at a 15 V differential.

| Symbol | Definition | Min. | Max. | Units |
|----------|--|------------|------------|-------|
| V_B | High-side floating supply absolute voltage | $V_S + 10$ | $V_S + 20$ | V |
| V_S | High-side floating supply offset voltage | Note 1 | 600 | |
| V_{HO} | High-side floating output voltage | V_S | V_B | |
| V_{CC} | Low-side and logic fixed supply voltage | 10 | 20 | |
| V_{LO} | Low-side output voltage | 0 | V_{CC} | |
| V_{IN} | Logic input voltage | V_{SS} | V_{CC} | |
| V_{SS} | Logic ground (IRS21064 only) | -5 | 5 | |
| T_A | Ambient temperature | -40 | 125 | °C |

Note 1: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $V_{SS} = \text{COM}$, $C_L = 1000\text{ pF}$, $T_A = 25\text{ °C}$.

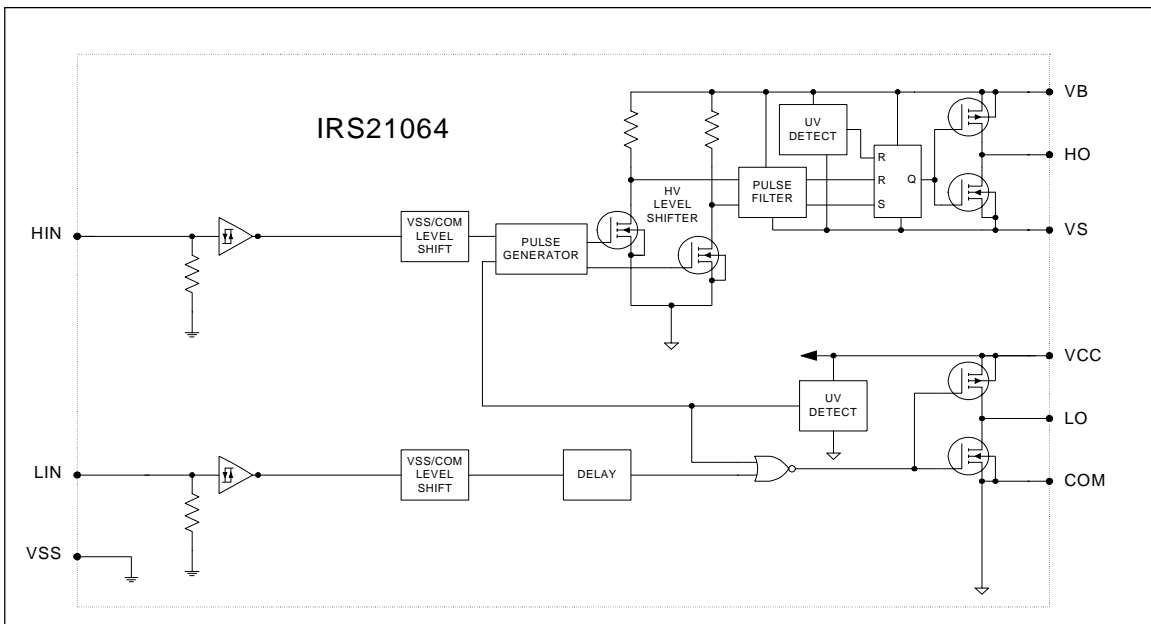
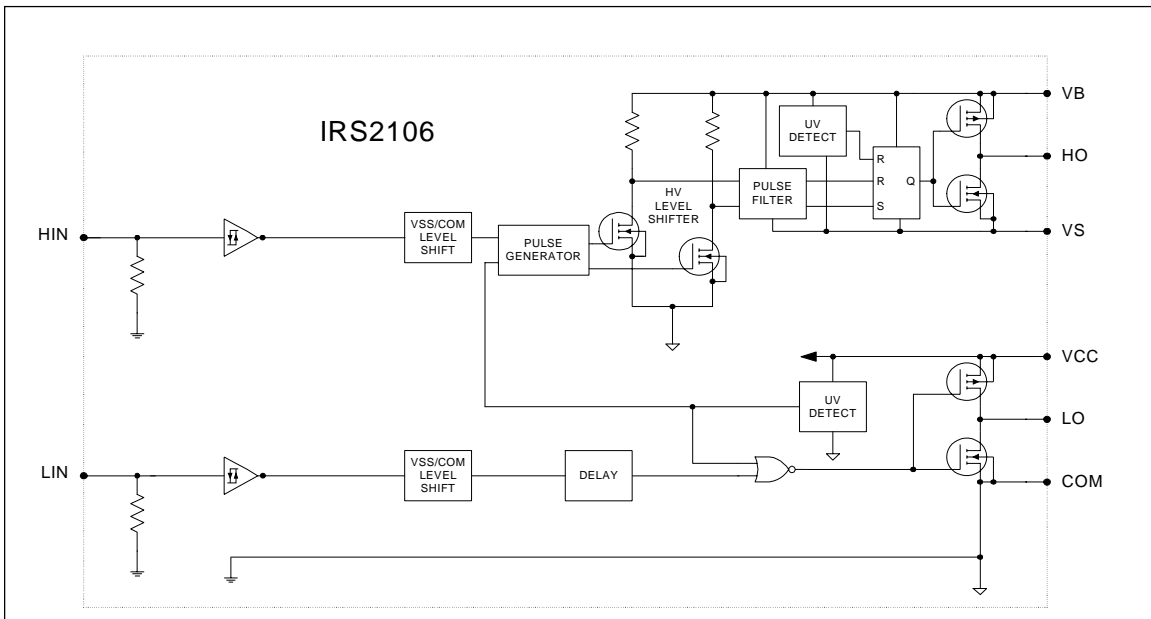
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|-------------------------------------|------|------|------|-------|--------------------------------------|
| t_{on} | Turn-on propagation delay | — | 220 | 300 | ns | $V_S = 0\text{ V}$ |
| t_{off} | Turn-off propagation delay | — | 200 | 280 | | $V_S = 0\text{ V}$ or 600 V |
| MT | Delay matching, HS & LS turn-on/off | — | 0 | 30 | | |
| t_r | Turn-on rise time | — | 100 | 220 | | $V_S = 0\text{ V}$ |
| t_f | Turn-off fall time | — | 35 | 80 | | |

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15 V, V_{SS} = COM and T_A = 25 °C unless otherwise specified. The V_{IL} , V_{IH} , and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads. The V_O , I_O , and R_{ON} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|----------------------------|--|------|------|------|---------------|---|
| V_{IH} | Logic "1" input voltage | 2.5 | — | — | V | $V_{CC} = 10\text{ V to }20\text{ V}$ |
| V_{IL} | Logic "0" input voltage | — | — | 0.8 | | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | — | 0.05 | 0.2 | | $I_O = 2\text{ mA}$ |
| V_{OL} | Low level output voltage, V_O | — | 0.02 | 0.1 | | |
| I_{LK} | Offset supply leakage current | — | — | 50 | μA | $V_B = V_S = 600\text{ V}$ |
| I_{QBS} | Quiescent V_{BS} supply current | 20 | 75 | 130 | | $V_{IN} = 0\text{ V or }5\text{ V}$ |
| I_{QCC} | Quiescent V_{CC} supply current | 60 | 120 | 180 | | |
| I_{IN+} | Logic "1" input bias current $V_{IN} = 5\text{ V}$ | — | 5 | 20 | | |
| I_{IN-} | Logic "0" input bias current $V_{IN} = 0\text{ V}$ | — | — | 5 | | |
| V_{CCUV+} V_{BSUV+} | V_{CC} and V_{BS} supply undervoltage positive going threshold | 8.0 | 8.9 | 9.8 | V | |
| V_{CCUV-} V_{BSUV-} | V_{CC} and V_{BS} supply undervoltage negative going threshold | 7.4 | 8.2 | 9.0 | | |
| V_{CCUVH} V_{BSUVH} | Hysteresis | 0.3 | 0.7 | — | | |
| I_{O+} | Output high short circuit pulsed current | 130 | 290 | — | mA | $V_O = 0\text{ V},$ $PW \leq 10\ \mu\text{s}$ |
| I_{O-} | Output low short circuit pulsed current | 270 | 600 | — | | $V_O = 15\text{ V},$ $PW \leq 10\ \mu\text{s}$ |

Functional Block Diagrams



Lead Definitions

| Symbol | Description |
|-----------------|---|
| HIN | Logic input for high-side gate driver output (HO), in phase |
| LIN | Logic input for low-side gate driver output (LO), in phase |
| VSS | Logic ground (IRS21064 only) |
| V _B | High-side floating supply |
| HO | High-side gate drive output |
| V _S | High-side floating supply return |
| V _{CC} | Low-side and logic fixed supply |
| LO | Low-side gate drive output |
| COM | Low-side return |

Lead Assignments

| | |
|--------------------|--------------------|
| <p>8 Lead PDIP</p> | <p>8 Lead SOIC</p> |
| IRS2106PbF | IRS2106SPbF |

| | |
|---------------------|---------------------|
| <p>14 Lead PDIP</p> | <p>14 Lead SOIC</p> |
| IRS21064PbF | IRS21064SPbF |

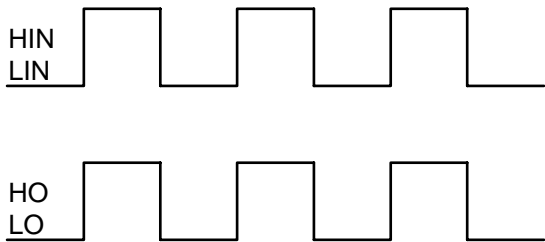


Figure 1. Input/Output Timing Diagram

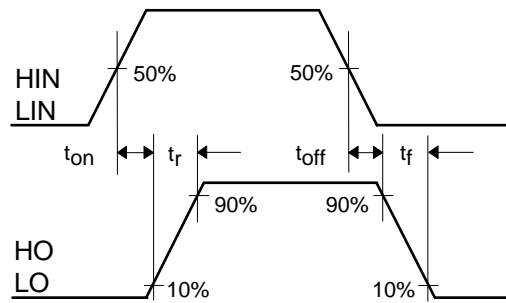


Figure 2. Switching Time Waveform Definitions

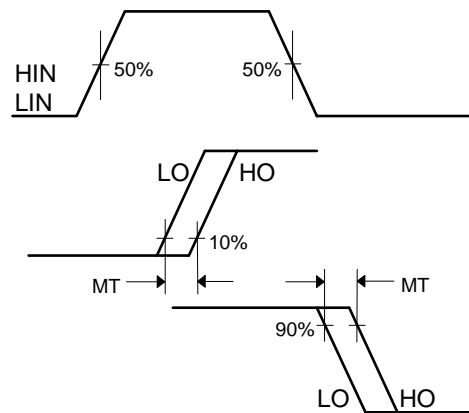


Figure 3. Delay Matching Waveform Definitions

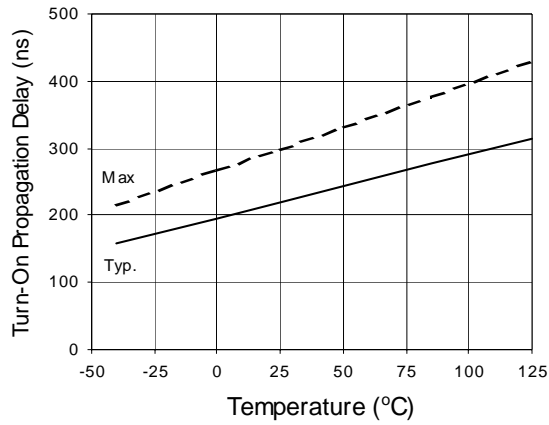


Figure 4A. Turn-On Propagation Delay vs. Temperature

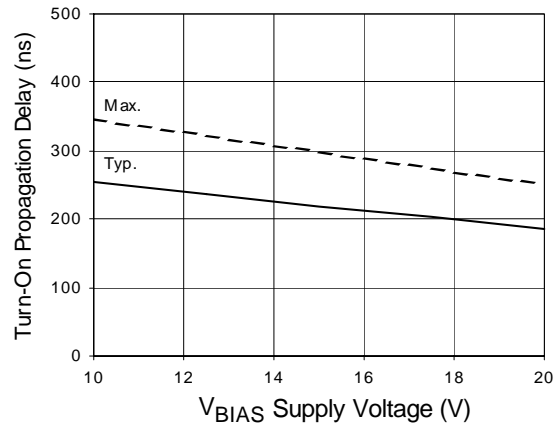


Figure 4B. Turn-On Propagation Delay vs. Supply Voltage

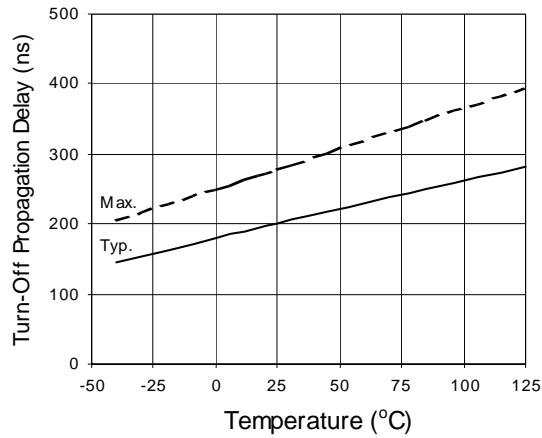


Figure 5A. Turn-Off Propagation Delay vs. Temperature

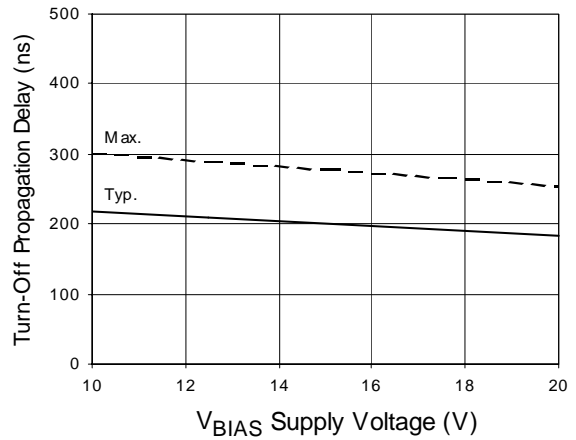


Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage

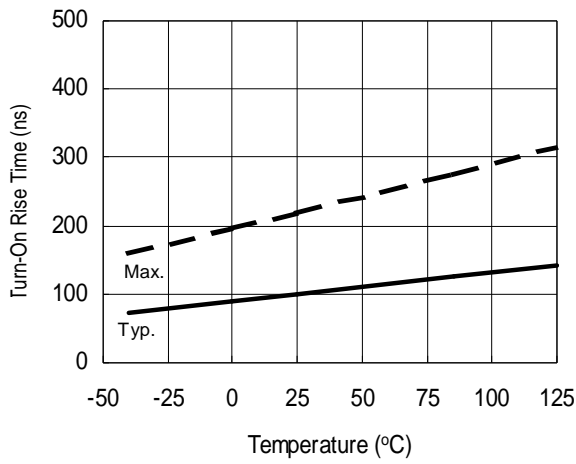


Figure 6A. Turn-On Rise Time vs. Temperature

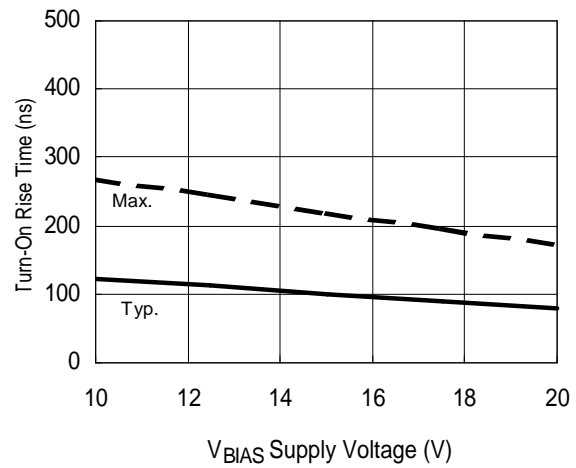


Figure 6B. Turn-On Rise Time vs. Supply Voltage

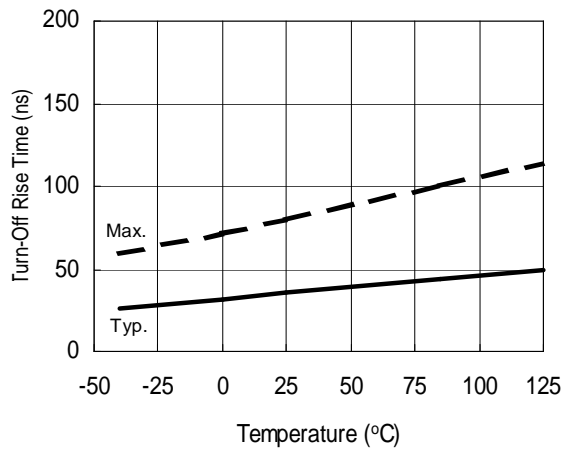


Figure 7A. Turn-Off Fall Time vs. Temperature

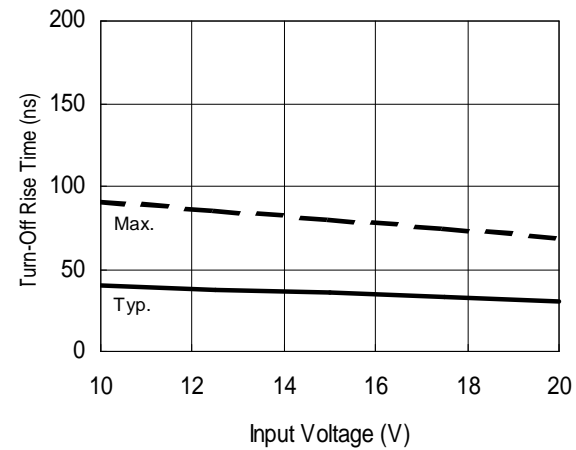


Figure 7B. Turn-Off Fall Time vs. Supply Voltage

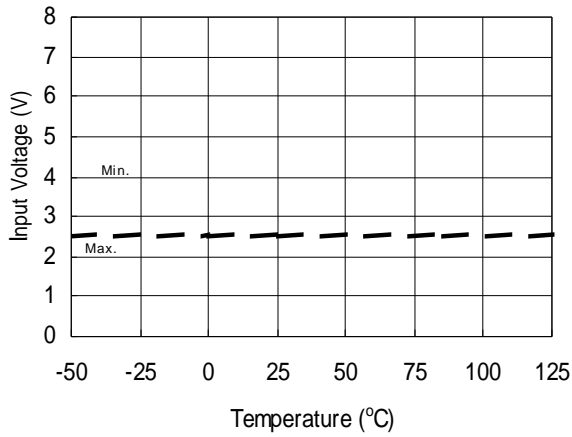


Figure 8A. Logic "1" Input Voltage vs. Temperature

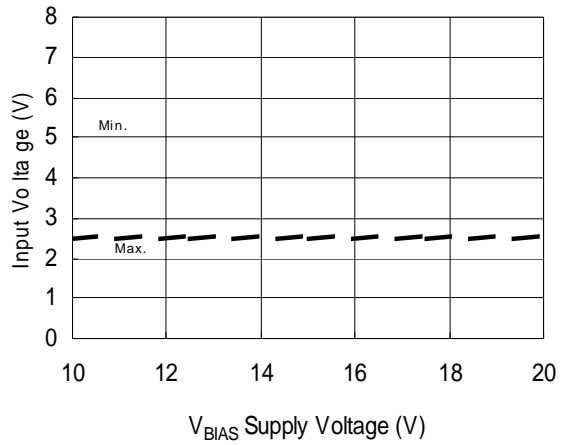


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

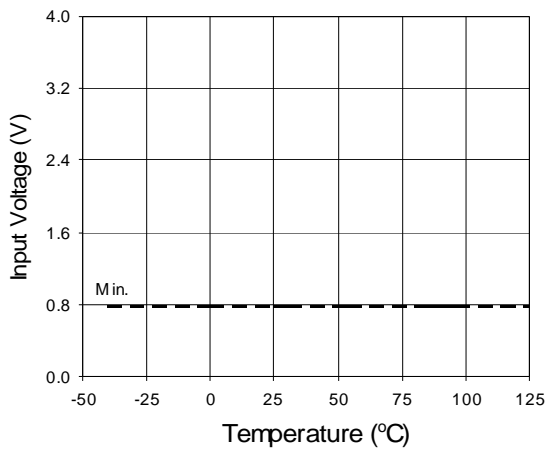


Figure 9A. Logic "0" Input Voltage vs. Temperature

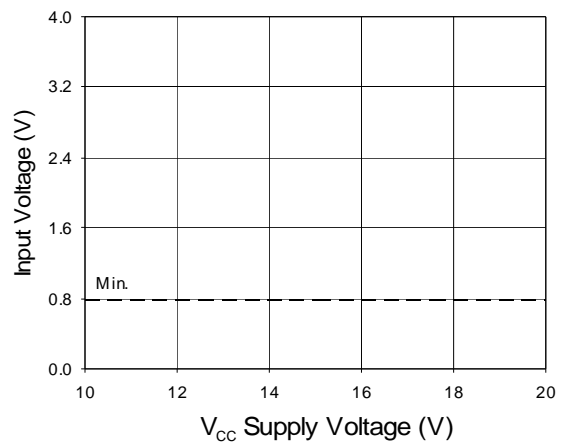


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

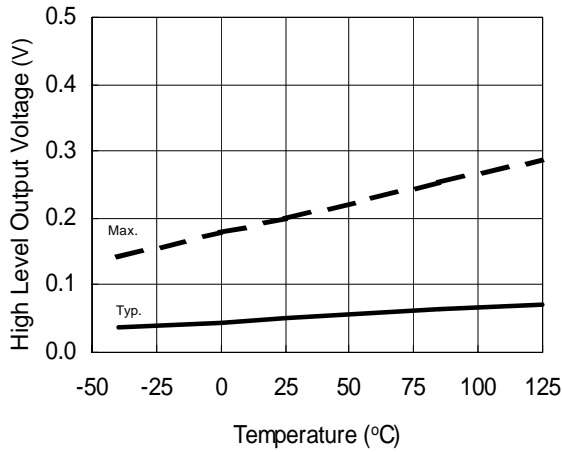


Figure 10A. High Level Output Voltage vs. Temperature

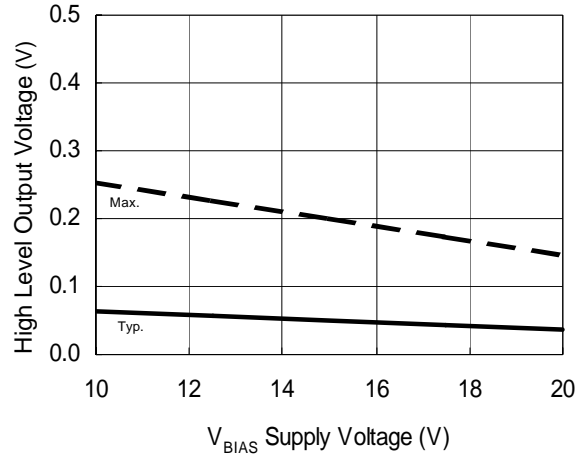


Figure 10B. High Level Output Voltage vs. Supply Voltage

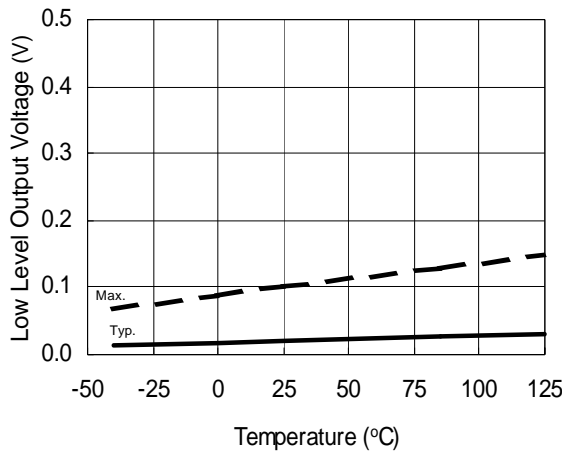


Figure 11A. Low Level Output Voltage vs. Temperature

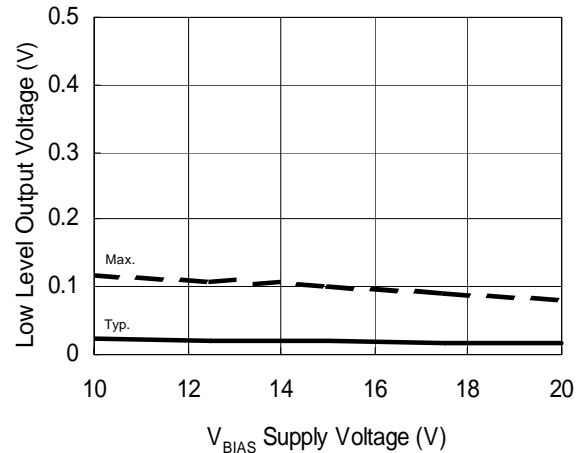


Figure 11B. Low Level Output Voltage vs. Supply Voltage

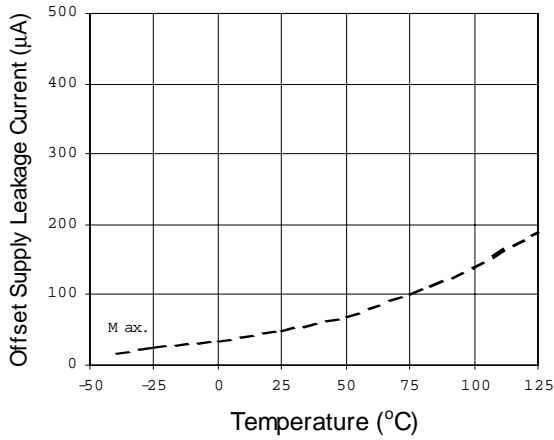


Figure 12A. Offset Supply Leakage Current vs. Temperature

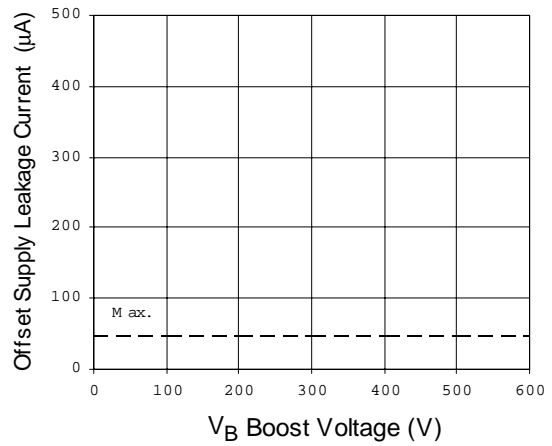


Figure 12B. Offset Supply Leakage Current vs. Supply Voltage

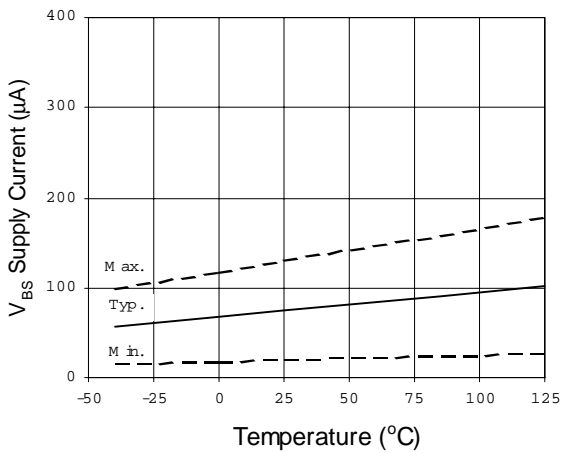


Figure 13A. V_{BS} Supply Current vs. Temperature

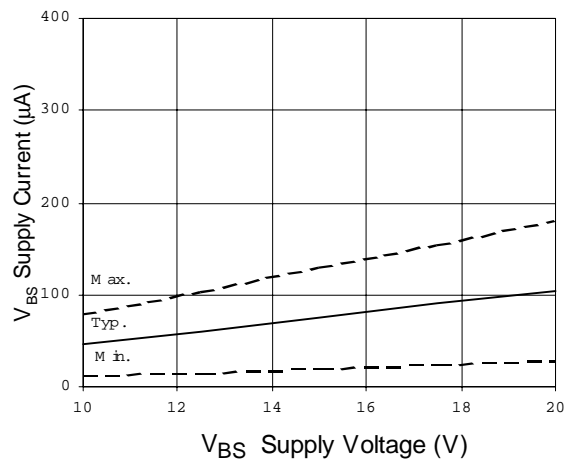


Figure 13B. V_{BS} Supply Current vs. Supply Voltage

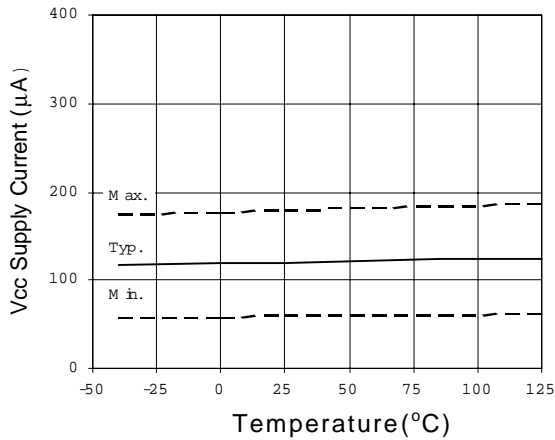


Figure 14A. Quiescent VCC Supply Current vs. Temperature

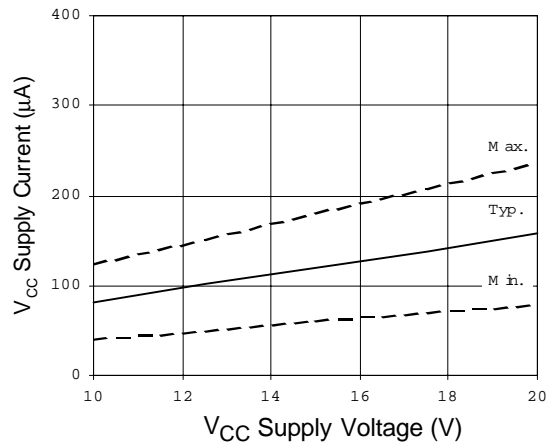


Figure 14B. Quiescent VCC Supply Current vs. VCC Supply Voltage

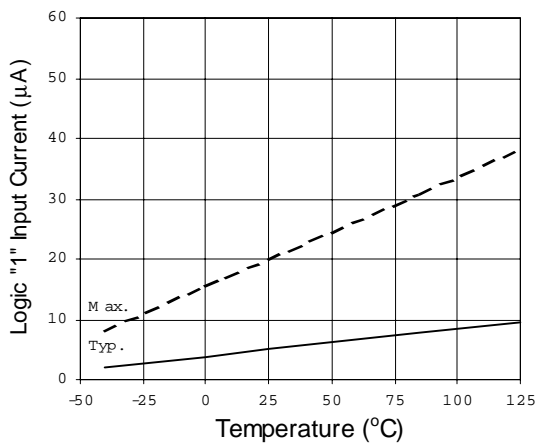


Figure 15A. Logic "1" Input Current vs. Temperature

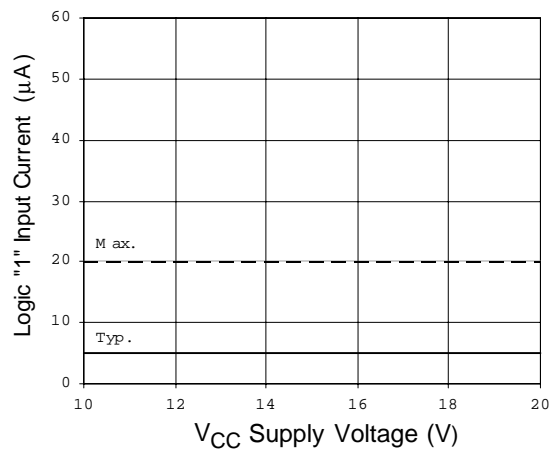


Figure 15B. Logic "1" Bias Current vs. Supply Voltage

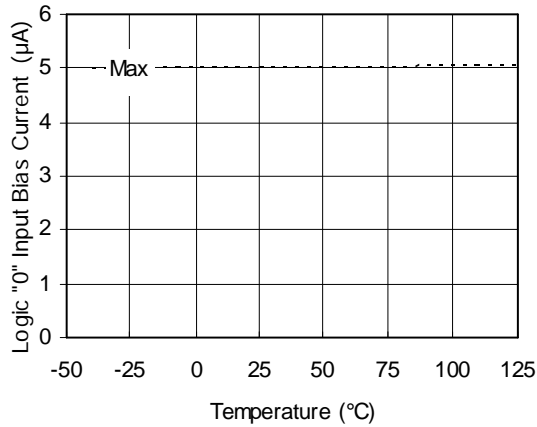


Figure 16A. Logic "0" Input Bias Current vs. Temperature

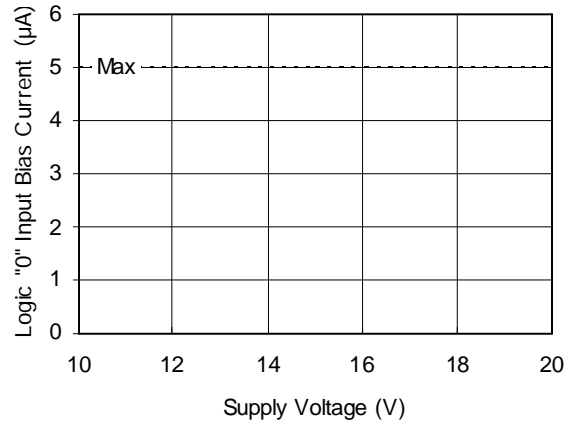


Figure 16B. Logic "0" Input Bias Current vs. Voltage

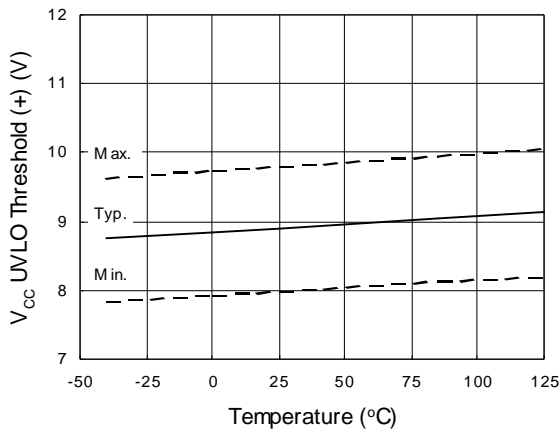


Figure 17. V_{CC} Undervoltage Threshold (+) vs. Temperature

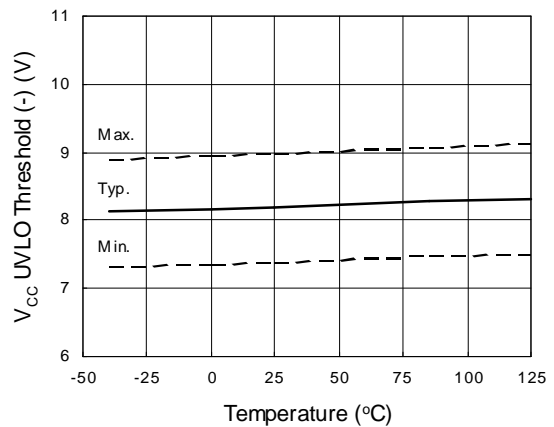


Figure 18. V_{CC} Undervoltage Threshold (-) vs. Temperature

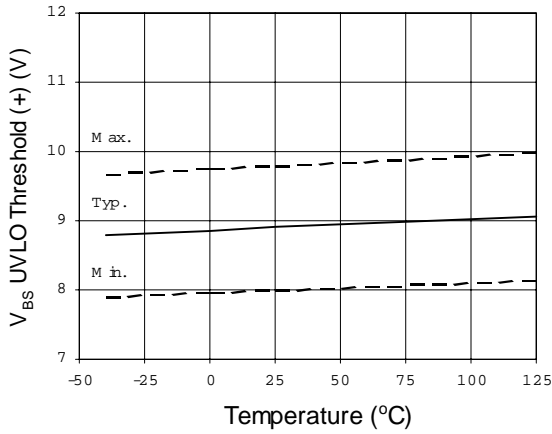


Figure 19. V_{BS} Undervoltage Threshold (+) vs. Temperature

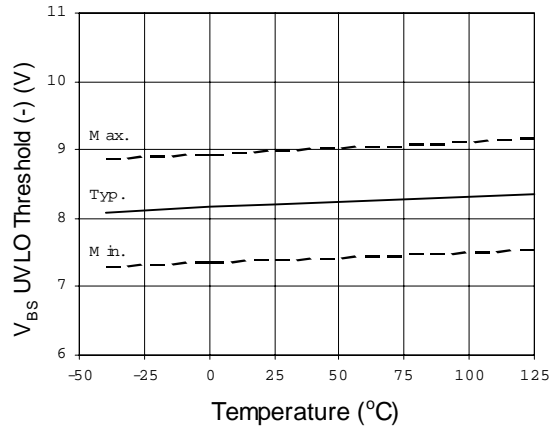


Figure 20. V_{BS} Undervoltage Threshold (-) vs. Temperature

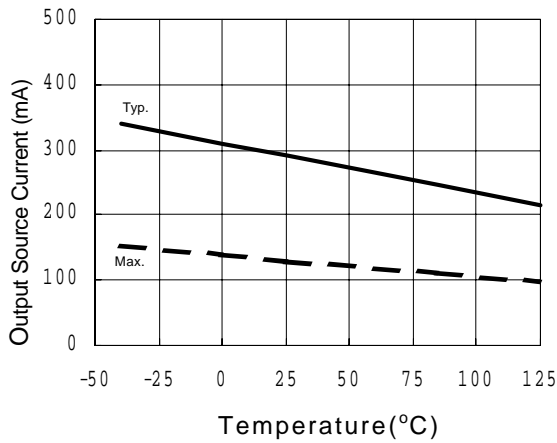


Figure 21A. Output Source Current vs. Temperature

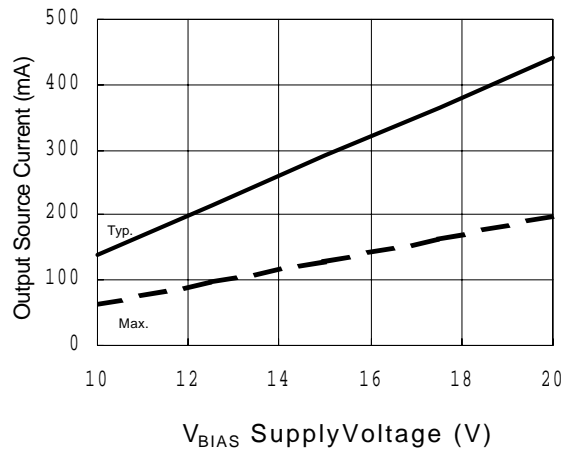


Figure 21B. Output Source Current vs. Supply Voltage

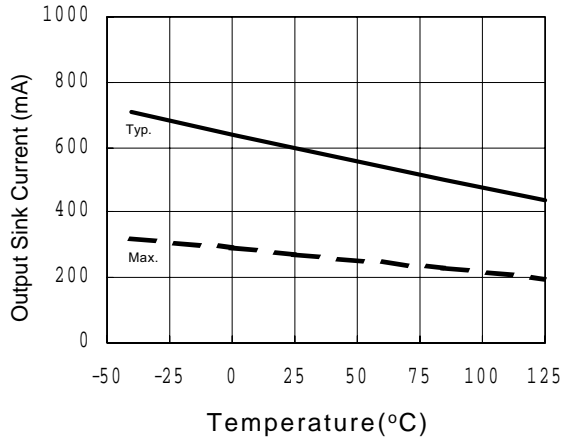


Figure 22A. Output Sink Current vs. Temperature

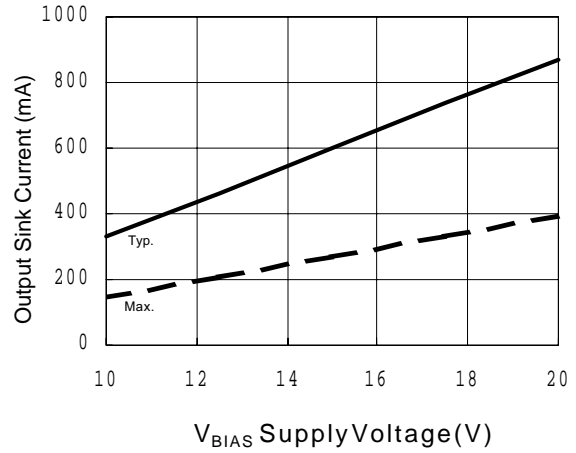


Figure 22B. Output Sink Current vs. Supply Voltage

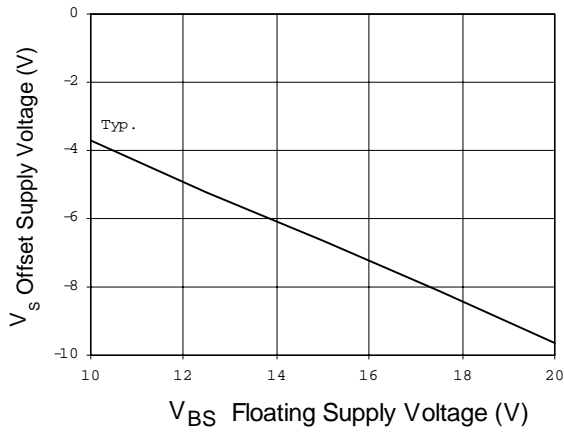


Figure 23. Maximum V_S Negative Offset vs. Supply Voltage

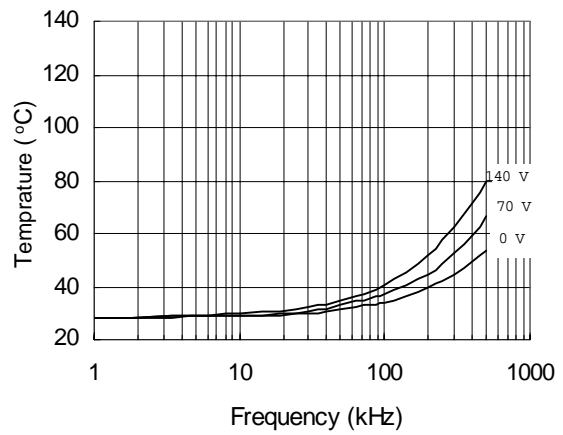


Figure 24. IRS2106 vs. Frequency (IRFBC20), R_{gate}=33 Ω, V_{CC}=15 V

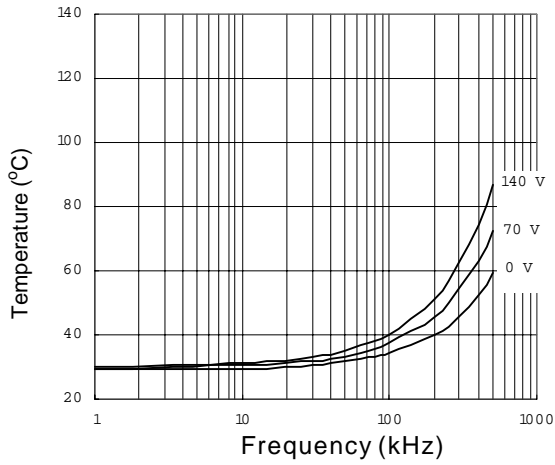


Figure 25. IRS2106 vs. Frequency (IRFBC30),
 $R_{gate}=22 \Omega$, $V_{CC}=15 V$

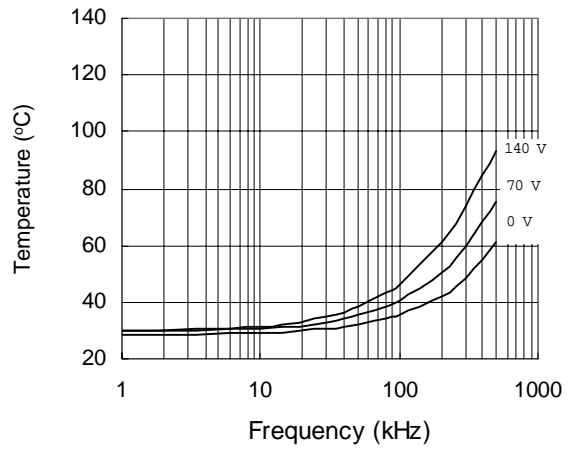


Figure 26. IRS2106 vs. Frequency (IRFBC40),
 $R_{gate}=15 \Omega$, $V_{CC}=15 V$

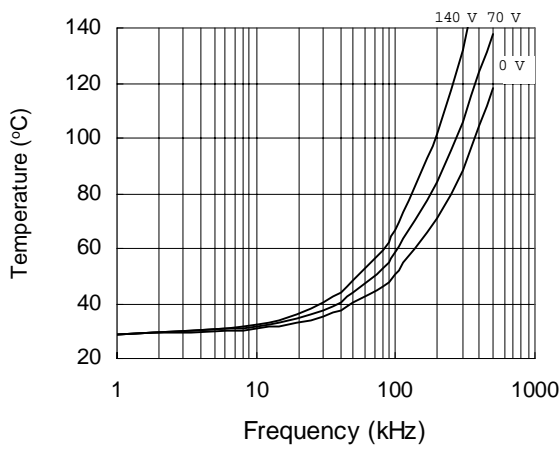


Figure 27. IRS2106 vs. Frequency (IRFPE50),
 $R_{gate}=10 \Omega$, $V_{CC}=15 V$

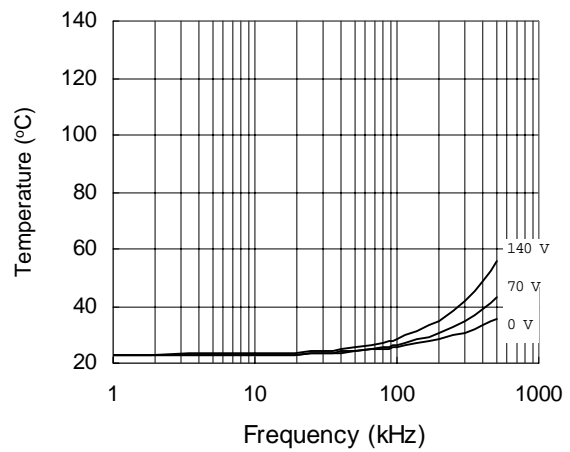
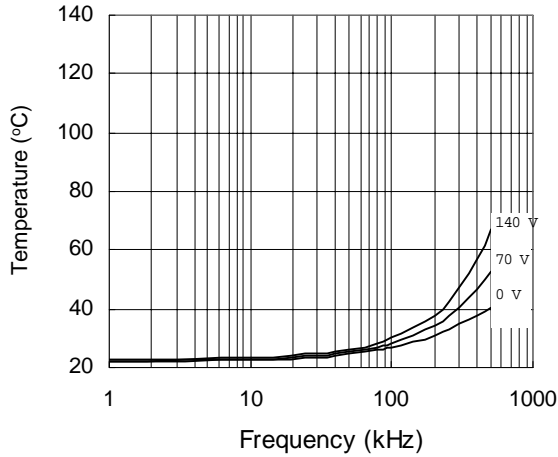
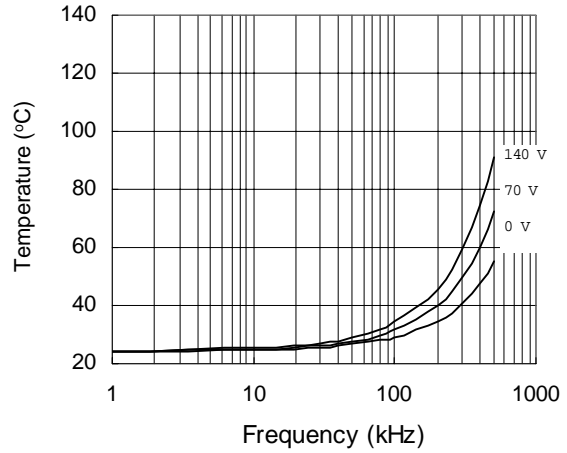


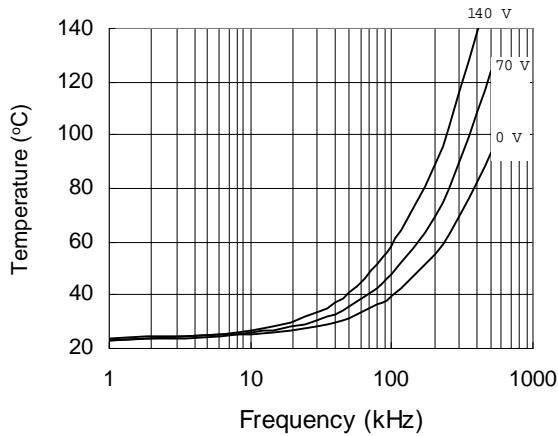
Figure 28. IRS21064 vs. Frequency (IRFBC20),
 $R_{gate}=33 \Omega$, $V_{CC}=15 V$



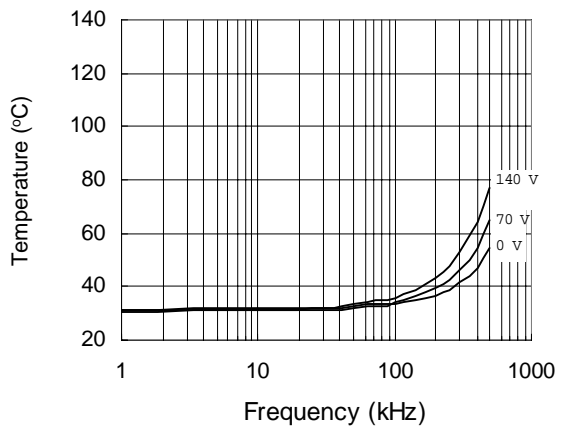
**Figure 29. IRS21064 vs. Frequency (IRFBC30),
 $R_{gate}=22 \Omega, V_{CC}=15 V$**



**Figure 30. IRS21064 vs. Frequency (IRFBC40),
 $R_{gate}=15 \Omega, V_{CC}=15 V$**



**Figure 31. IRS21064 vs. Frequency (IRFPE50),
 $R_{gate}=10 \Omega, V_{CC}=15 V$**



**Figure 32. IRS2106S vs. Frequency (IRFBC20),
 $R_{gate}=33 \Omega, V_{CC}=15 V$**

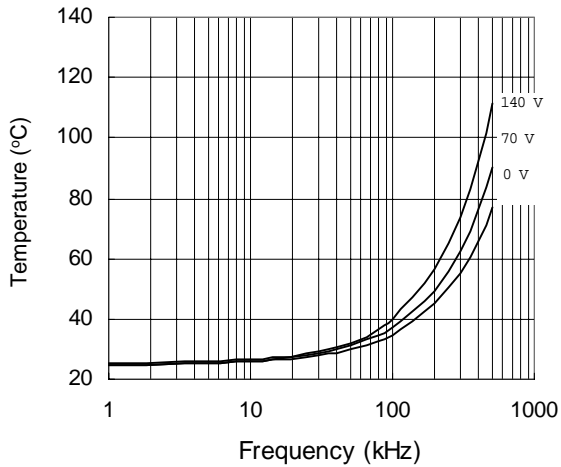


Figure 33. IRS2106S vs. Frequency (IRFBC30),
 $R_{gate}=22 \Omega$, $V_{CC}=15 V$

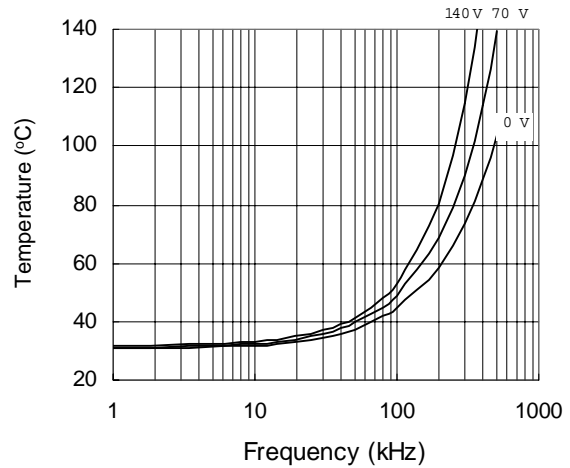


Figure 34. IRS2106S vs. Frequency (IRFBC40),
 $R_{gate}=15 \Omega$, $V_{CC}=15 V$

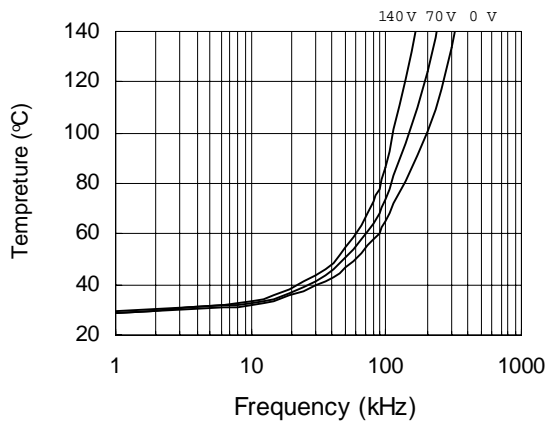


Figure 35. IRS2106S vs. Frequency (IRFPE50),
 $R_{gate}=10 \Omega$, $V_{CC}=15 V$

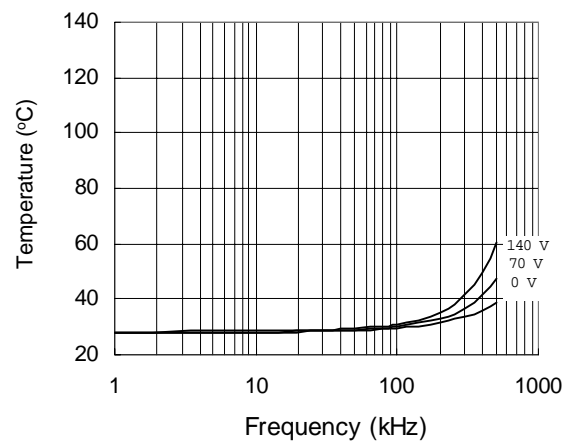
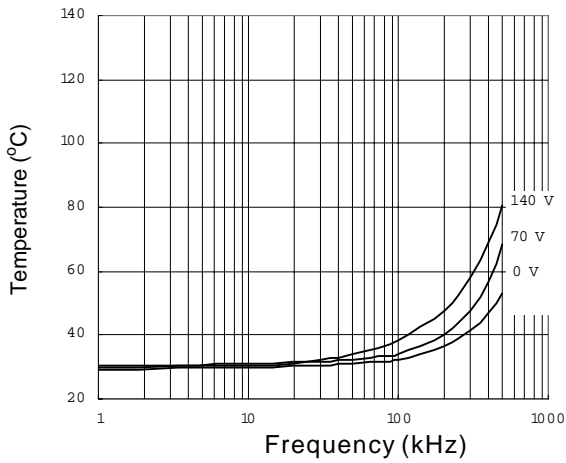
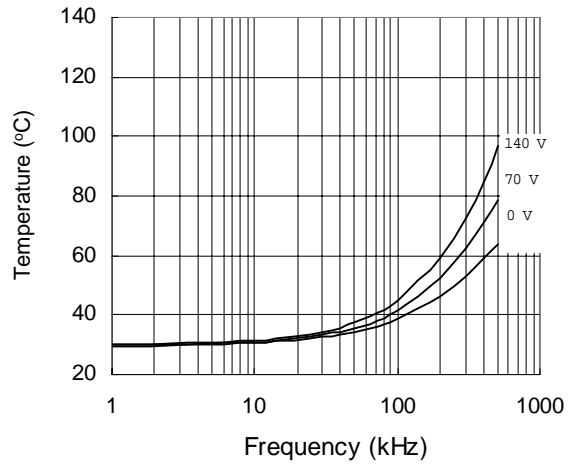


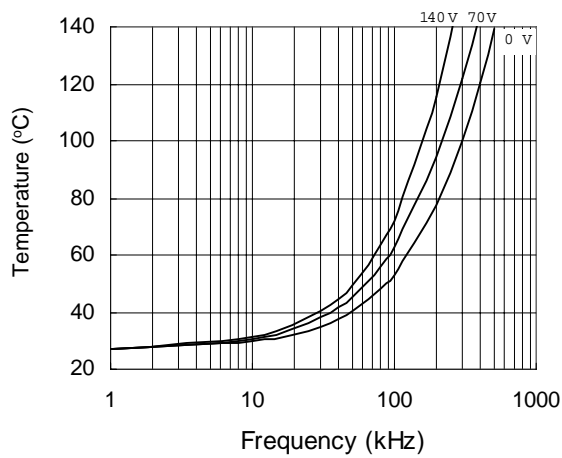
Figure 36. IRS21064S vs. Frequency (IRFBC20),
 $R_{gate}=33 \Omega$, $V_{CC}=15 V$



**Figure 37. IRS21064S vs. Frequency (IRFBC30),
 $R_{gate}=22 \Omega$, $V_{CC}=15 V$**

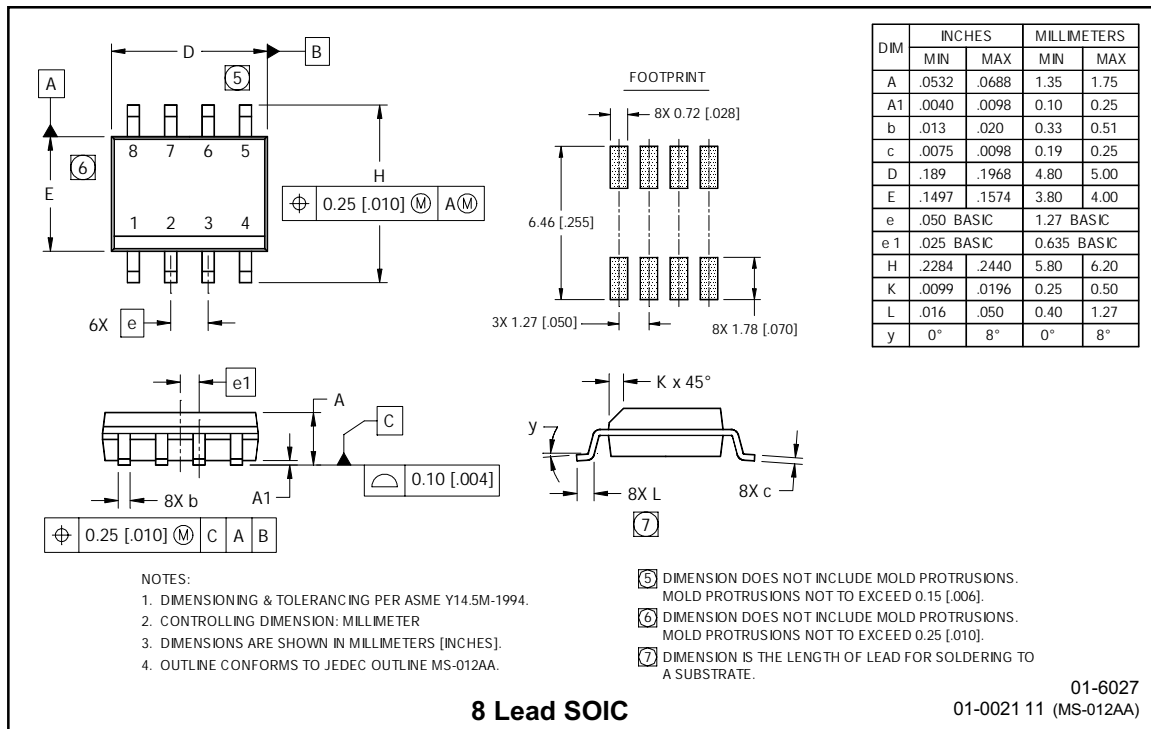
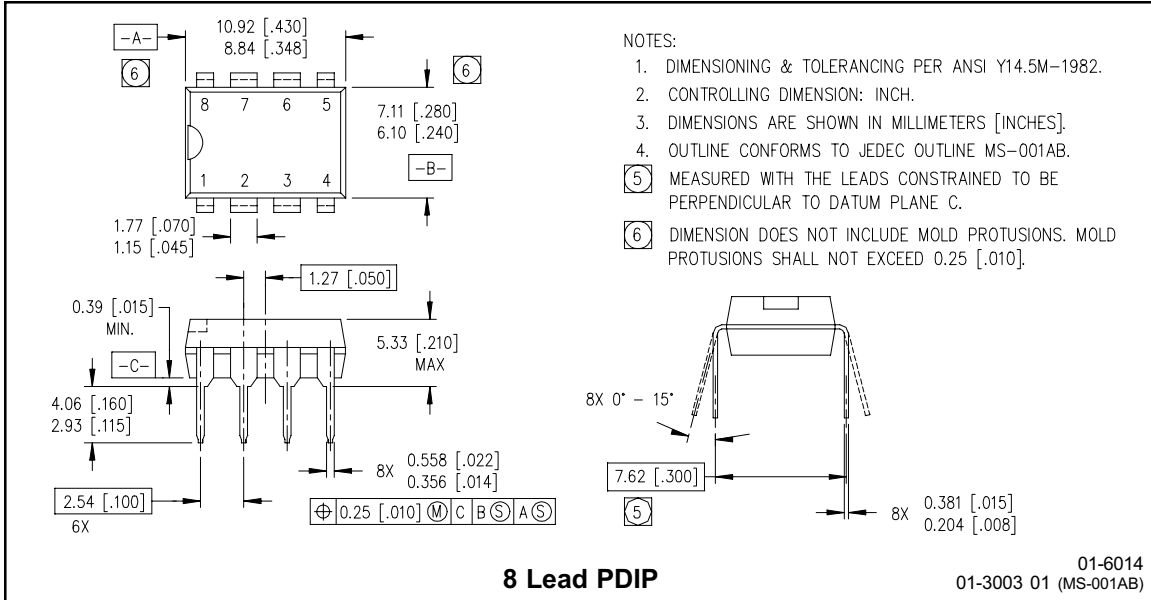


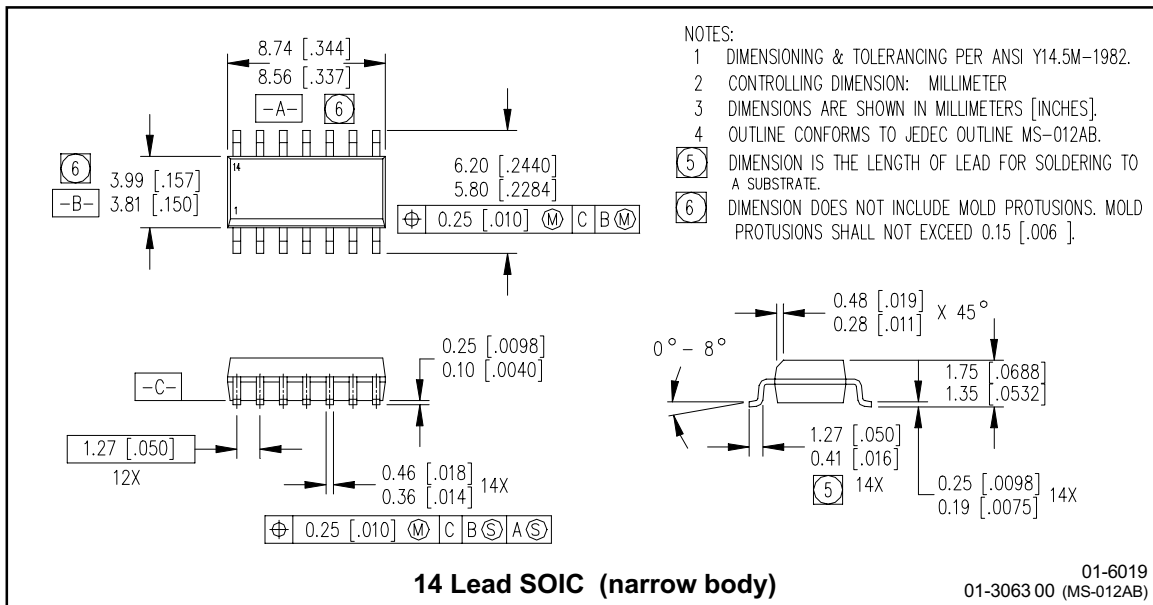
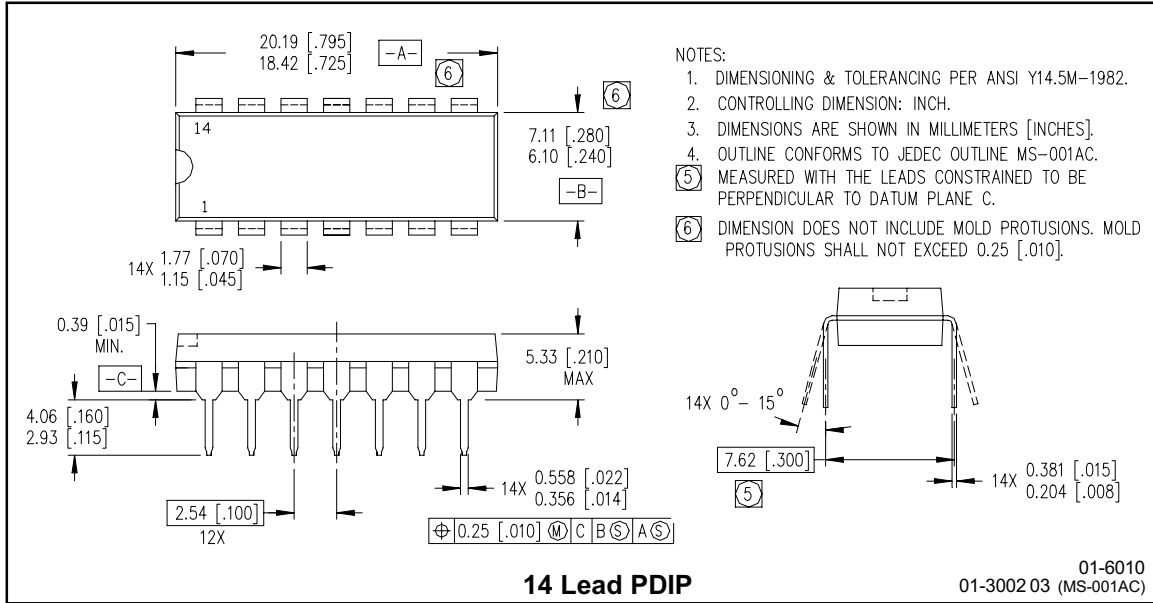
**Figure 38. IRS21064S vs. Frequency (IRFBC40),
 $R_{gate}=15 \Omega$, $V_{CC}=15 V$**



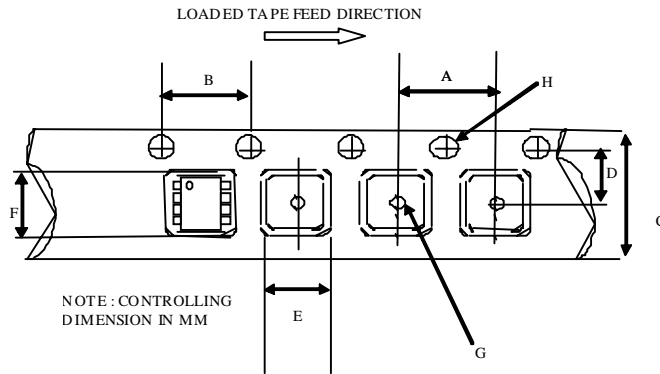
**Figure 39. IRS21064S vs. Frequency (IRFPE50),
 $R_{gate}=10 \Omega$, $V_{CC}=15 V$**

Case Outlines



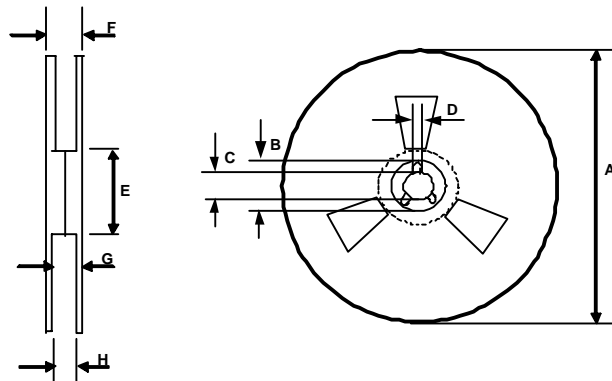


Tape & Reel 8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

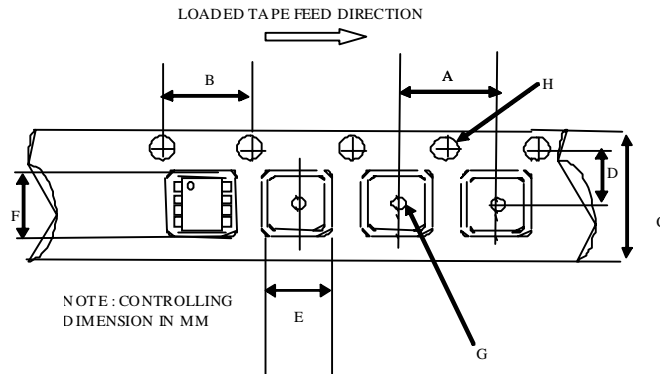
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 8SOICN

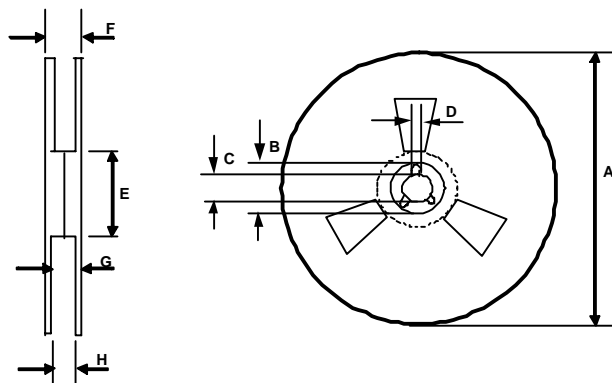
| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

Tape & Reel 14-lead SOIC



CARRIER TAPE DIMENSION FOR 14SOICN

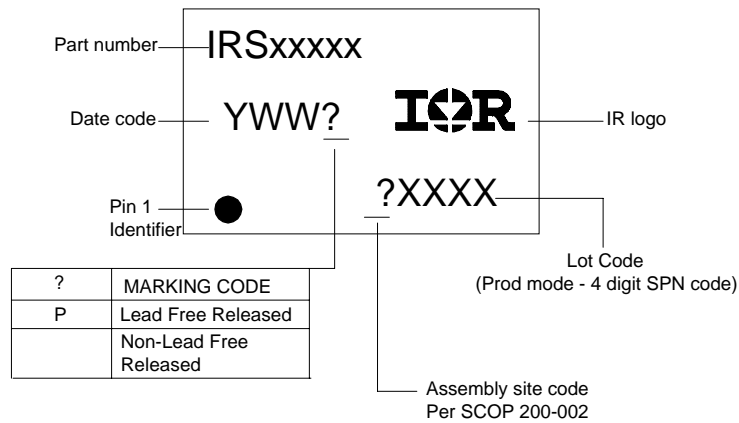
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 15.70 | 16.30 | 0.618 | 0.641 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 6.40 | 6.60 | 0.252 | 0.260 |
| F | 9.40 | 9.60 | 0.370 | 0.378 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 14SOICN

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 22.40 | n/a | 0.881 |
| G | 18.50 | 21.10 | 0.728 | 0.830 |
| H | 16.40 | 18.40 | 0.645 | 0.724 |

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

- | | |
|---------------------------------------|---|
| 8-Lead PDIP IRS2106PbF | 14-Lead PDIP IRS21064PbF |
| 8-Lead SOIC IRS2106SPbF | 14-Lead SOIC IRS21064SPbF |
| 8-Lead SOIC Tape & Reel IRS2106STRPbF | 14-Lead SOIC Tape & Reel IRS21064STRPbF |

SOIC8 & 14 are MSL2 qualified.

This product has been designed and qualified for the industrial level.

Qualification standards can be found at www.irf.com

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
 Data and specifications subject to change without notice. 12/4/2006