AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}^* (V)	74ACT $T_A = +25°C$ $C_L = 50\ pF$	
			Typ	
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	–	2.5
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	–	1.0
t_w	CP Pulse Width HIGH or LOW	5.0	–	3.0

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
 Voltage Range 5.0 V is 5.0 V ±0.5 V.
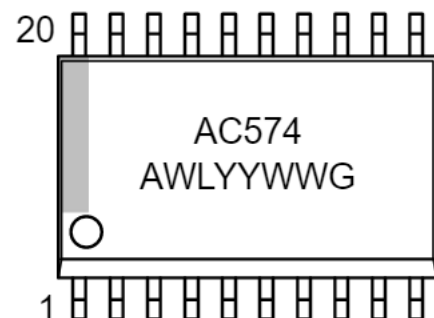
CAPACITANCE

Symbol	Parameter	Value
C_{IN}	Input Capacitance	4.5
C_{PD}	Power Dissipation Capacitance	40

MARKING DIAGRAMS

PDIP−20

MC74AC574N
AWLYYWWG

SOIC−20W

AC574
AWLYYWWG

MC74ACT574N
AWLYYWWG

20

1

ACT574
AWLYYWWG
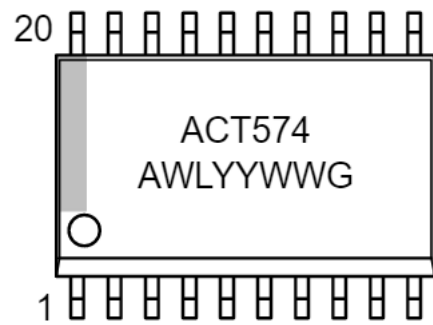
20

1

20

1

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either loc

ORDERING INFORMATION

Device	Package
MC74AC574N	PDIP−20
MC74AC574NG	PDIP−20 (Pb−Free)
MC74ACT574N	PDIP−20
MC74ACT574NG	PDIP−20 (Pb−Free)
MC74AC574DW	SOIC−20
MC74AC574DWG	SOIC−20 (Pb−Free)
MC74AC574DWR2	SOIC−20
MC74AC574DWR2G	SOIC−20 (Pb−Free)
MC74ACT574DW	SOIC−20
MC74ACT574DWG	SOIC−20 (Pb−Free)
MC74ACT574DWR2	SOIC−20
MC74ACT574DWR2G	SOIC−20 (Pb−Free)
MC74AC574DTR2	TSSOP−20*
MC74AC574DTR2G	TSSOP−20*
MC74ACT574DTR2	TSSOP−20*
MC74ACT574DTR2G	TSSOP−20*
MC74AC574M	SOEIAJ−20
MC74AC574MG	SOEIAJ−20 (Pb−Free)
MC74AC574MEL	SOEIAJ−20
MC74AC574MELG	SOEIAJ−20 (Pb−Free)
MC74ACT574M	SOEIAJ−20
MC74ACT574MG	SOEIAJ−20 (Pb−Free)

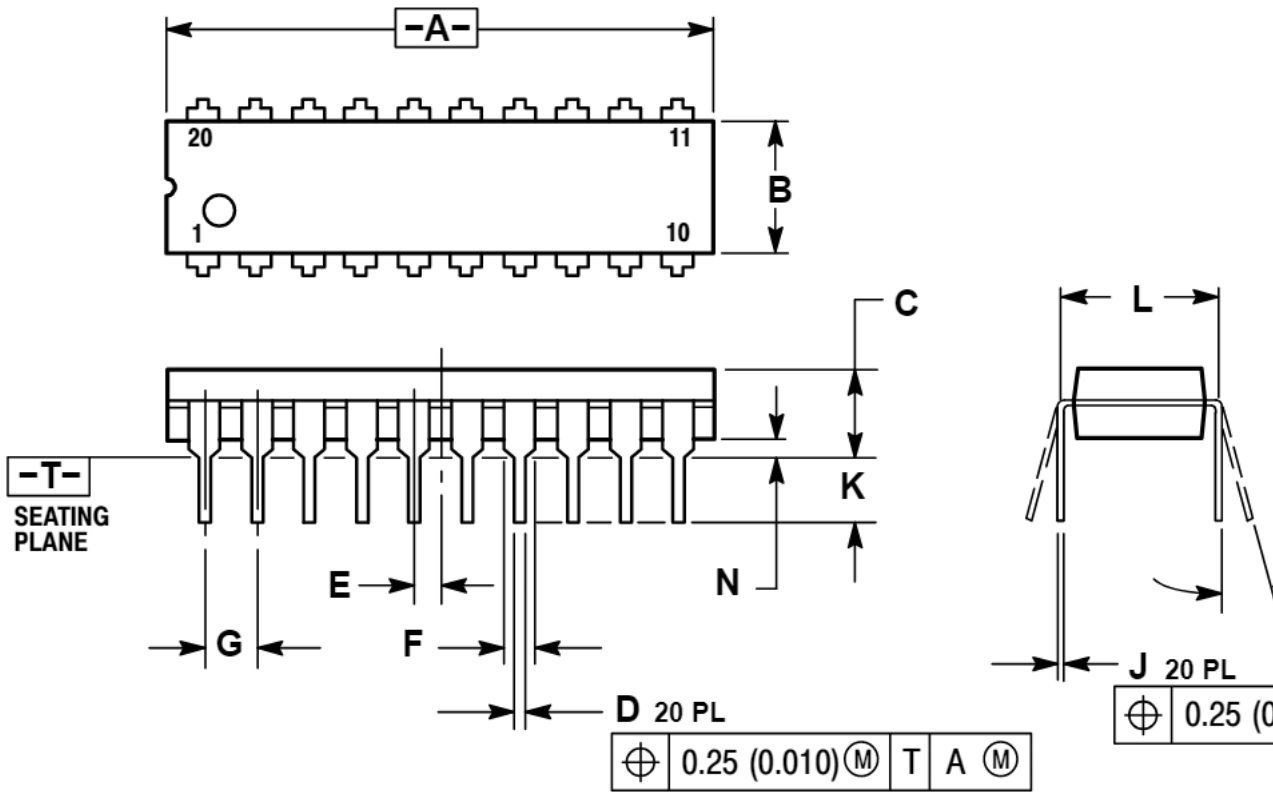|	
MC74ACT574MEL	SOEIAJ-20
MC74ACT574MELG	SOEIAJ-20 (Pb-Free)

†For information on tape and reel specifications, including part orientation and ta[
 Specifications Brochure, BRD8011/D.
*These packages are inherently Pb-Free.

PACKAGE DIMENSION

PDIP−20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738−03
ISSUE E

-A-

20   11

B

1   10

C

-T-
SEATING PLANE

K

E

N

G   F

D 20 PL

⊕ | 0.25 (0.010) Ⓜ | T | A Ⓜ

L

J 20 PL

⊕ | 0.25 (0

SOIC−20W
DW SUFFIX
CASE 751D−05
ISSUE G

D

A

20   11

H

Ⓜ B Ⓜ

E

θ

X 45°

20X **B**

| ⊕ | 0.25 Ⓜ | T | AⓈ | BⓈ |

18X **e**

A

A1

▼ SEATING
PLANE

T

C

L