

P-Channel Enhancement Mosfet

GENERAL DESCRIPTION

The ME7423 P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 13m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 17m\Omega @ V_{GS} = -4.5V$

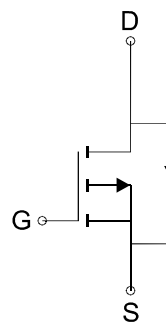
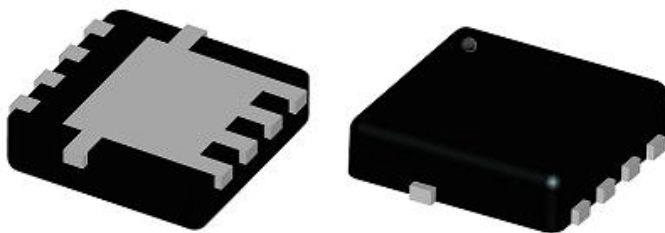
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(DFN 3.3x3.3)

Top View



P-Channel MOSFET

Ordering Information: ME7423S-G (Green product-Halogen free)

Absolute Maximum Ratings (T_j=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V _{DSS}	-30	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (t _J =150°C)	T _A =25°C	I _D	-17	A
	T _A =70°C		-13	
Pulsed Drain Current		I _{DM}	68	A
Maximum Power Dissipation	T _A =25°C	P _D	3.8	W
	T _A =70°C		2.4	
Operating Junction Temperature		T _J	-55 to 150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	33	°C/W

The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ Unless Otherwise Specified)

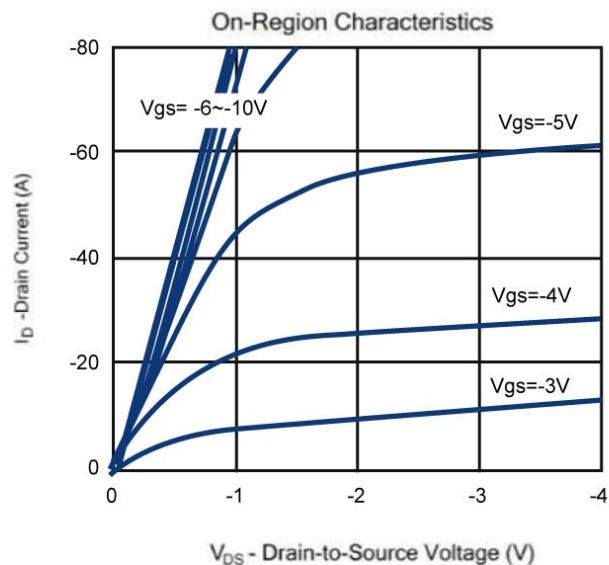
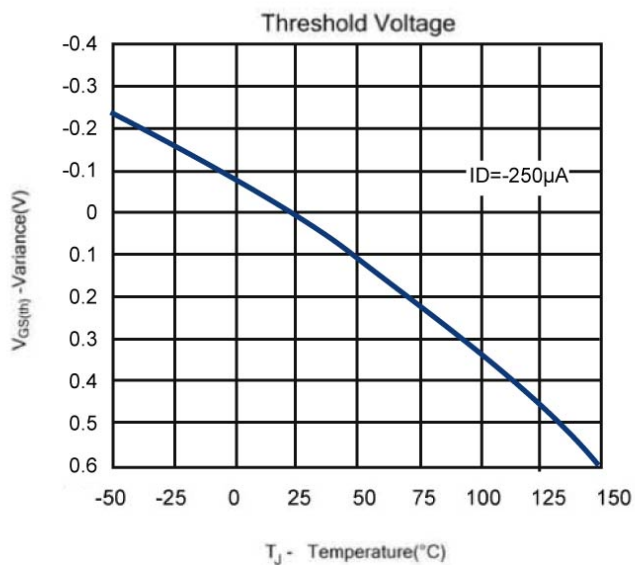
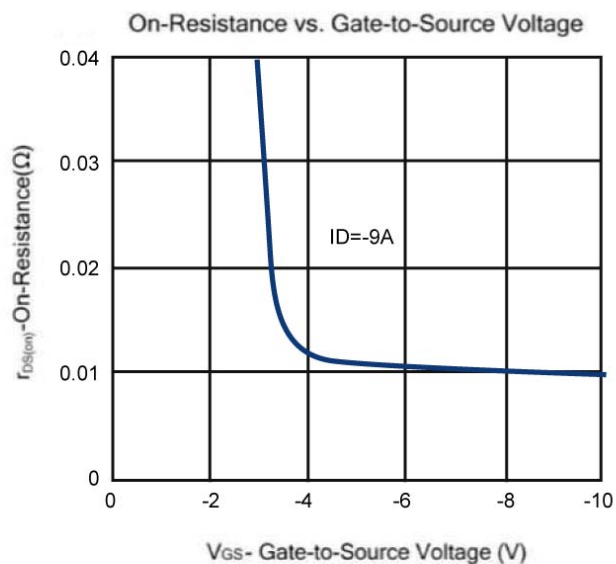
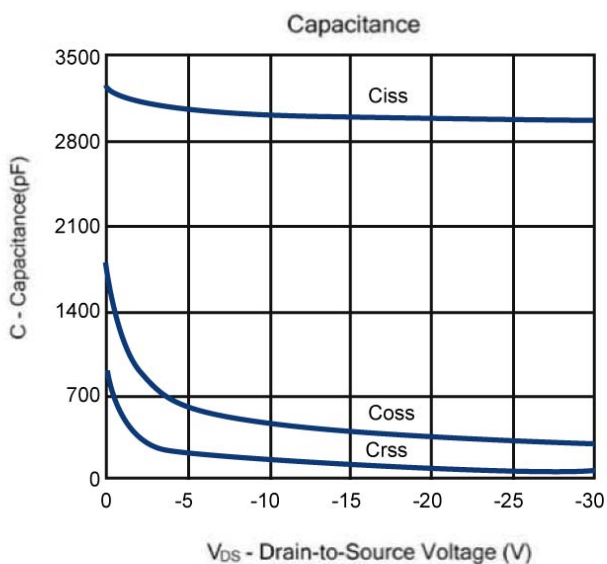
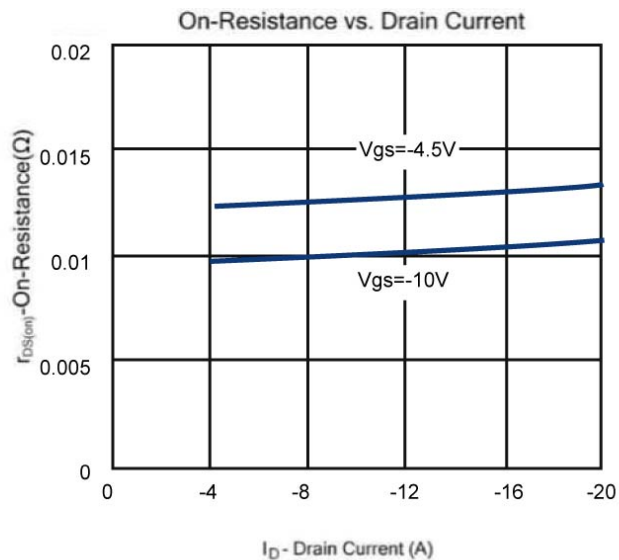
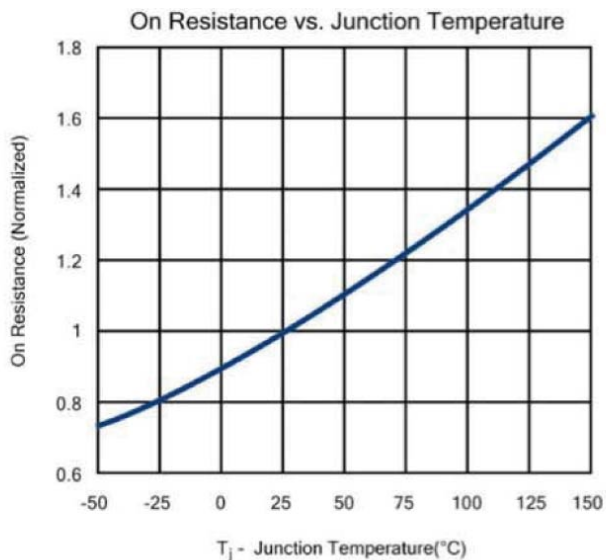
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-3	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$			1	μA
$R_{DS(on)}$	Drain-Source On-State Resistance ^a	$V_{GS}=-10V, I_D=-11.7A$		10	13	m Ω
		$V_{GS}=-4.5V, I_D=-9A$		13	17	
V_{SD}	Diode Forward Voltage	$I_S=-9A, V_{GS}=0V$		0.8	1.2	V
DYNAMIC						
Q_g	Total Gate Charge (-10V)	$V_{DS}=-15V, V_{GS}=-10V,$ $I_D=-11.7A$		70		nC
Q_g	Total Gate Charge (-4.5V)			35		
Q_{gs}	Gate-Source Charge			13		
Q_{gd}	Gate-Drain Charge			17		
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$		3020		pF
C_{oss}	Output Capacitance			400		
C_{rss}	Reverse Transfer Capacitance			135		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=-15V, R_L=15\Omega$ $R_{GEN}=6\Omega, V_{GS}=-10V$		47		ns
t_r	Turn-On Rise Time			20		
$t_{d(off)}$	Turn-Off Delay Time			212		
t_f	Turn-Off Fall Time			61		

Notes: a. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

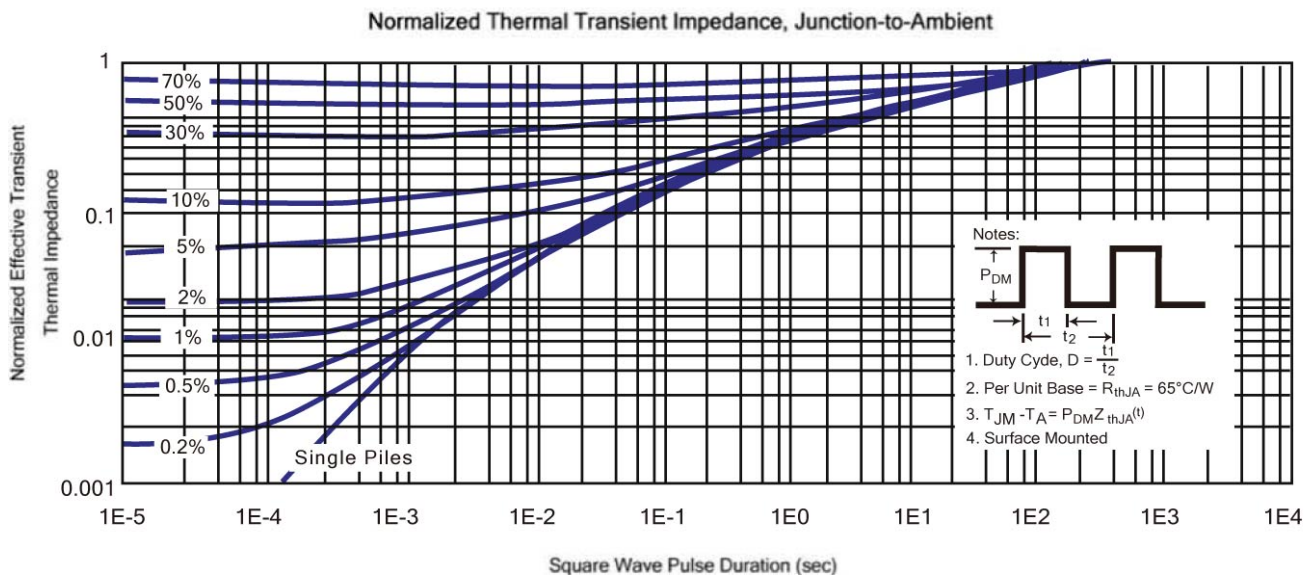
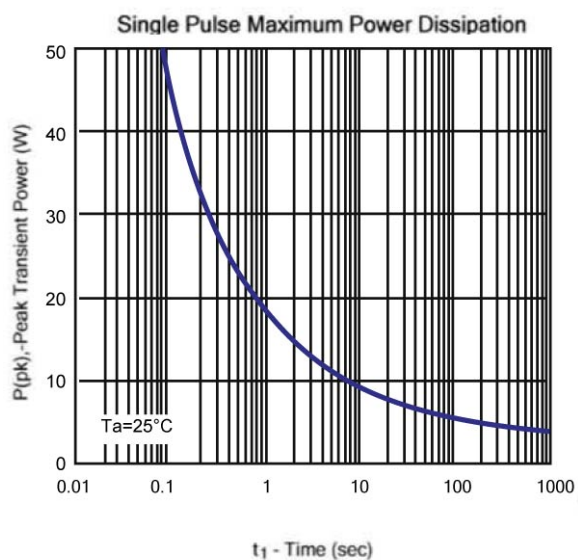
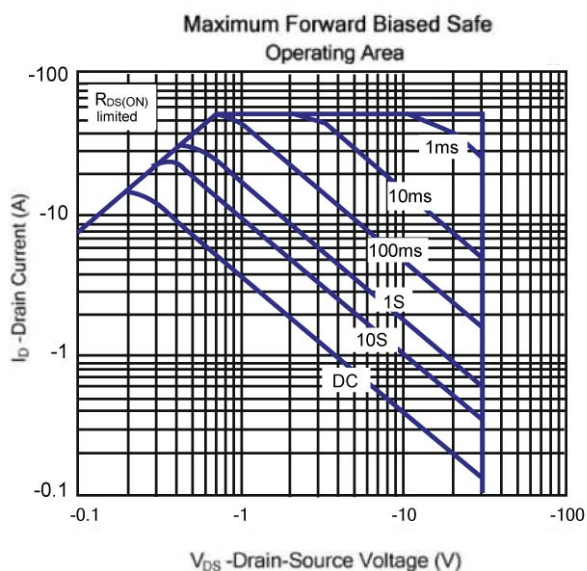
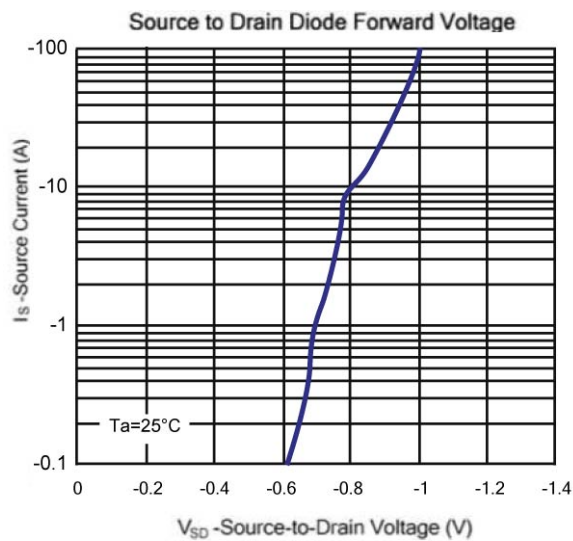
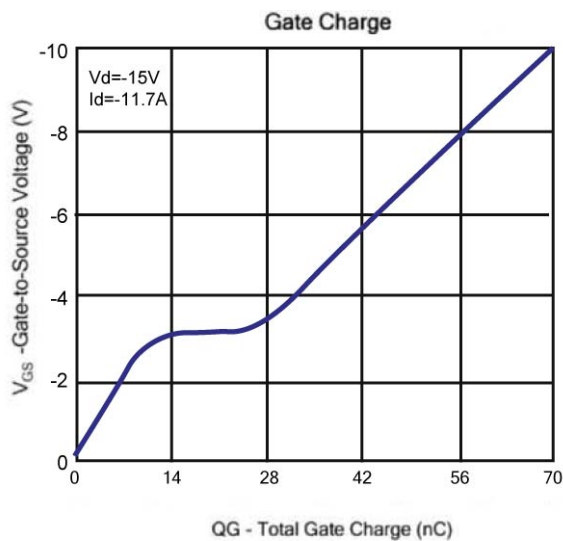
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Typical Characteristics (T_J =25°C Noted)

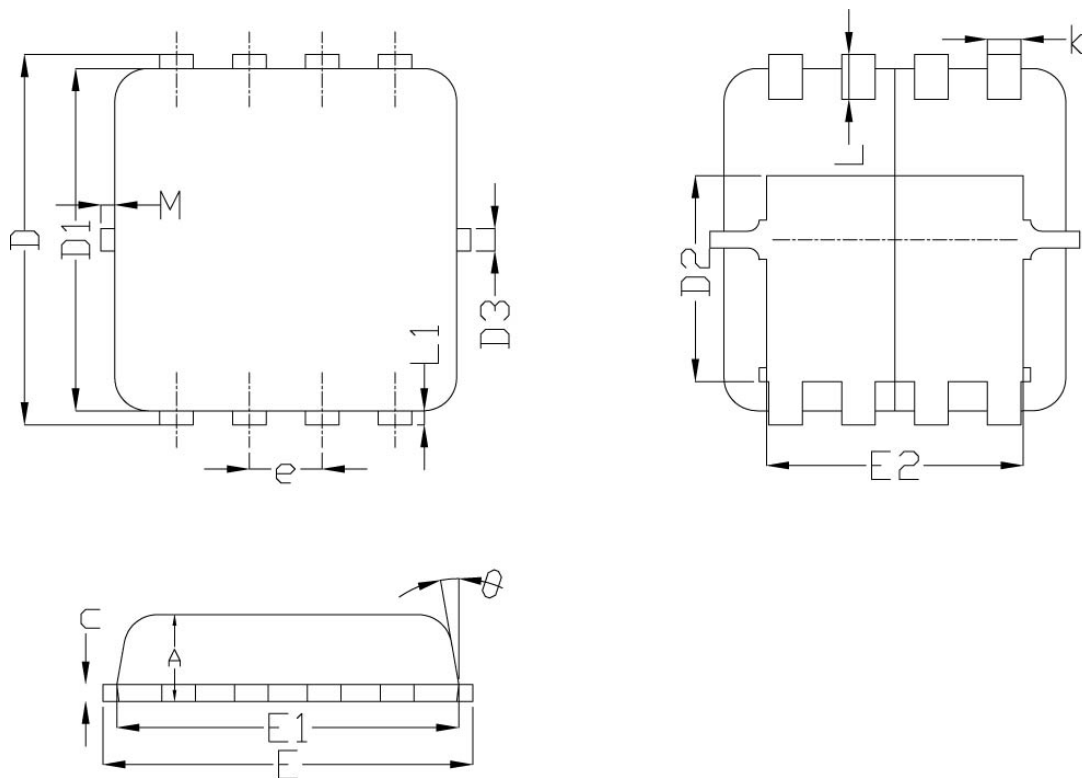


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Typical Characteristics (T_J =25°C Noted)



DFN(S) 3.3x3.3 Package Outline



SYMBOL	MILLIMETERS (mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.27	0.32	0.37
c	0.10	0.15	0.25
D	3.20	3.30	3.40
D1	2.95	3.05	3.15
D2	1.70	1.83	1.96
D3	-	0.20	-
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	-	2.29	-
e	0.65BSC		
θ	0.30	0.40	0.50
L	0.06	0.13	0.20
L1	0	10°	12°
M	-	0.13	-