ME60N04/ME60N04-G

N- Channel 40V (D-S) MOSFET

GENERAL DESCRIPTION

The ME60N04 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

FEATURES

- $R_{DS(ON)} \leqq 12m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 17m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

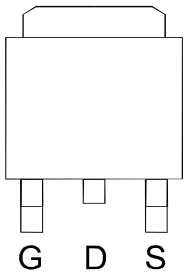
APPLICATIONS

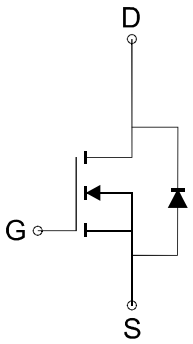
- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- Secondary Synchronous Rectification

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME60N04 (Pb-free)

ME60N04-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Steady	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Tj=150℃,limited by package)	Tc=25℃	I_D	39	A
	Tc=70℃		31	
Pulsed Drain Current		I_{DM}	156	A
Maximum Power Dissipation (Note A)	Tc=25℃	P_D	30	W
	Tc=70℃		18.5	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient(Note A)		$R_{\theta JA}$	42	℃/W
Thermal Resistance-Junction to Case(Note A)		$R_{\theta JC}$	4.3	℃/W

Note A: The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	1.9	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 15A		9	12	mΩ
		V_{GS}=4.5V, I_D= 13A		13	17	
V_{SD}	Diode Forward Voltage	I_S=15A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg (TOT)	Total Gate Charge, V_{GS}=10V	V_{DS}=20V, I_D=15A		31	36	nC
Qg	Total Gate Charge, V_{GS}=4.5V			16	18	
Qgs	Gate-Source Charge			6.5		
Qgd	Gate-Drain Charge			8.3		
Rg	Gate Resistance	Vgs=Vds=0V, f=1MHz		1.6		Ω
Ciss	Input capacitance	V_{DS}=20V, V_{GS}=0V, f=1MHz		1240	1500	pF
Coss	Output Capacitance			170		
Crss	Reverse Transfer Capacitance			60		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=20V, I_D=1A V_{GS}=10V, R_{GEN}=6Ω		16	20	ns
t_r	Turn-On Rise Time			13	17	
$t_{d(off)}$	Turn-Off Delay Time			60	75	
t_f	Turn-On Fall Time			7	10	

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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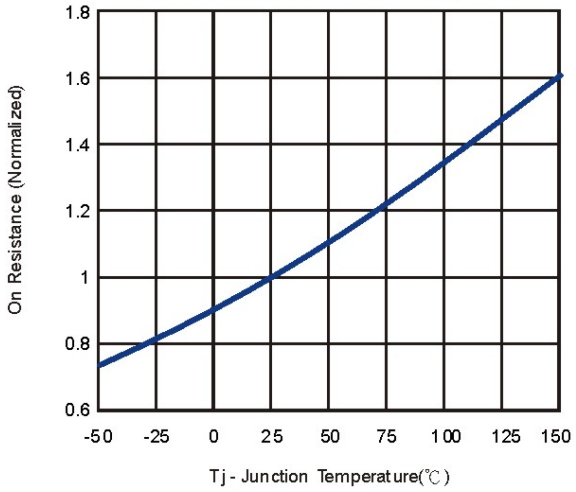
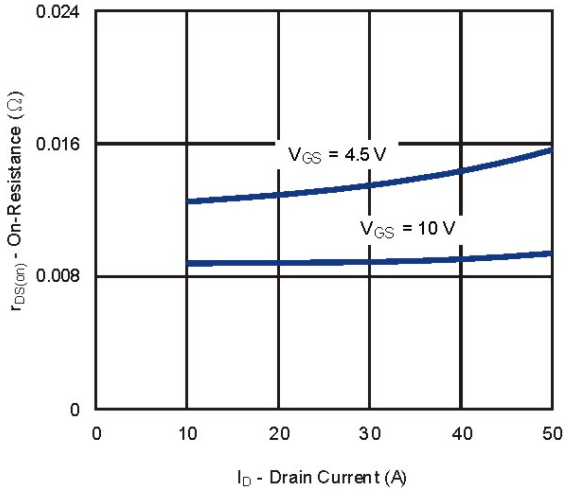
Typical Characteristics (T_J =25℃ Noted)

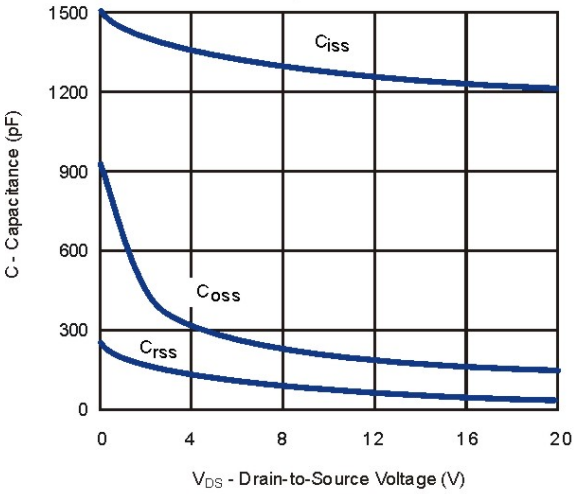
On Resistance vs. Junction Temperature



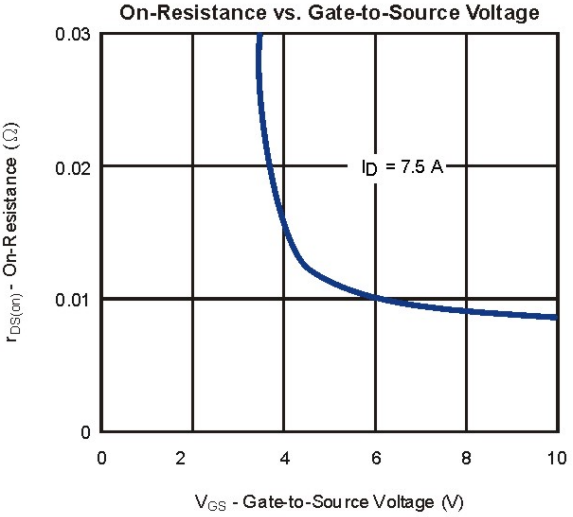
On-Resistance vs. Drain Current



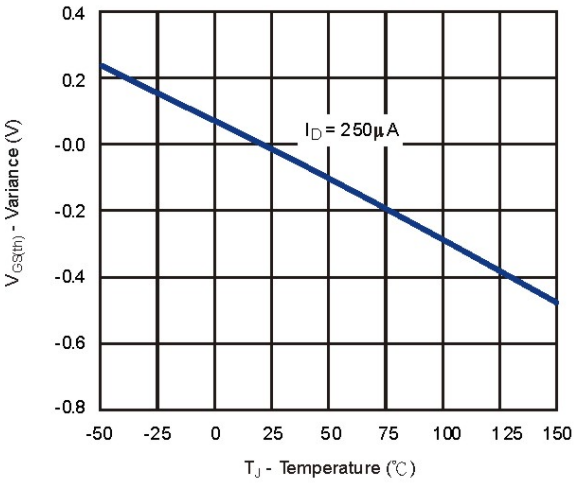
Capacitance



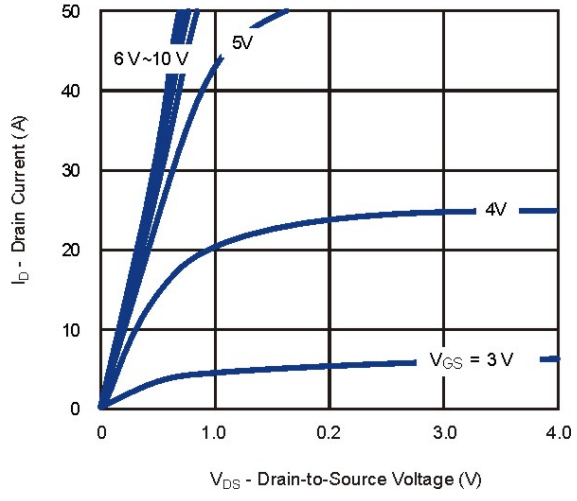
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



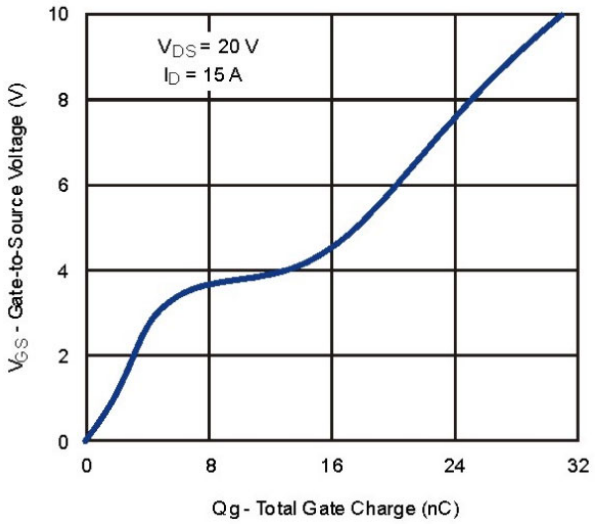
On-Region Characteristics



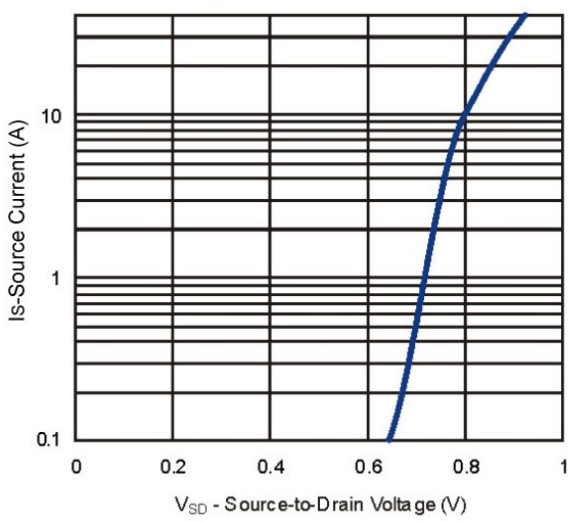
N- Channel 40V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

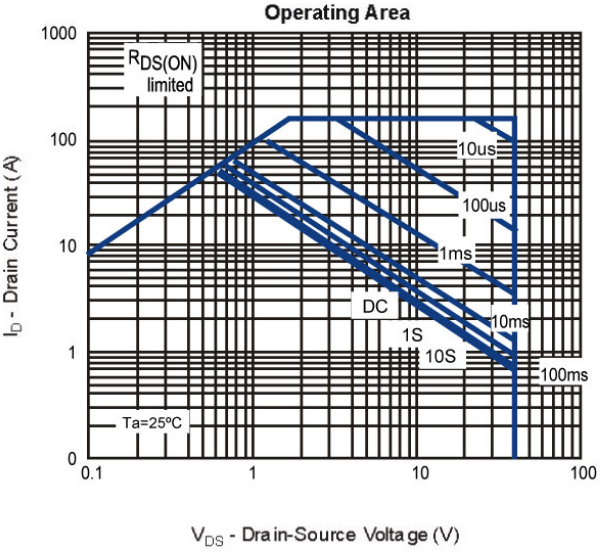
Gate Charge



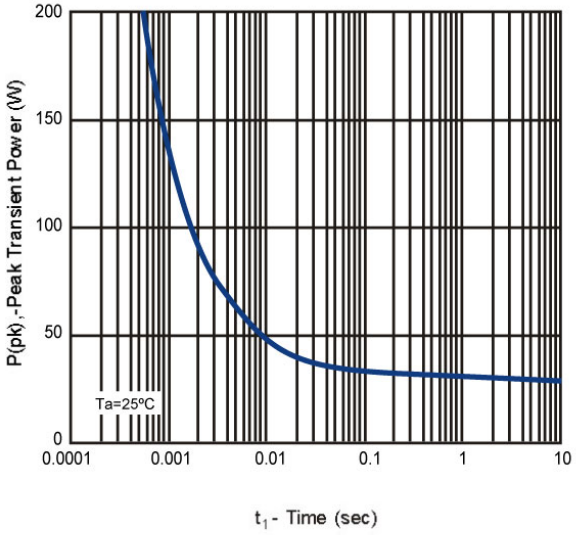
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Case