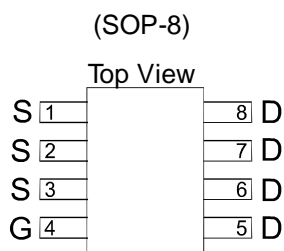


P-Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4457 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

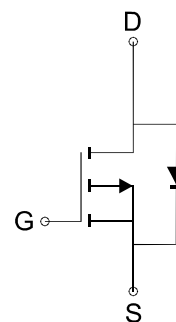


FEATURES

- $R_{DS(ON)} \leq 45m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 68m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



P-Channel MOSFET

Ordering Information: ME4457 (Pb-free)

ME4457-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Steady State	Unit
Drain-Source Voltage	V_{DSS}	-40	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current (Tj=150°C)	I_D	TA=25°C	-5.9
		TA=70°C	-4.7
Pulsed Drain Current	I_{DM}	-24	A
Maximum Power Dissipation	P_D	TA=25°C	2.5
		TA=70°C	1.6
Operating Junction Temperature	T_J	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	50	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper



P-Channel 40-V (D-S) MOSFET
Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0, I_D=-250\ \mu\text{A}$	-40			V
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\ \mu\text{A}$	-1		-3	V
I _{GSS}	Gate Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-40\text{V}, V_{GS}=0\text{V}$			-1	μA
R _{DS(on)}	Drain-Source On-State Resistance	$V_{GS}=-10\text{V}, I_D=-10\text{A}$		37	45	m Ω
		$V_{GS}=-4.5\text{V}, I_D=-8\text{A}$		54	68	
V _{SD}	Diode Forward Voltage	$I_S=-10\text{A}, V_{GS}=0\text{V}$		-0.9	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	$V_{DS}=-20\text{V}, V_{GS}=-10\text{V}, I_D=-5\text{A}$		21		nC
Q _g	Total Gate Charge			10.5		
Q _{gs}	Gate-Source Charge	$V_{DS}=-20\text{V}, V_{GS}=-4.5\text{V}, I_D=-5\text{A}$		5		
Q _{gd}	Gate-Drain Charge			4.5		
C _{iss}	Input capacitance			911		pF
C _{oss}	Output Capacitance	$V_{DS}=-15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		99		
C _{rss}	Reverse Transfer Capacitance			67		
t _{d(on)}	Turn-On Delay Time			36		ns
t _r	Turn-On Rise Time	$V_{DD}=-15\text{V}, R_L=15\ \Omega$		15		
t _{d(off)}	Turn-Off Delay Time	$V_{GEN}=-10\text{V}, R_G=6\ \Omega$		58		
t _f	Turn-On Fall Time			9		

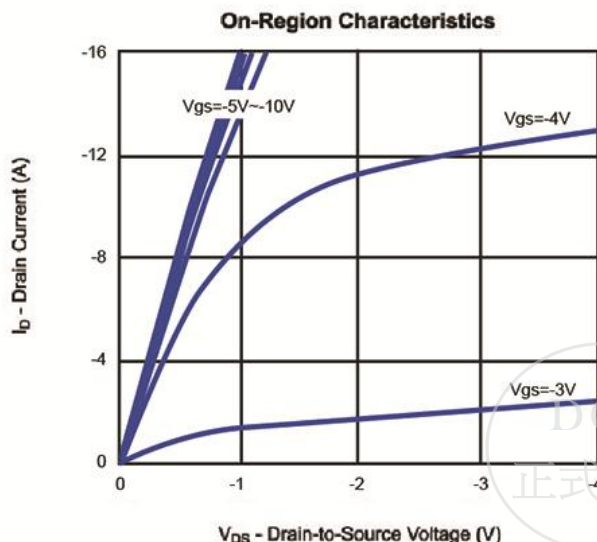
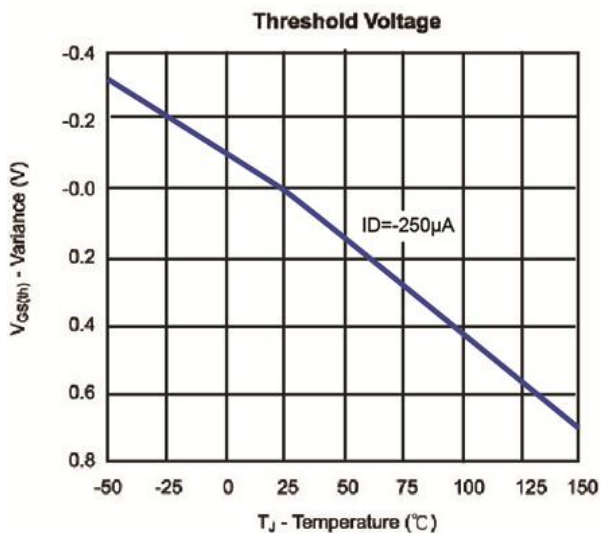
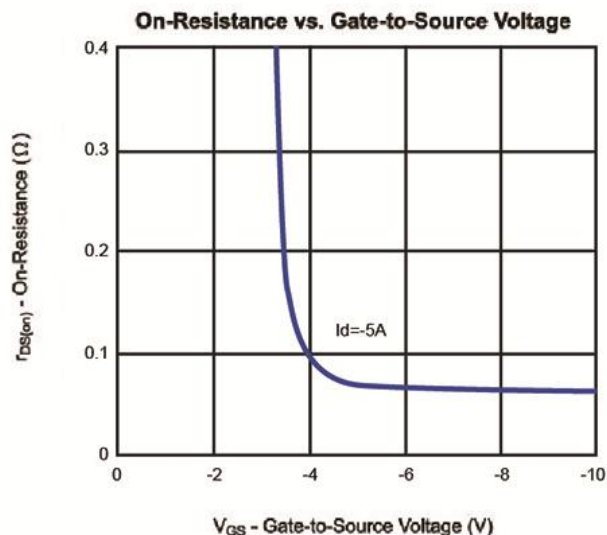
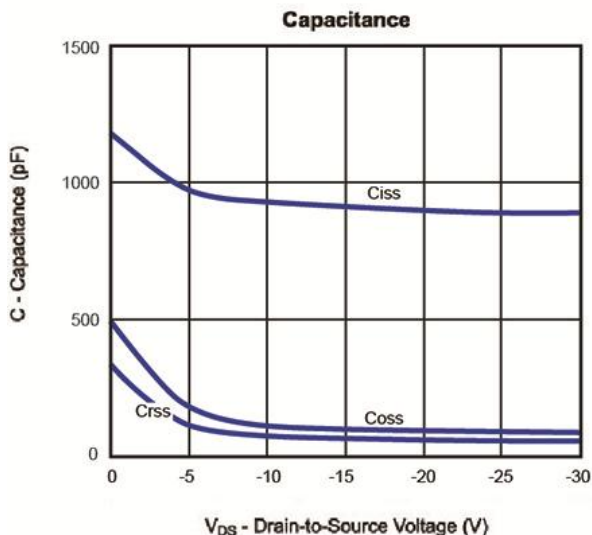
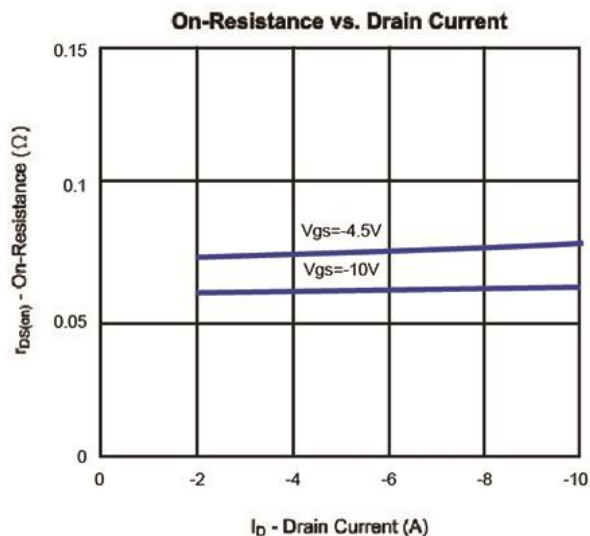
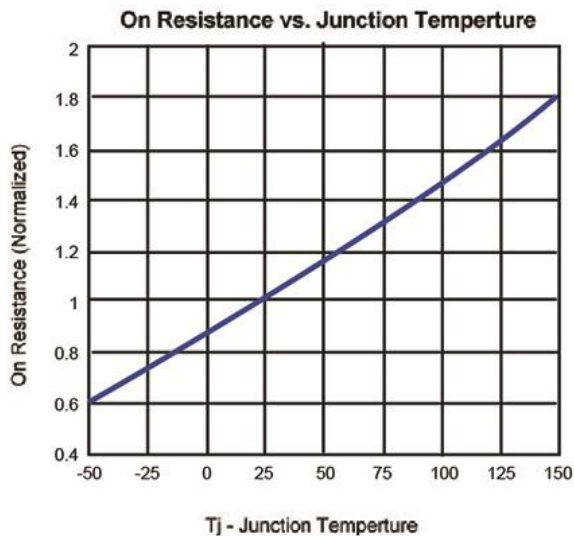
 Notes: a. Pulse test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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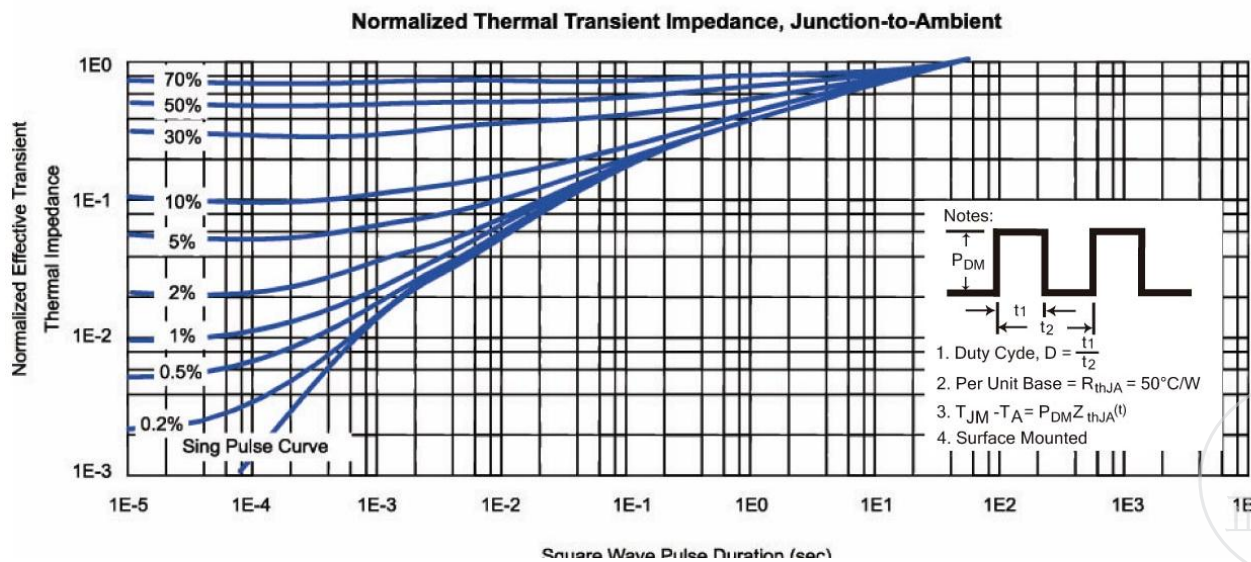
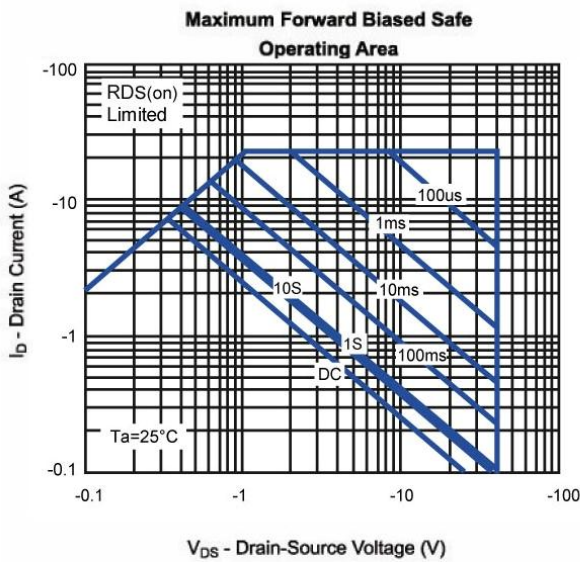
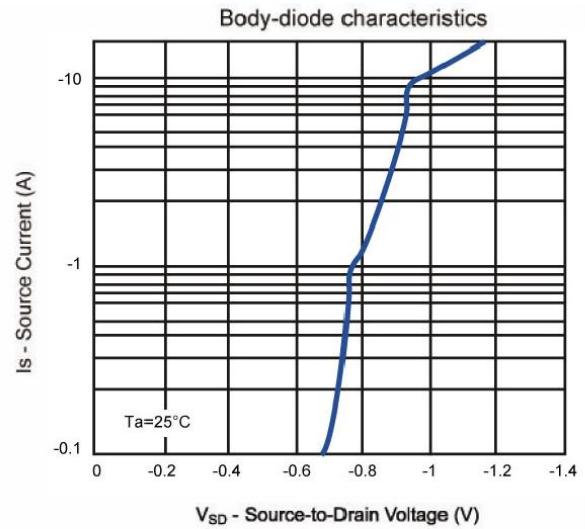
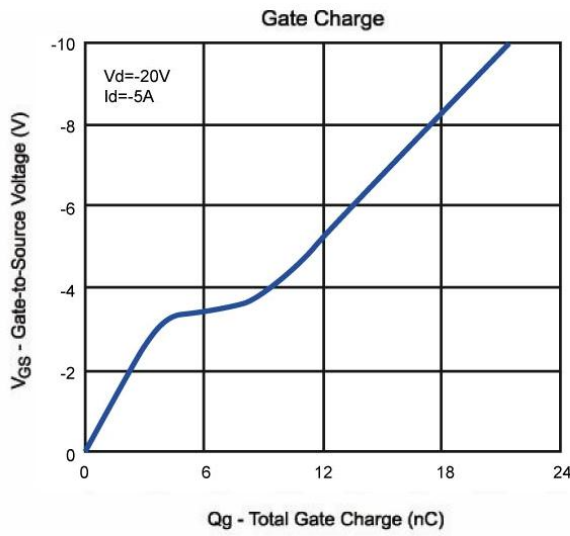
P-Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

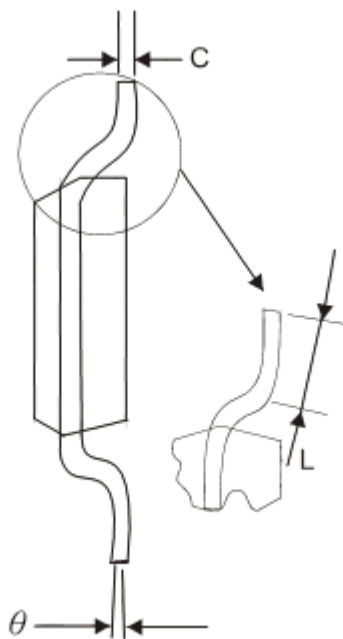
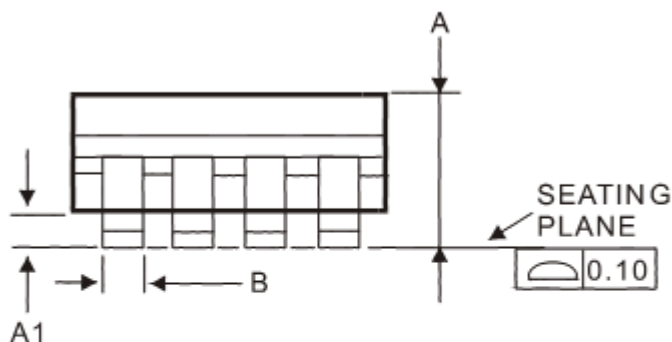
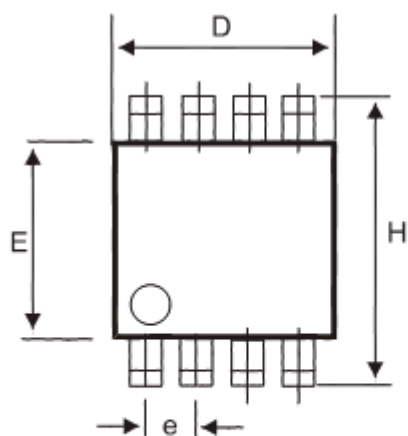


P-Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)



SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

