

**N-Channel 60V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME2308S is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

**FEATURES**

- $R_{DS(ON)} \leq 100m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 130m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- DC/DC Converter
- Load Switch
- LCD Display inverter

**PIN CONFIGURATION**



**Ordering Information:** ME2308S (Pb-free)

ME2308S-G (Green product-Halogen free)

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	$V_{DSS}$	60	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current (Tj=150°C)*	$I_D$	TA=25°C	2.6
		TA=70°C	2.1
Pulsed Drain Current	$I_{DM}$	10	A
Maximum Power Dissipation*	$P_D$	TA=25°C	1.04
		TA=70°C	0.67
Operating Junction & Storage Temperature Range	$T_J$	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	110	°C/W

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

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### Electrical Characteristics (T<sub>A</sub> = 25°C Unless Otherwise Specified)

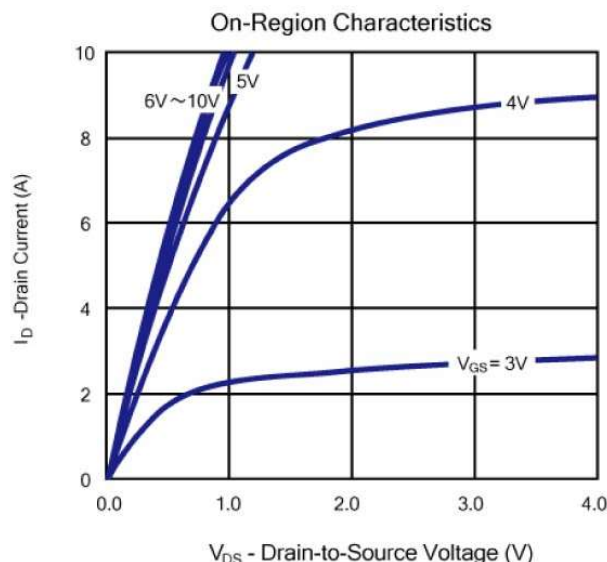
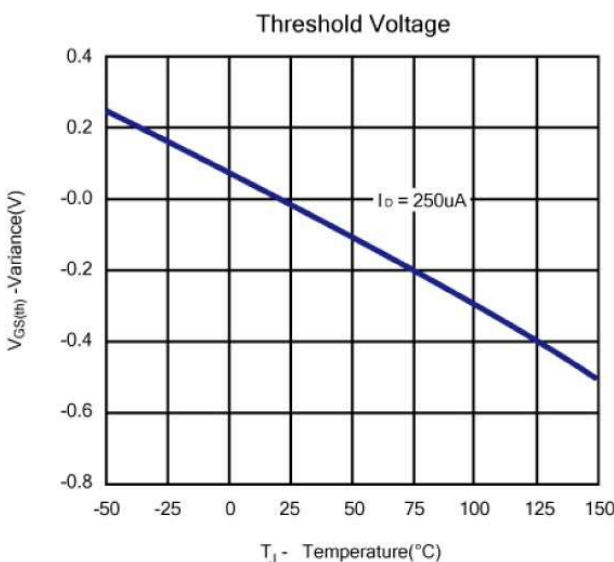
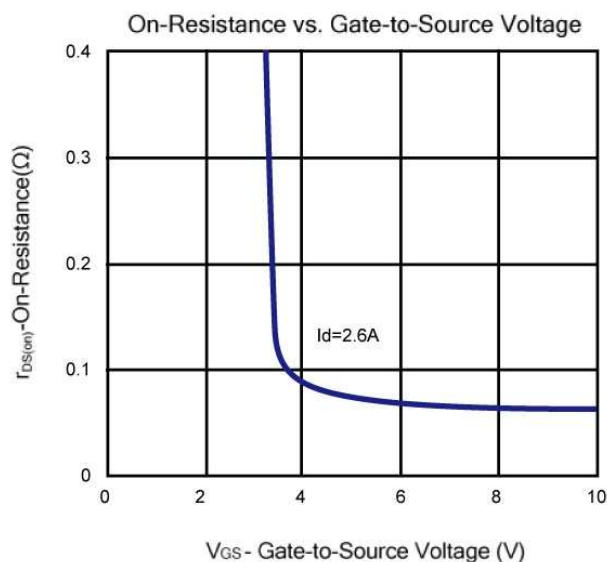
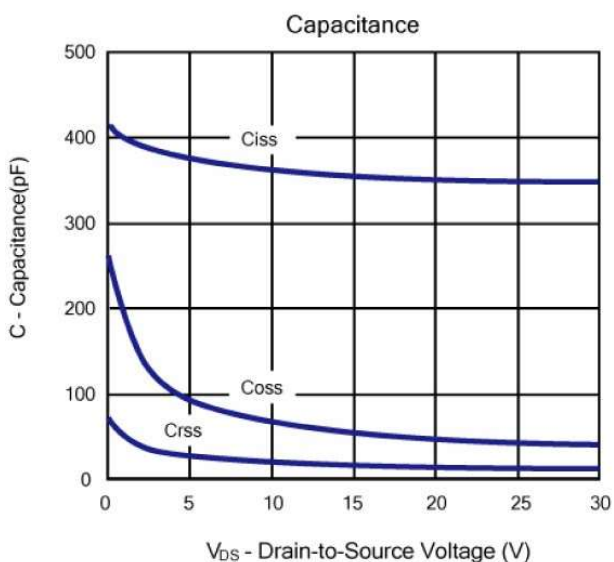
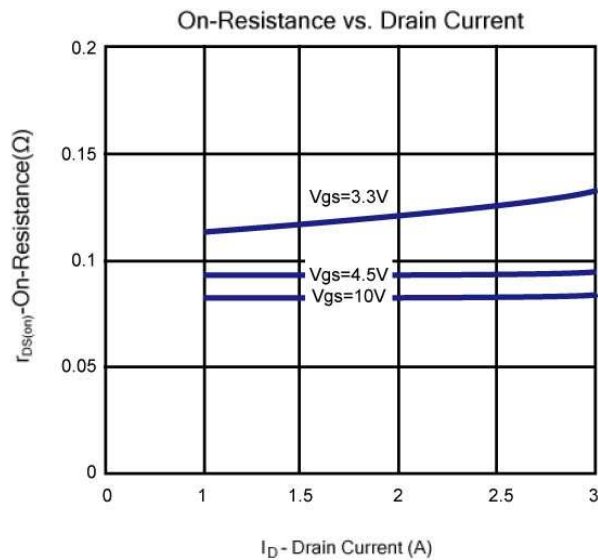
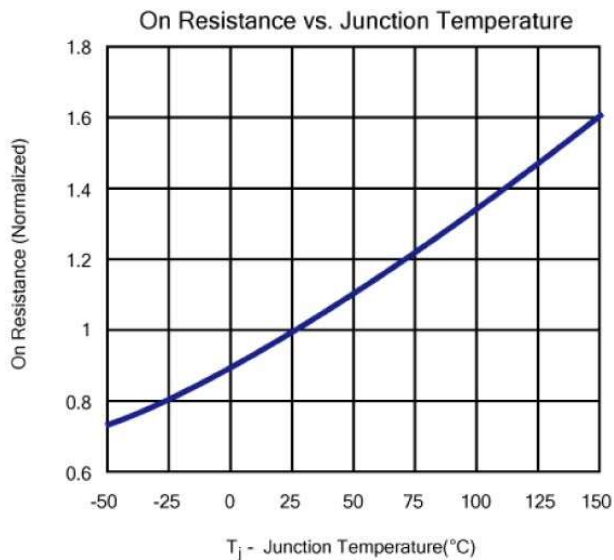
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>DS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	60			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1.0		3.0	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance <sup>a</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> = 2.6A		82	100	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> = 2.1A		96	130	
		V <sub>GS</sub> =3.3V, I <sub>D</sub> = 1.8A		139	200	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.8	1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, V <sub>GS</sub> =10V, I <sub>D</sub> =2.6A		12		nC
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =2.6A		6.5		
Q <sub>gs</sub>	Gate-Source Charge			2.2		
Q <sub>gd</sub>	Gate-Drain Charge			2.7		
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1.0MHz		350		pF
C <sub>oss</sub>	Output Capacitance			40		
C <sub>rss</sub>	Reverse Transfer Capacitance			12		
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		0.7		Ω
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =20V, R <sub>L</sub> =20 Ω I <sub>D</sub> =1A, V <sub>GEN</sub> =10V R <sub>G</sub> =1 Ω		10		ns
t <sub>r</sub>	Turn-On Rise Time			11		
t <sub>d(off)</sub>	Turn-Off Delay Time			29		
t <sub>f</sub>	Turn-Off Fall Time			3		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**



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