1.1A 1.2MHz Synchronous Boost Converter

CJ9311 Series

■ INTRODUCTION:

The CJ9311 devices provide a power supply solution for products powered by either a one-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-ion or Li-polymer battery. The boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency, which contains an internal NMOS switch and PMOS synchronous rectifier. The maximum peak current in the boost switch is typically limited to a value of 1.1A.

A switching frequency of 1.2MHz minimizes solution footprint by allowing the use of tiny, low profile inductors and ceramic capacitors. The current mode PWM design is internally compensated, reducing external parts count. Anti-ringing control circuitry reduces EMI concerns by damping the inductor in discontinuous mode. In shutdown, V_{OUT} and V_{IN} are connected, which allows the input battery to be used for backup power. The device features low shutdown current less than 1μA.

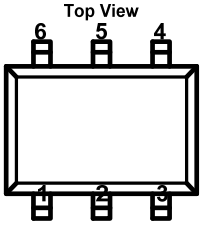
■ FEATURES:

- Up to 96% Efficiency
- Delivers 100mA@3.3V from Single AA Cell
- Delivers 300mA@5V from Two AA Cells
- Delivers 600mA@5V from Single Li Cell
- Maintains High Efficiency Over the Output Current Range for Improved Battery Life
- Low Voltage Start-Up: 0.85V
- Continuous Switching at Light Loads
- Internal Synchronous Rectifier
- Current Mode Control with Internal Compensation
- 1.2MHz Fixed Frequency Switching
- Input Range: 0.9V to5V
- Output Range: 2.5V to 4.5V (Up to 5V with Schottky)
- Logic Controlled Shutdown(<1μA)
- Anti-ringing Control Minimizes EMI
- 1.1A Peak Switch Current Limit
- Over Temperature Protection
- Tiny External Components

■ APPLICATIONS：

- Digital Still and Video Cameras
- Personal Information Appliances
- Wireless and DSL Modems
- Personal Medical Products
- GPS Receivers
- LCD Bias Supplies
- Handheld Instruments
- Portable Audio Players

■ PIN CONFIGURATION



■ DEVICE INFORMATION:

PART NUMBER	PACKAGE
CJ9311T6	SOT-23-6L

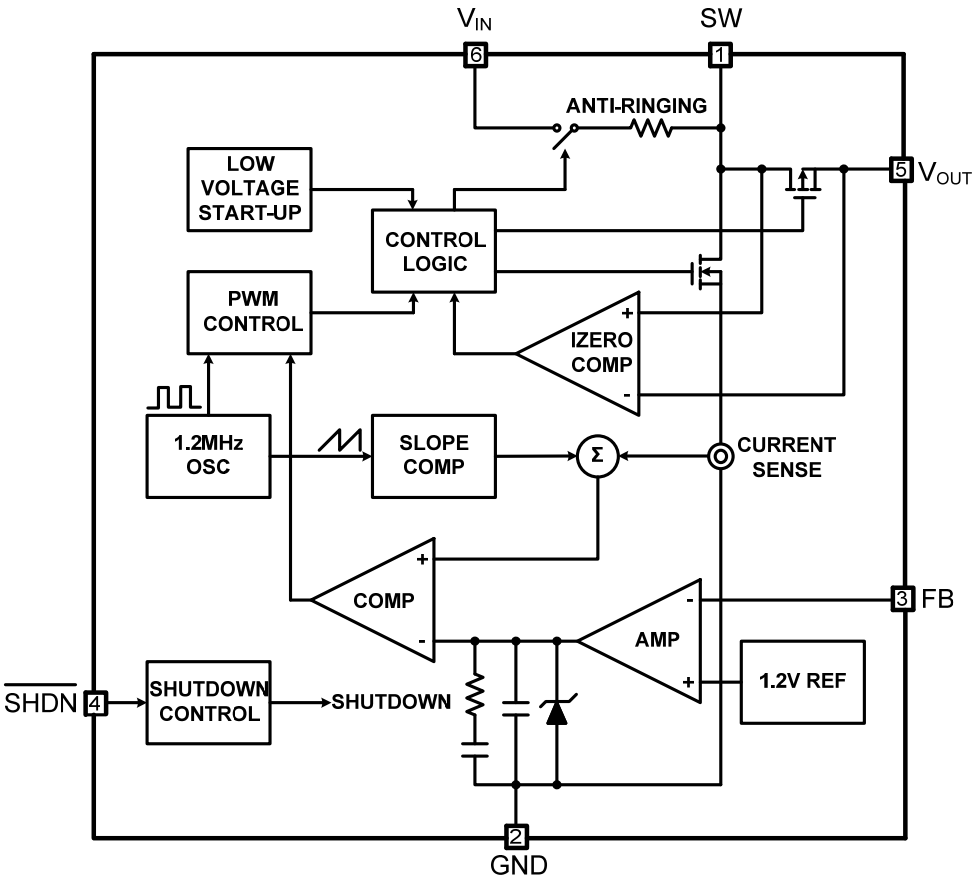
Electrical Characteristics

Table1. Pin Description

PIN NUMBER	PIN NAME	FUNCTION
1	SW	**Switch Pin**. Connect inductor between SW and V_{IN}. Optional Schottky diode is connected between SW and V_{OUT}. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. If the inductor current falls to zero, or CE is low, an internal 100Ω antiringing switch is connected from SW to V_{IN} to minimize EMI.
2	GND	**Signal and Power Ground**. Provide a short direct PCB path between GND and the (–) side of the output capacitor(s). Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.
3	FB/NC	**Feedback Input / Not Connected** (for fixed output voltage option). Feedback Input to the g_m Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 2.5V to 5.5V by: V_{OUT} =1.23V•[1+(R1/R2)] The feedback networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the GND pin. If no analog ground plane is available, then the ground connection of the feedback network must tie directly to the GND pin. The feedback network, resistors R1 and R2 must be connected to FB pin directly as closely as possible. And FB is a sensitive signal node, trace area at FB pin should be small. Please keep FB away from the inductor and SW switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
4	$\overline{SHDN}$	**Logic Controlled Shutdown Input**. $\overline{SHDN}$=High: Normal free running operation , 1.2MHz typical operating frequency. $\overline{SHDN}$=Low: Shutdown; quiescent current <1μA. An 100Ω anti-ringing switch is internally connected between SW and V_{IN}. If $\overline{SHDN}$ is driven from a logic-level output, the logic high-level (on) should be referenced to V_{OUT} to avoid intermittently switching the device on.

PIN NUMBER	PIN NAME	FUNCTION
4	$\overline{SHDN}$	**Note**: If pin $\overline{SHDN}$ is not used, it should be connected directly to pin OUT.V_{OUT} is held at approximately V_{IN} – 0.6V in shutdown due to the body diode of the internal PMOS. Typically, $\overline{SHDN}$ should be connected to V_{IN} through a 1M pull-up resistor. If $\overline{SHDN}$ is undefined, pin SW may ring.
5	V_{OUT}	**DC-DC Power Output** (Drain of the Internal Synchronous Rectifier P-MOSFET) and **Output Voltage Sense Input**. Bias is derived from V_{OUT} when V_{OUT} exceeds 2.3V. PCB trace length from V_{OUT} to the output filter capacitor(s) should be as short and wide as possible. Care should be taken to minimize the loop area formed by the output filter capacitor(s) connections, the V_{OUT} pin, and the SCJ9311 GND pin. The minimum recommended output filter capacitance is 4.7μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the GND pin. V_{OUT} is held at approximately V_{IN} – 0.6V in shutdown due to the body diode of the internal PMOS.
6	V_{IN}	**Battery Supply Input Voltage**. The device gets its start-up bias from V_{IN}. Once V_{OUT} exceeds V_{IN}, bias comes from V_{OUT}. Thus, once started, operation is completely independent from V_{IN}. Operation is only limited by the output power level and the battery's internal series resistance. The V_{IN} pin should be connected to the positive terminal of the battery and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{IN} pin, and the CJ9311 GND pin. The minimum recommended bypass capacitance is 1μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{IN} pin and the GND pin. PCB trace length from V_{IN} to the input filter capacitor(s) should be as short and wide as possible.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS(1)

(Unless otherwise specified, T_A=25°C)

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage(2)	V_{IN}	-0.3~ 7	V
SW Voltage(2)		-0.3~ 7	V
$\overline{SHDN}$ Voltage(2)		-0.3~ 7	V
FB Voltage(2)		-0.3~ 6	V
V_{OUT} Voltage(2)		-0.3~7	V
Peak SW Sink Current	I_{SWMAX}	1500	mA
Power Dissipation SOT23-6	P_D	400	mW
Operating Virtual Junction Temperature Range	T_j	125	℃
Storage Temperature Range	T_{stg}	-40~+125	℃
Lead Temperature (Soldering, 10 sec)	T_{solder}	260	℃
ESD rating(3)	Human Body Model - (HBM)	2000	V
	Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Chipower recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

■ RECOMMENDED OPERATING CONDITIONS

	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	0.9	-	5.5	V
Output voltage at V_{OUT}	2.5	-	5.5	V
Operating free air temperature range(1), T_A	-40	-	85	℃
Operating virtual junction temperature range, T_j	-40	-	125	℃

Electrical Characteristics

Typical values are at T_A=25℃, unless otherwise specified, specifications apply for condition V_{IN} = $V_{\overline{SHDN}}$ = 1.2 V, V_{OUT} = 3.3 V

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
Minimum Start-Up Voltage	V_{START}	I_{LOAD} =1mA		0.85	1	V
Minimum Operating Voltage(2)	V_{IN}	$V_{\overline{SHDN}}$= V_{IN}		0.5	0.65	V
Output Voltage Adjust Range(3)	V_{OUT}		2.5		5	V
Feedback Voltage	V_{FB}		1.192	1.230	1.268	V
Feedback Current(4)	I_{FB}	V_{FB}=1.30V			±30	nA
Quiescent Current (Shutdown)	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$=0V, Not Including Switch Leakage		0.1	1.0	μA
Quiescent Current (Active)	I_Q	Measured On V_{OUT}		300	500	μA
NMOS Switch Leakage	$I_{NMOSSWL}$	$V_{\overline{SHDN}}$=0V,V_{SW}=5.0V		±0.01	±1	μA
PMOS Switch Leakage	$I_{PMOSSWL}$	$V_{\overline{SHDN}}$=0V,V_{SW}=0V		±0.01	±1	μA
NMOS Switch On Resistance(5)	R_{ONNMOS}	V_{OUT} = 3.3V		0.35		Ω
		V_{OUT} = 5.0V(6)		0.20		
PMOS Switch On Resistance(5)	R_{ONPMOS}	V_{OUT} = 3.3V		0.45		Ω
		V_{OUT} = 5.0V(6)		0.30		
NMOS Cycle by Cycle Current Limit(7)	I_{NMOSCL}	V_{IN}=2.5V		1.1		A
Max Duty Cycle	D_{MAX}	V_{FB} = 1.15V	80	87		%
Oscillator Frequency	f_{osc}		0.95	1.2	1.5	MHz
$\overline{SHDN}$ "High" Voltage(8)	$V_{\overline{SHDN}"H"}$		1.5		V_{IN}	V
$\overline{SHDN}$ "Low" Voltage(9)	$V_{\overline{SHDN}"L"}$				0.35	V
$\overline{SHDN}$ Input Current		$V_{\overline{SHDN}}$=5.5V		±0.1	±1	μA

(1) Typical numbers are at 25°C and represent the most likely norm.

(2) Minimum V_{IN} operation after start-up is only limited by the battery's ability to provide the necessary power as it enters a deeply discharged state.

(3) The fixed voltage version effective output voltage.

(4) Bias current flows into FB pin. Specification is guaranteed by design and not 100% tested in production.

(5) Does not include the bond wires. Measured directly at the die.

(6) Specification is guaranteed by design and not 100% tested in production.

(7) Duty cycle affects current limit due to ramp generator.

(8) High Voltage level：Forcing $\overline{SHDN}$ above 1.5V enables the part.

(9) Low Voltage level：Forcing $\overline{SHDN}$ below 0.35V shuts down the device. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave $\overline{SHDN}$ floating.

■ TYPICAL APPLICATION CIRCUITS

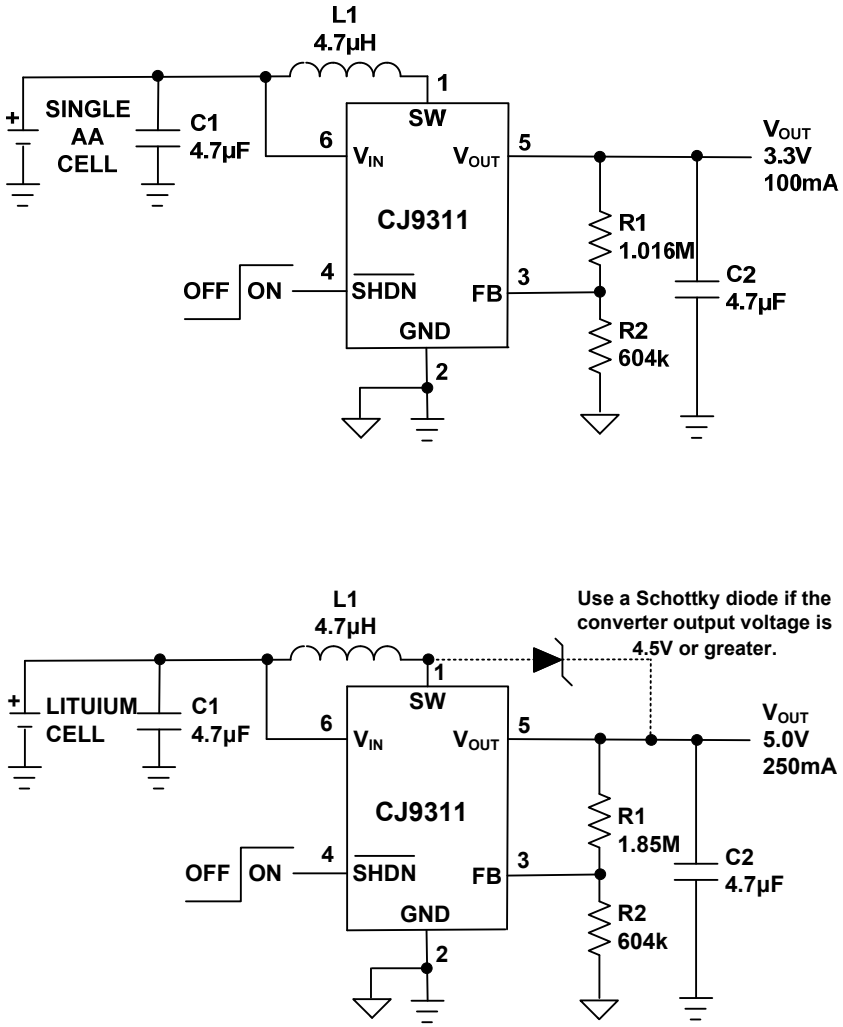
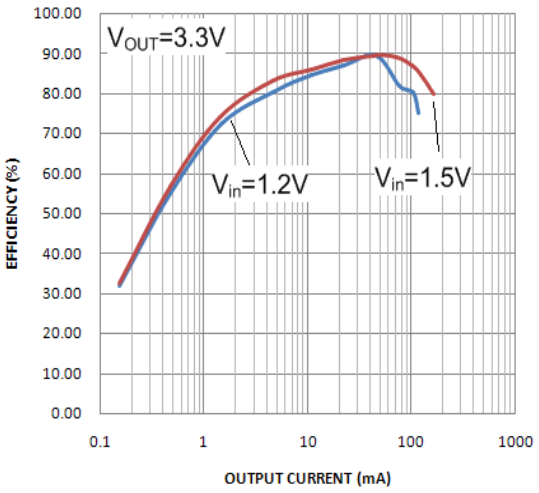


Figure1. Basic Application Circuit

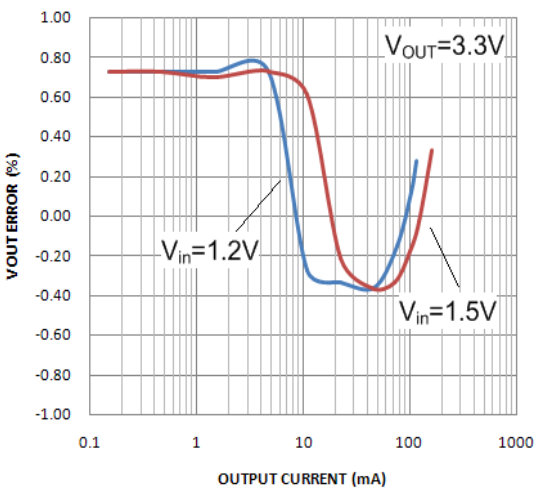
Typical Characteristics

(T_A=25℃, unless otherwise specified, Test Figure1 above)

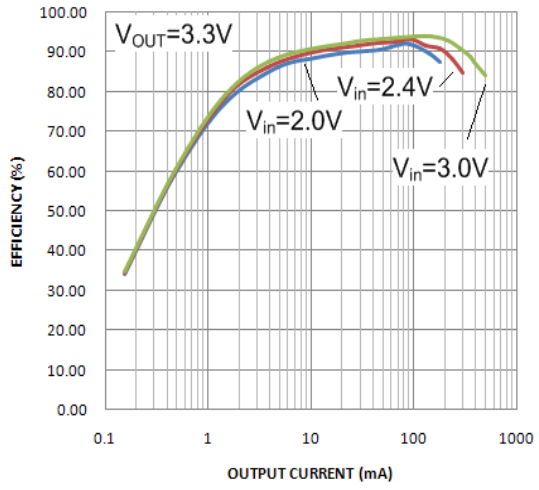
Efficiency vs Output Current



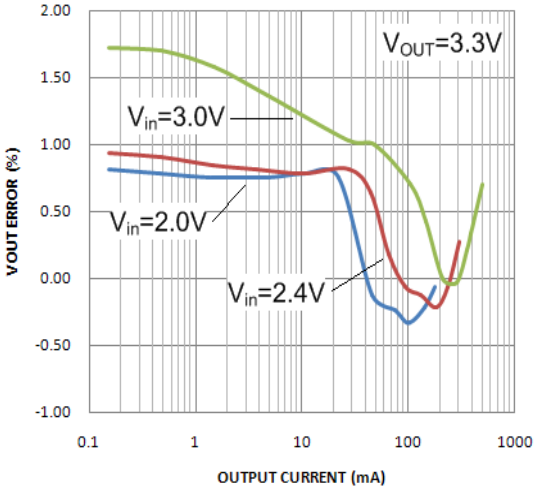
Load Regulation



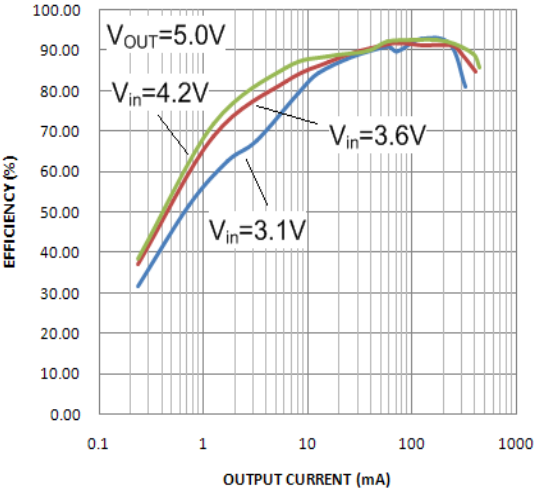
Efficiency vs Output Current



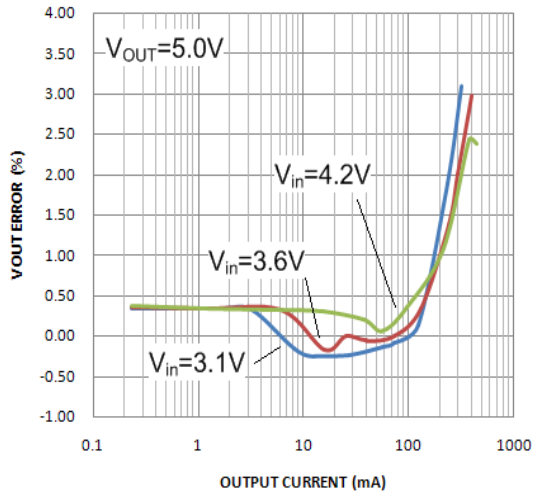
Load Regulation



Efficiency vs Output Current

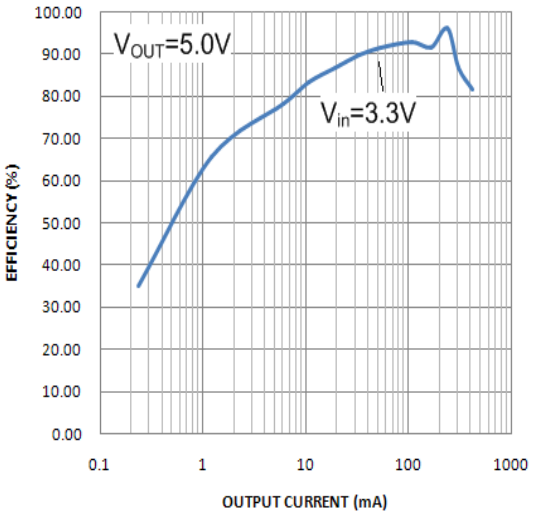


Load Regulation

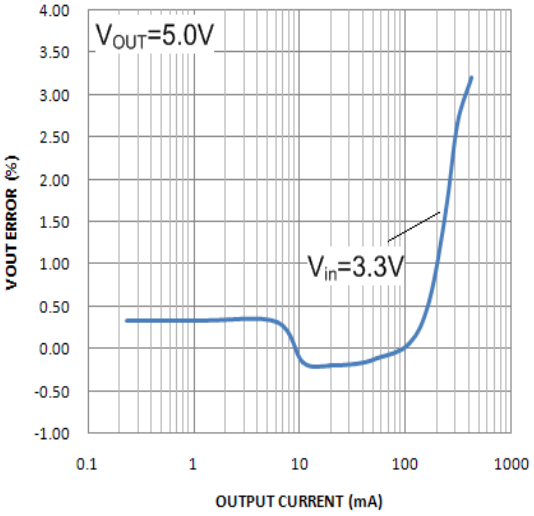


Typical Characteristics

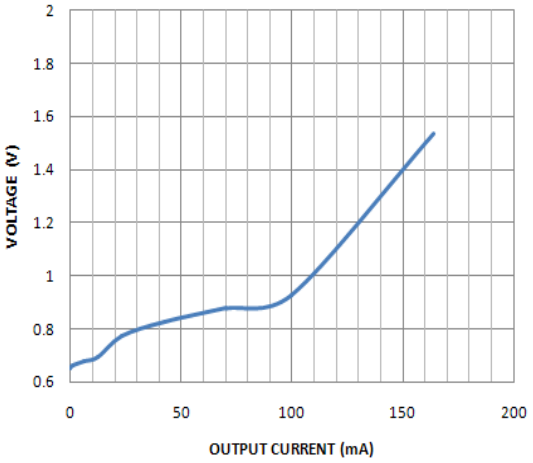
Efficiency vs Output Current



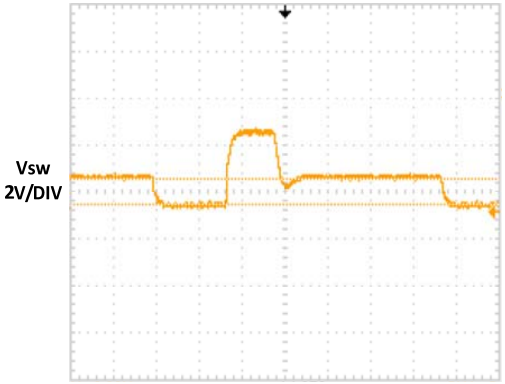
Load Regulation



Minimum Start-Up Voltage vs Output Current



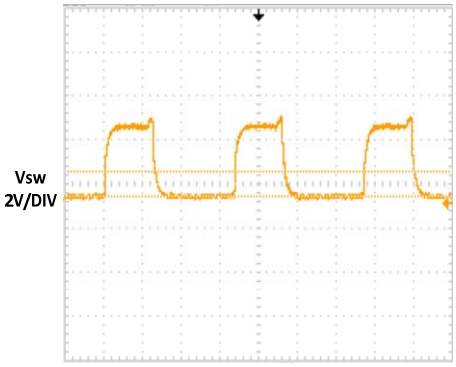
SW Pin Antiringing Operation



VIN=1.3V VOUT=3.3V
IOUT=10mA L=4.7µH
COUT=4.7µF

250ns/DIV

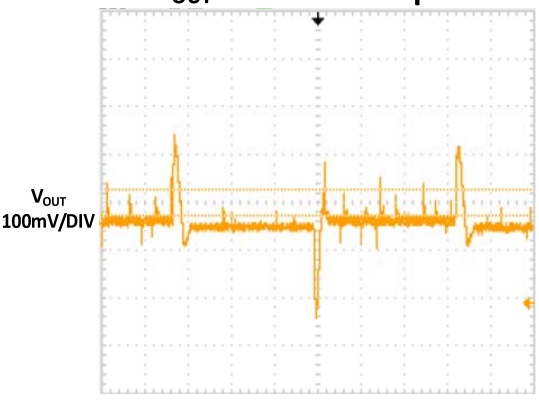
SW Pin Continuous Current Operation



VIN=1.3V VOUT=3.3V
IOUT=50mA L=4.7µH
COUT=4.7µF

250ns/DIV

V_{OUT} Transient Response



VIN=1.3V VOUT=3.3V
IOUT=40mA TO 100mA
L=4.7µH COUT=4.7µF

250µs/DIV

■ DETAILED DESCRIPTION

The CJ9311 high efficiency synchronous boost converter. Able to operate from an input voltage below 1V, the devices feature fixed frequency, current mode PWM control for exceptional line and load regulation. With its low $R_{DS(ON)}$ and gate charge internal MOSFET switches, the devices maintain high efficiency over a wide range of load current. Detailed descriptions of the three distinct operating modes follow. Operation can be best understood by referring to the Block Diagram.
The high 1.2MHz switching frequency of the CJ9311 facilitates output filter component size reduction for improved power density and reduced overall footprint. It also provides greater bandwidth and improved transient response over other lower frequency step-up converters. The compensation and feedback is integrated with only three external components needed.

Synchronous Rectification

The CJ9311 integrates a synchronous rectifier to improve efficiency as well as to eliminate the need for an external Schottky diode. The synchronous rectifier is used to reduce the conduction loss contributed by the forward voltage of an external Schottky diode.
The synchronous rectifier is realized by a P-channel MOSFET (PMOS) with gate control circuitry that incorporates relatively complicated timing concerns. An external Schottky diode is required when the output voltage is greater than 4.5V.

START-UP AND INRUSH CURRENT LIMIT

The start-up sequence of the CJ9311 series depending upon whether the input voltage is greater than or less than 2.3V. Under 2.3V, a start-up oscillator operating at 20% duty cycle controls the synchronous power stage charges,
the output current is limited to 300mA until the output up to 2.3V. For an input voltage greater than 2.3V, the output is charged at a fixed 1.2MHz frequency. The boost converter then takes control and continues to charge the output to the steady-state voltage. The boost converter N-channel switch current is limited to 1.1A and the typical start-up time is 0.5ms.

SLOPE COMPENSATION

Slope compensation provides stability in constant frequency architecture by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 50%.
This control topology features stable switching and cycle-by-cycle current limiting which can prevent the main switch from overstress and the external inductor from saturating, it provides excellent load and line response,

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator: The frequency of operation is internally set to 1.2MHz.
Current Sensing: A signal representing NMOS switch current is summed with the slope compensator. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. Peak switch current is limited to approximately 1A independent of input or output voltage. The current signal is blanked for 40ns to enhance noise rejection.
Zero Current Comparator: The zero current comparator monitors the inductor current to the output and shuts off the synchronous rectifier once this current reduces to approximately 20mA. This prevents the inductor current from reversing in polarity improving efficiency at light loads.
Antiringing Control: The antiringing control circuitry prevents high frequency ringing of the SW pin as the inductor current goes to zero by damping the resonant circuit formed by L and C_{SW} (capacitance on SW pin).

Device Shutdown

When $\overline{SHDN}$ is set logic high, the CJ9311 is put into active mode operation. If $\overline{SHDN}$ is set logic low, the device is put into shutdown mode and consumes less than 1μA of current from battery. In shutdown, the battery input is connected to the output through the inductor and the internal synchronous rectifier P-MOSFET. Due to the body diode of the internal synchronous rectifier P-MOSFET, V_{OUT} is held at approximately V_{IN} - 0.6V during shutdown. This allows the input battery to provide backup power for devices such as an idle microcontroller, memory, or real-time-clock, without the usual diode forward drop. In this way a separate backup battery is not needed.
After start-up, the internal circuitry is supplied by V_{OUT}, however, if shutdown mode is enabled, the internal circuitry will be supplied by the input source again.

■ APPLICATION INFORMATION

The basic CJ9311 application circuits are shown in Figure 1.External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

SETTING THE OUTPUT VOLTAGE

Figure1 shows the basic application circuit of CJ9311 adjustable output version. The internal 1.23V reference voltage is compared to the voltage at the FB pin to generate an error signal at the output of the error amplifier. A voltage divider from V_{OUT} to ground programs the output voltage via FB from 2.5V to 5V using the Equation 1:

V_{OUT} = 1.23V • [1 + (R1/R2)] (1)

Table 2 lists the recommended values for particular output voltage settings.

Table 2. Resistor Selection for V_{OUT} Setting

V_{OUT}	R1(Ω)	R2(Ω)
3.3V	1.02M	604K
5.0V	1.02M	332K

Fixed Output Voltage

The CJ9311 has two fixed output voltage options: 3.3V and 5V. An internal resistor divider is connected to the FB pin inside the package which eliminates the need for external feedback resistors. When designing with the fixed output voltage option, remember to leave the FB pin open; otherwise the output voltage will be affected. However, a feed-forward capacitor can still be added between the FB and V_{OUT} pins to enhance the control loop performance.

INDUCTOR SELECTION

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required.

The CJ9311 can utilize small surface mount and chip inductors due to their fast 1.2MHz switching frequency.

To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the CJ9311's switch is 1.1A. The highest peak current through the inductor and the switch depends on the output load, the input (V_{IN}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current is done using Equation 2:

$$I_L = I_O \times \frac{VOUT}{VBAT \times 0.8} \quad (2)$$

For example, for an output current of 75mA at 3.3 V, at least 340mA of average current flows through the inductor at a minimum input voltage of 0.9 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. The inductor current ripple is typically set for 20% to 40% of the maximum average inductor current (I_L). A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time rises at load changes. In addition, a larger inductor increases the total system costs. With these parameters, it is possible to calculate the value for the inductor by using Equation 3:

$$L = \frac{VBAT \times (VOUT - VBAT)}{\Delta I_L \times f \times VOUT} \quad (3)$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 40% ΔI_L. In this example, the desired inductor has the value of 4μH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. In typical applications, a 4.7μH inductance is recommended. The device has been optimized to operate with inductance values between 2.2μH and 10μH. Nevertheless, operation with higher inductance values may be possible in some applications. Detailed stability analysis is then recommended. Care must be taken because load transients and losses in the circuit can lead to higher currents as estimated in Equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The third parameter for choosing the inductor is the saturation current rating of the inductor. The inductor saturation current rating must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L} \quad (4)$$

High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low ESR (series resistance of the windings) to reduce the I^2R power losses, and must be able to handle the peak inductor current without saturating. Molded chokes and some chip inductors usually do not have enough core to support the peak inductor currents of 1.1A seen on the CJ9311. To

minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. Different core materials and shapes will change the size/current and price/current relationship of an inductor. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the CJ9311 requires to operate. Table 3 shows some typical surface mount inductors that work well in CJ9311 applications.

Table3. Representative SMD Inductors

Part Number	Value (μH)	Max DCR (mΩ)	Rated DC Current (A)	Size W×L×H (mm)
Sumida CDRH 3D16	2.2 3.3 4.7	75 110 162	1.20 1.10 0.90	3.8×3.8×1.8
Sumida CR43	2.2 3.3 4.7	71.2 86.2 108.7	1.75 1.44 1.15	4.3×4.8×3.5
Sumida CDRH 4D18	2.2 3.3 4.7	75 110 162	1.32 1.04 0.84	4.7×4.7×2.0

OUTPUT AND INPUT CAPACITOR SELECTION

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 5:

$$C_{min} = \frac{I_O \times (VOUT - VBAT)}{f \times \Delta V \times VOUT} \quad (5)$$

Parameter f is the switching frequency and Δ V is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 4.5μF is needed. In this value range, ceramic capacitors are a good choice. The ESR and the additional ripple created are negligible. It is calculated using Equation 6:

$$\Delta V_{ESR} = I_O \times R_{ESR} \quad (6)$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor has to completely supply the load during the charging phase of the inductor. The value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of 4.5μF and load transient considerations, the recommended output capacitance value is in a 10 μF range.

Care must be taken on capacitance loss caused by derating due to the applied dc voltage and the frequency characteristic of the capacitor. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the same frequency range as the CJ9311 operating frequency. So the effective capacitance of the capacitors used may be significantly lower. Therefore, the recommendation is to use smaller capacitors in parallel instead of one larger capacitor.

Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 4.7μF to 10μF output capacitor with 10V voltage rating is sufficient for most applications. Larger values up to 22μF may be used to obtain extremely low output voltage ripple and improve transient response. An additional phase lead capacitor may be required with output capacitors larger than 10μF to maintain acceptable phase margin. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges.

The ripple current through input capacitor is calculated using Equation 7:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}} \quad (7)$$

The intput capacitor is selected to handle the input ripple noise requirements.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 4.7μF/6.3V input capacitor is sufficient for virtually any application. A 10μF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended. Larger values may be used without limitations. Table 4 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers directly for detailed information on their entire selection of ceramic parts.

Table 4. Capacitor Vendor Information

SUPPLIER	WEBSITE
Murata	www.murata.com
TDK	www.tdk.com

APPLICATION INFORMATION

OUTPUT DIODE

Use a Schottky diode such as an MBR0520, B1020X, B5817WS or equivalent if the converter output voltage is 4.5V or greater. The Schottky diode carries the output current for the time it takes for the synchronous rectifier to turn on. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency. A Schottky diode is optional for output voltages below 4.5V, but will increase converter efficiency by 2% to 3%.

LOAD DISCONNECT IN SHUTDOWN

In conventional synchronous boost converters, a conduction path exists from input to output through the backgate(body diode) of the P-channel MOSFET during shutdown. Special application circuitry can disconnect the load from the battery during shutdown (see Figure 2).

PCB LAYOUT GUIDANCE

As for all switching power supplies, the layout is an important step in the design, especially at high-peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pin of the IC.

The feedback divider should be placed as close as possible to the ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

The high speed operation of the SCJ9311 demands careful attention to board layout. You will not get advertised performance with careless layout. Figure 2 shows the recommended component placement. A large ground pin copper area will help to lower the chip temperature. A multilayer board with a separate ground plane is ideal, but not absolutely necessary.

For the best efficiency and minimum noise problems, the following suggestions should be taken. These items are also illustrated graphically in Figure 2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. A multilayer board with a separate ground plane is ideal, but not absolutely necessary.

2) The power traces, consisting of the GND trace, the switching trace and the V_{IN} trace should be kept short, direct and wide to allow large current flow. Put enough multiply-layer pads when they need to change the trace layer.

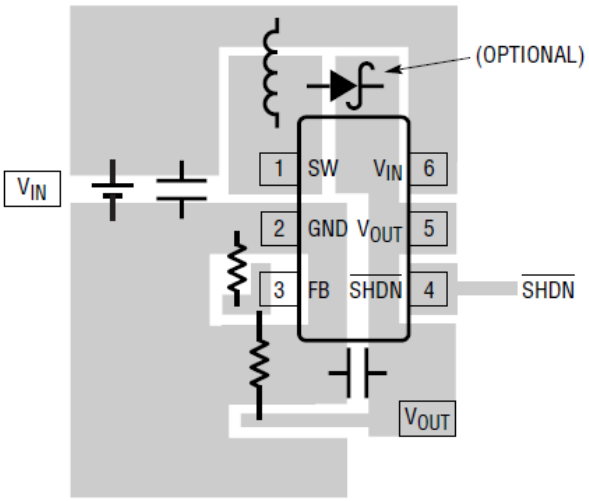
3) Place the (+) plate of C_{IN} near V_{IN} as closely as possible and the loop area formed by C_{IN} and GND must be minimized to maintain input voltage steady and filter out the pulsing input current.

4) The GND of the IC, the (-) plate of C_{IN} and C_{OUT} should be connected as close as possible, together directly to a ground plane.

5) The PCB copper area associated with SW must be minimized to avoid the potential noise problem and reduce EMI.

6) The resistive divider R1 and R2 must be connected to FB pin directly as closely as possible. And FB is a sensitive node. Please keep it away from SW on the PCB layout to avoid the noise problem.

7) If the system chip interfacing with the $\overline{SHDN}$ pin has a high impedance state at shutdown mode and the V_{IN} is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the $\overline{SHDN}$ and GND pins to prevent the noise from falsely turning on the boost regulator at shutdown mode.

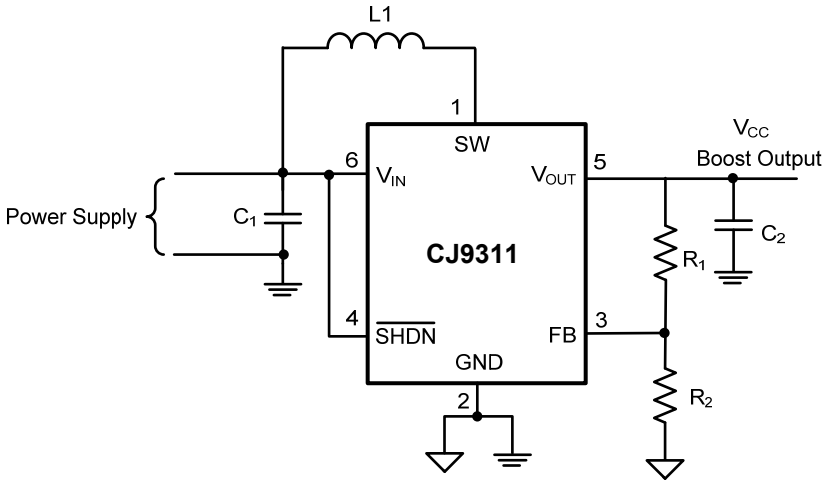


RECOMMENDED COMPONENT PLACEMENT. TRACES CARRYING HIGH CURRENT ARE DIRECT. TRACE AREA AT FB PIN IS SMALL. LEAD LENGTH TO BATTERY IS SHORT.

Figure2. Recommended Component Placement for Single Layer Board

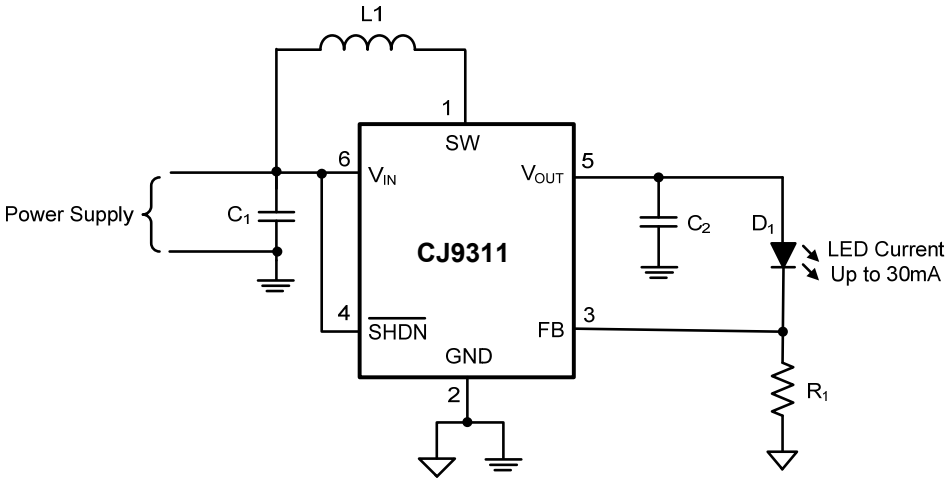
APPLICATION EXAMPLES

The CJ9311 is perfectly suited for LED matrix displays, bar-graph displays, instrument-panel meters, dot matrix displays, set-top boxes, white goods, professional audio equipment, medical equipment, industrial controllers to name a few applications.
Along with Figure 1 on page 7, Figures 3-9 depict a few of the many applications for which the CJ9311 converters are perfectly suited.



List of Components:
U1 = CJ9311T6
L1 = 4.7µH Taiyo Yuden CB2016B4R7M
C1 = 1 x 4.7µF, 0603, X7R/X5R Ceramic
C2 = 2 x 4.7µF, 0603, X7R/X5R Ceramic

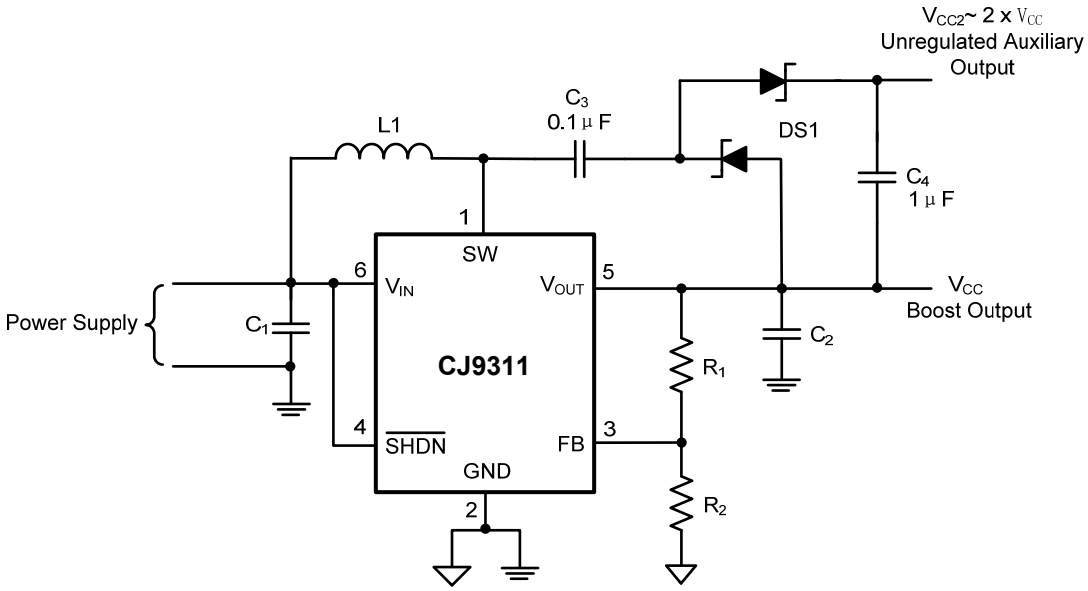
Figure 3. Power Supply Solution Having Small Total Solution Size



List of Components:
U1 = CJ9311T6
L1 = 4.7µH Taiyo Yuden CB2016B4R7M
C1 = 1 x 4.7µF, 0603, X7R/X5R Ceramic
C2 = 2 x 4.7µF, 0603, X7R/X5R Ceramic

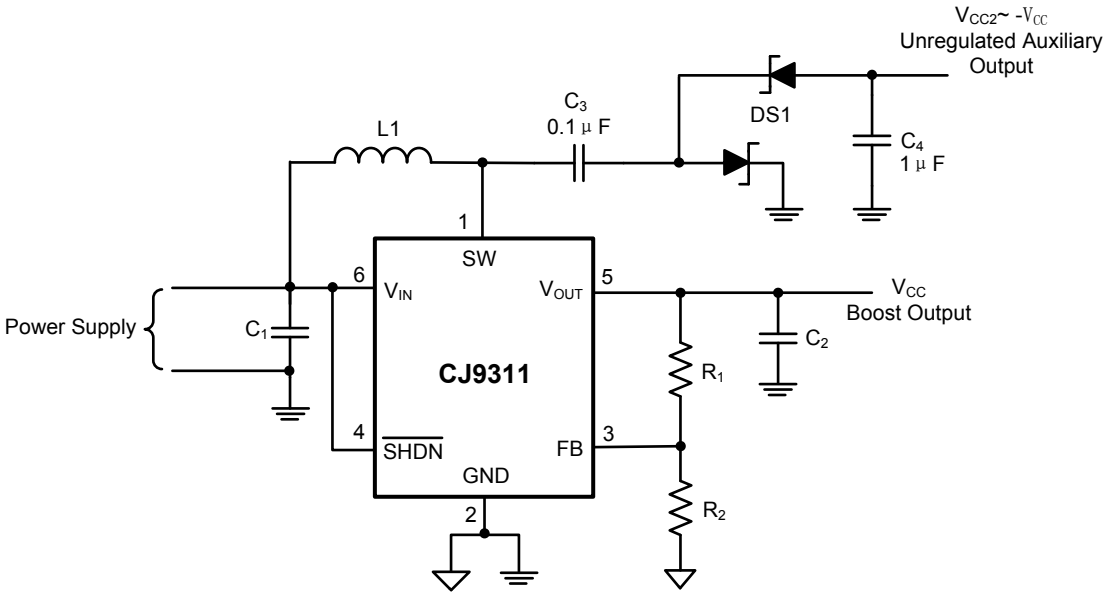
Figure 4. Power Supply Solution for Powering White LEDs in Lighting Applications

APPLICATION INFORMATION



List of Components:
U1 = CJ9311T6
L1 = 4.7µH Wurth Elektronik 744031004
C1 = 2 x 4.7µF, 0603, X7R/X5R Ceramic
C2 = 2 x 4.7µF, 0603, X7R/X5R Ceramic

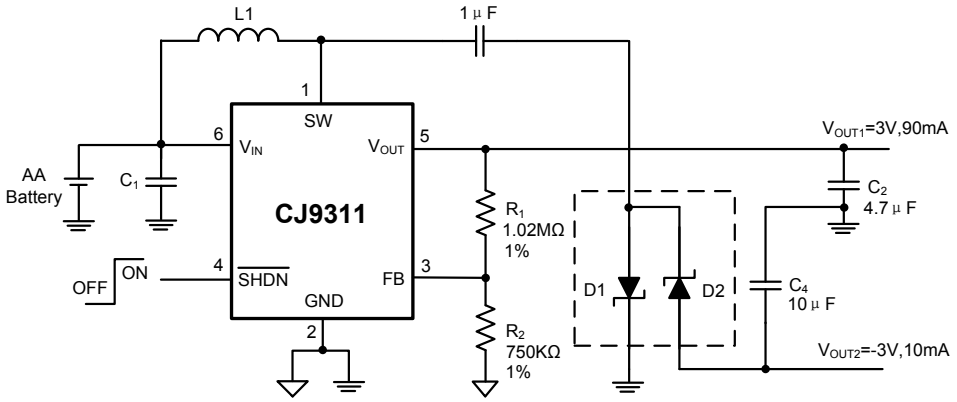
Figure 5. Power Supply Solution With Auxiliary Positive Output Voltage



List of Components:
U1 = CJ9311T6
L1 = 4.7µH Wurth Elektronik 744031004
C1 = 2 x 4.7µF, 0603, X7R/X5R Ceramic
C2 = 2 x 4.7µF, 0603, X7R/X5R Ceramic

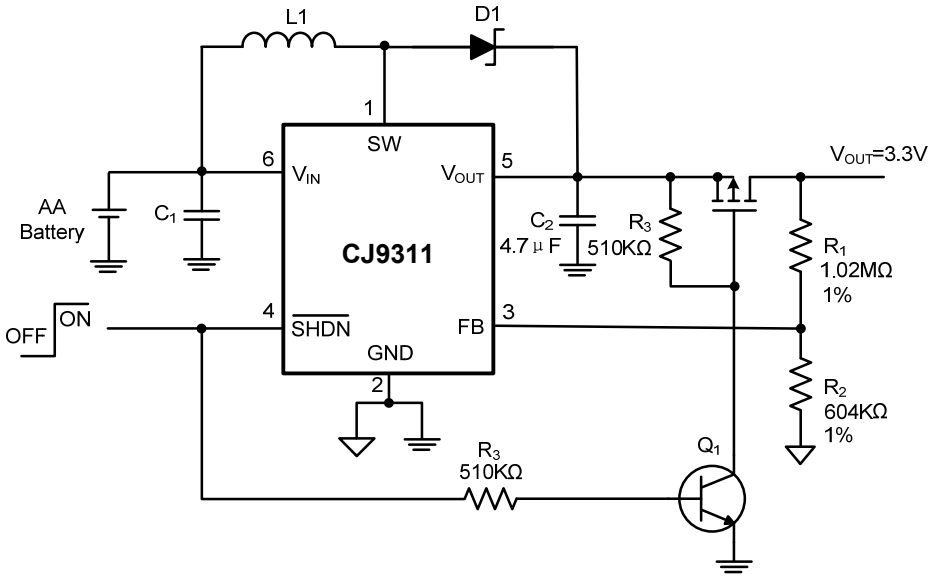
Figure 6. Power Supply Solution With Auxiliary Negative Output Voltage

APPLICATION INFORMATION



List of Components:
U1 = CJ9311T6
L1 = 4.7μH Wurth Elektronik 744031004
C1 = 1 x 4.7μF, 0603, X7R/X5R Ceramic
C2 = 1 x 4.7μF, 0603, X7R/X5R Ceramic

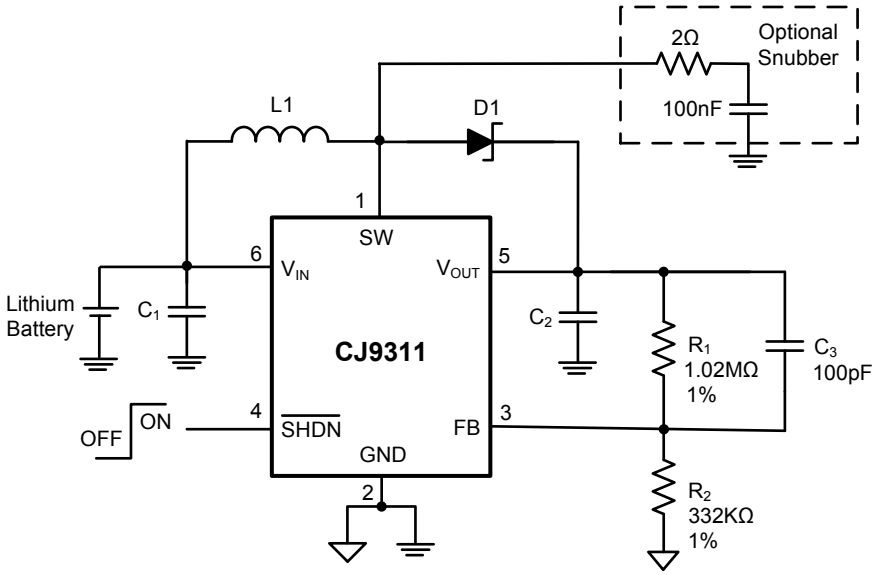
Figure 7. Single AA Cell to ±3V Synchronous Boost Converter



List of Components:
U1 = CJ9311T6
L1 = 4.7μH Wurth Elektronik 744031004
C1 = 1 x 4.7μF, 0603, X7R/X5R Ceramic
C2 = 1 x 4.7μF, 0603, X7R/X5R Ceramic

Figure 8. Single AA Cell to 3.3V Synchronous Boost Converter with Load Disconnect in Shutdown

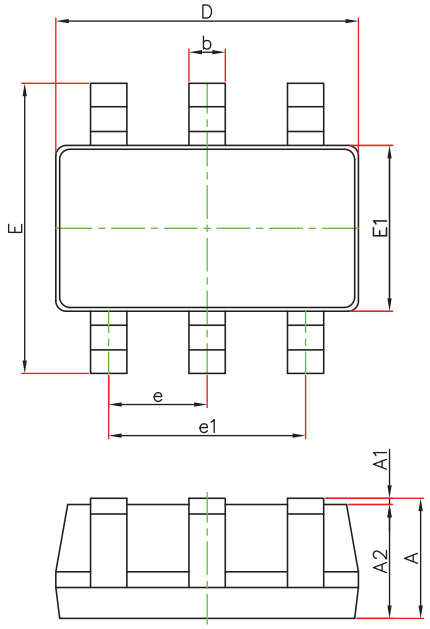
APPLICATION INFORMATION

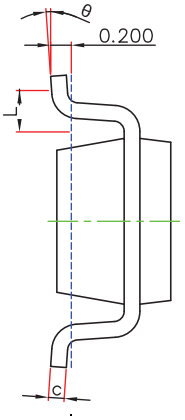


List of Components:
U1 = CJ9311T6
L1 = 4.7μH Wurth Elektronik 744031004
C1 = 1 x 4.7μF, 0603, X7R/X5R Ceramic
C2 = 1 x 4.7μF, 0603, X7R/X5R Ceramic

Figure9. Single Lithium Cell to 5V, 250mA

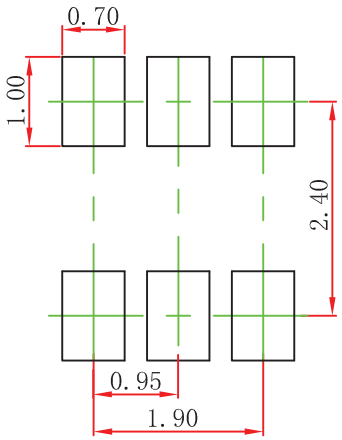
SOT-23-6L Package Outline Dimensions





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-6L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.