A4407

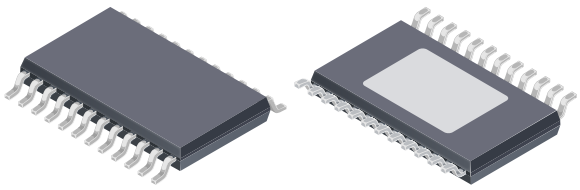
2.2 MHz Constant On-Time Buck Regulator with Two External and Two Internal Linear Regulators

FEATURES AND BENEFITS

- AEC-Q100 Grade 0 qualified
- Internal buck pre-regulator followed by LDO outputs
- 5.5 to 36 V V_{IN} operating range (50 V maximum); for start/stop, cold crank, and load dump requirements
- Constant on-time (COT) buck pre-regulator
- Valley current sensing achieves shortest buck on-times
- 2.2 MHz (V_{IN}-adjusted) switching frequency
- 5 V internal low-dropout tracking linear regulator with foldback short circuit and short-to-battery protections
- 5 V internal low-dropout linear regulator with foldback short circuit protection
- 3.3 V external FET controller/driver with programmable current limit and foldback short circuit protection
- 1.2 V/1.5 V/1.8 V external FET controller/driver with programmable current limit and foldback protection
- Power-on reset (NPOR) with adjustable rising delay
- Logic enable input (ENB) for microprocessor control
- Ignition enable input (ENBAT) for remote startup
- Ignition status indicator (ENBATS) output
- Buck pulse-by-pulse overcurrent protection
- Buck LX short circuit protection (latched)
- Missing asynchronous diode protection (latched)
- UVLO for VIN, charge pump, and the internal rail
- Thermal shutdown protection
- −40°C to 150°C junction temperature range

PACKAGE:

24-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

The A4407 is an automotive power management IC that uses a 2.2 MHz constant on-time (COT) buck pre-regulator to supply a 5 V linear regulator, a 5 V tracking/protected linear regulator, a 3.3 V linear FET controller/driver, and a 1.2 V/1.5 V/1.8 V linear FET controller/driver. The A4407 provides a pin to set the master reference for the 5 V tracking regulator to either the 3.3 V or the 5 V output. The on-time of the buck is internally adjusted as a function of V_{IN} to maintain the 2.2 MHz switching frequency. Efficient operation is achieved by using the buck pre-regulator to drop the input voltage before supplying the linear regulators. Designed to supply CAN and microprocessor power supplies in high temperature environments, the A4407 is ideal for under hood applications.

The switching regulator is designed to operate at a nominal switching frequency of 2.2 MHz. The high switching frequency enables the customer to select low value inductors and ceramic capacitors while avoiding EMI in the AM frequency band.

Protection features include: undervoltage lockout, pulse-by-pulse current limit, LX short circuit protection, and thermal shutdown. In case of a shorted load all linear regulators feature foldback overcurrent protection. In addition, the V5P output is protected from a short-to-battery event. The A4407 features both a logic level and a high-voltage (current and voltage limited) enable input. The A4407 also features a power-on-reset (NPOR) output with adjustable delay for microprocessor control.

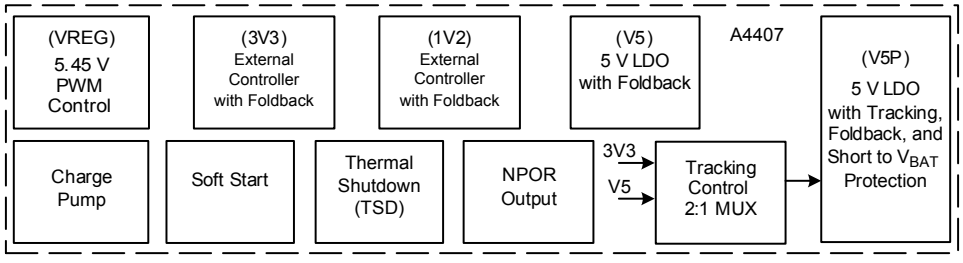
The A4407 is supplied in a low profile (1.1 mm) 24-lead TSSOP package with exposed pad for enhanced thermal dissipation (suffix LP). The package is lead (Pb) free with 100% matte-tin leadframe plating.

APPLICATIONS:

Automotive Control Modules, such as:

- Electronic power steering (EPS)
- Transmission control (TCU)
- Antilock braking (ABS)
- Emissions control

Simplified Functional Block Diagram



Selection Guide

Part Number	Operating Ambient Temperature Range T_A, (°C)	Package	Packing*	Leadframe Plating
A4407KLPTR-T	–40 to 135	24-pin TSSOP with exposed thermal pad	4000 pieces per 13-in. reel	100% matte tin

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Unit
VIN Pin			−0.3 to 50	V
LX Pin	V_{LX}		–0.3 to 50	V
		t < 250 ns	–1.5	V
VCP, CP1, CP2 Pins			−0.3 to 60	V
ISEN– Pin			−0.5 to 1	V
ISEN+ Pin			−0.5 to 0.5	V
ENBAT Pin		The ENBAT pin is internally clamped to approximately 8.5 V due to an ESD protection device.	−0.3	V
			−50 to 50	mA
VREG Pin			−0.3 to 8	V
G1V2 and G3V3 Pins		These pins are internally clamped by an ESD protection device. Clamp voltages range from 10 V (min) to 15 V (max).	−0.3	V
CL1V2 and CL3V3 Pins			−0.3 to 10	V
V5P Pin			–0.3 to V_{IN}+0.5	V
V5 Pin			−0.3 to 7	V
TON Pin			−0.3 to 50	V
NPOR, CPOR, ENB, ENBATS, TRACK, 1V2, and 3V3 Pins			−0.3 to 7	V
Operating Ambient Temperature	T_A	Range K	−40 to 135	°C
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

*Absolute Maximum Ratings are limiting values that should not be exceeded under worst case operating conditions or damage may occur. Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute-Maximum–rated conditions for extended periods may affect device reliability.

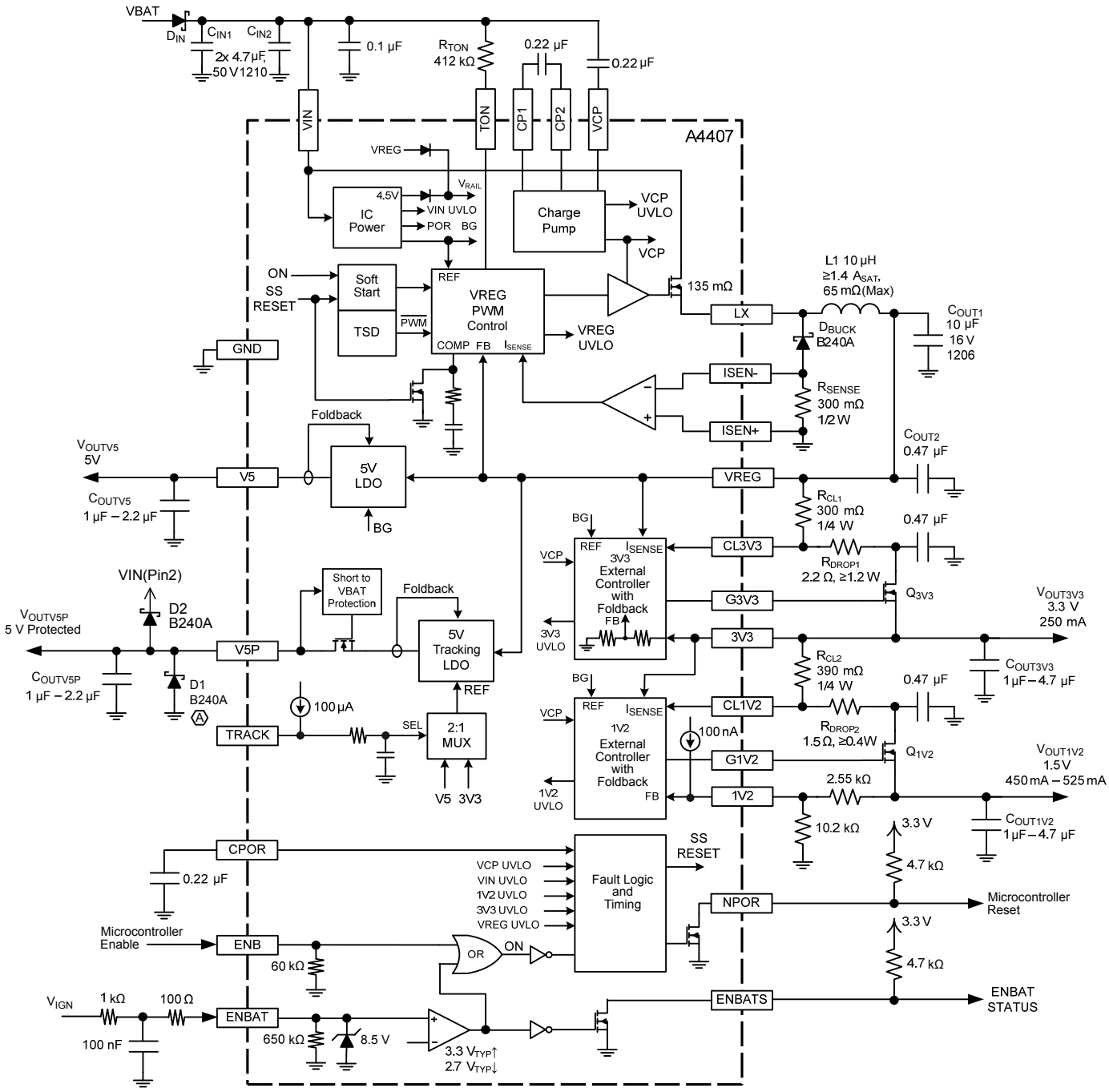
Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	28	°C/W

*Additional thermal information available on the Allegro™ website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

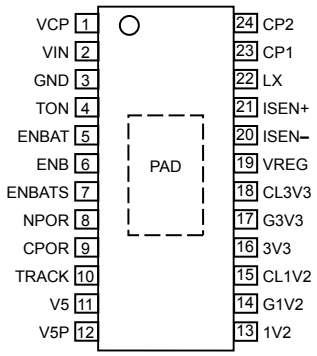
Functional Block Diagram



Ⓐ Protection diodes D1 and D2 are required when the V5P pin is driving a wiring harness (or excessively long PCB trace) where parasitic inductance will cause the voltage at the V5P to momentarily transition above VIN or below ground during a fault condition.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCP	Charge pump reservoir capacitor
2	VIN	Input voltage
3	GND	Ground
4	TON	Buck regulator on-time programming pin
5	ENBAT	Ignition enable input from the key/switch via a 1 kΩ resistor
6	ENB	Logic enable input from the microcontroller
7	ENBATS	Open drain ignition status output
8	NPOR	Open-drain fault indication output; active low
9	CPOR	NPOR delay programming pin
10	TRACK	Sets the V5P tracking to either the 3V3 or V5 linear regulator
11	V5	5 V regulator output
12	V5P	5 V tracking/protected regulator output
13	1V2	1.2 V/1.5 V/1.8 V regulator output
14	G1V2	Gate driver to the external MOSFET for 1.2 V/1.5 V/1.8 V regulation
15	CL1V2	1.2 V/1.5 V/1.8 V current sense/limit input
16	3V3	3.3 V regulator output
17	G3V3	Gate driver to the external MOSFET for 3.3 V regulation
18	CL3V3	3.3 V current sense/limit input
19	VREG	Buck regulator DC output and input to the 3.3 V external regulator
20	ISEN–	Buck negative current sense pin, sense resistor and diode node
21	ISEN+	Buck positive current sense pin, sense resistor/ground node
22	LX	Buck regulator switching node
23	CP1	Charge pump capacitor connection
24	CP2	Charge pump capacitor connection
–	PAD	Exposed thermal pad for enhanced heat dissipation

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS Valid at 5.5 V < V_{IN} < 36 V, −40°C < T_J < 150°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
General Specifications						
Functional Input Voltage	$V_{IN(FUNC)}$	A4407 functional, parameters not guaranteed	5.5	–	46	V
Operating Input Voltage	$V_{IN(OP)}$		5.5	13.5	36	V
Supply Quiescent Current[1]	I_Q	V_{IN} = 13.5 V, V_{IGN} > $V_{IGN(H)}$ or V_{ENB} > $V_{ENB(H)}$, no load on VREG	–	10	–	mA
	$I_{Q(SLEEP)}$	V_{IN} = 13.5 V, V_{IGN} < $V_{IGN(L)}$ and V_{ENB} < $V_{ENB(L)}$, no load on VREG	–	–	10	µA
Buck Switching Regulator (VREG)						
Switcher Output – Regulating	$V_{REG(PWM)}$	$V_{IN(SWNOM)}$ < V_{IN} < 27 V, V_{ENB} = high, 100 mA < I_{VREG} < 1100 mA	5.30	5.45	5.60	V
Switcher Output – Dropout	$V_{REG(100\%)}$	V_{IN} = 5.5 V, LX at 100% duty cycle, I_{VREG} = 1100 mA	5.03	–	–	V
		V_{IN} = 6.4 V and LX at 100% duty cycle, I_{VREG} = 200 mA	–	–	6.38	V
Switcher Period[2]	$T_{SW(L)}$	$V_{IN(SWL)}$ < V_{IN} < $V_{IN(SWNOM)}$, R_{TON} = 412 kΩ	–	1.6	–	µs
	$T_{SW(NOM)}$	$V_{IN(SWNOM)}$ < V_{IN} < $V_{IN(SWH)}$, R_{TON} = 412 kΩ	–	450	–	ns
	$T_{SW(H)}$	$V_{IN(SWH)}$ < V_{IN} < 36 V, R_{TON} = 412 kΩ	–	1.6	–	µs
Switcher On-Time	t_{ON}	V_{IN} = 7.5 V, R_{TON} = 412 kΩ	1030	1290	1550	ns
		V_{IN} = 13.5 V, R_{TON} = 412 kΩ	160	200	240	ns
		V_{IN} = 27 V, R_{TON} = 412 kΩ	80	118	135	ns
		V_{IN} = 35 V, R_{TON} = 412 kΩ	225	280	335	ns
Switcher Period Threshold	$V_{IN(SWL)}$	V_{IN} falling, T_{SW} changes from $T_{SW(L)}$ to 100% duty cycle	6.2	6.5	6.8	V
	$V_{IN(SWNOM)}$	V_{IN} falling, T_{SW} changes from $T_{SW(NOM)}$ to $T_{SW(L)}$	8.0	8.6	9.2	V
	$V_{IN(SWH)}$	V_{IN} rising, T_{SW} changes from $T_{SW(NOM)}$ to $T_{SW(H)}$	28	31	34	V
Switcher Period Hysteresis	$V_{IN(SWL)hys}$	Relative to the VIN voltage that initially caused the switcher period to change	–	250	–	mV
	$V_{IN(SWNOM)hys}$	Relative to the VIN voltage that initially caused the switcher period to change	–	250	–	mV
	$V_{IN(SWH)hys}$	Relative to the VIN voltage that initially caused the switcher period to change	–	700	–	mV
Switch On-Resistance	$R_{DS(on)}$	T_J = 25°C, I_{DS} = 0.1 A	–	135	180	mΩ
		T_J = 150°C, I_{DS} = 0.1 A	–	270	360	mΩ
Minimum On-Time	$t_{ON(min)}$	V_{IN} = 13.5 V, R_{TON} = 49.9 kΩ	–	65	90	ns
Minimum Off-Time	$t_{OFF(min)}$	V_{IN} = 13.5 V	85	110	140	ns

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued) Valid at 5.5 V < V_{IN} < 36 V, −40°C < T_J < 150°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Buck Switching Regulator (VREG) (continued)						
Current Feedback Gain[2]	G_{ISEN}		–	4.0	–	V/V
Error Amplifier Transconductance[2]	g_m		–	7.5	–	µA/V
Error Amplifier Open Loop Gain[2]	AV_{OL}		–	57	–	dB
0 dB Crossover Frequency[2]	f_C	V_{IN} = 13.5 V, R_{SENSE} = 300 mΩ, C_O = 10 µF, R_L = 5.5 Ω	–	65	–	kHz
Soft Start Ramp Time	t_{SS}		–	10	–	ms
5 V and 5VP Linear Regulators						
V5 Accuracy and Load Regulation	err_{V5}	10 mA < I_{V5} < 215 mA, V_{REG} ≥ 5.25 V	4.9	5.0	5.1	V
V5P Accuracy and Load Regulation	err_{V5P}	10 mA < I_{V5P} < 280 mA, V_{REG} ≥ 5.25 V	4.9	5.0	5.1	V
V5P/3V3 Tracking Ratio		V_{V5P} / V_{3V3}	1.507	1.515	1.523	–
V5P/3V3 Tracking Accuracy	$err_{Track3V3}$	2.69 V < V_{3V3} < 3.37 V, I_{V5P} = 75 mA, 5.5 V < V_{IN} < 27 V	−0.5	–	+0.5	%
V5P/V5 Tracking Accuracy[3]	$err_{TrackV5}$	I_{V5P} = I_{V5} = 75 mA, 5.5 V < V_{IN} < 27 V, –20°C < T_J < 150°C	−25	–	+25	mV
		I_{V5P} = I_{V5} = 75 mA, 5.5 V < V_{IN} < 27 V, T_J = –40°C	−32	–	+32	mV
3.3 V Linear Regulator and FET Driver						
3V3 Accuracy	err_{3V3}	10 mA < I_{3V3} < 700 mA	3.23	3.30	3.37	V
3V3 Input Resistance	R_{IN3V3}		–	300	–	kΩ
G3V3 Source Current[1]	$I_{G3V3(SRC)}$	V_{3V3} = 3.0 V, V_{G3V3} = $V_{G3V3(MAX)}$ – 1 V	−160	−320	–480	µA
G3V3 Sink Current[1]	$I_{G3V3(SINK)}$	V_{3V3} = 3.6 V, V_{G3V3} = 6 V	0.5	4	–	mA
G3V3 Maximum Voltage	$V_{G3V3(MAX)}$	V_{3V3} = 3.0 V	9	–	15	V
G3V3 Minimum Voltage	$V_{G3V3(MIN)}$	V_{3V3} = 3.6 V	–	0.7	1.0	V
G3V3 Output Impedance[2]	$R_{OUT(G3V3)}$		–	175	–	Ω
3V3 External FET Gate Capacitance[2]	C_{ISS3V3}		250	–	5200	pF
1.2 V/1.5 V/1.8 V Linear Regulator and FET Driver						
1V2 Accuracy	err_{1V2}	10 mA < I_{1V2} < 500 mA	1.174	1.205	1.236	V
1V2 Bias Current[1]	I_{1V2}		–	−100	–	nA
G1V2 Source Current[1]	$I_{G1V2(SRC)}$	V_{1V2} = 0.9 V, V_{G1V2} = $V_{G1V2(MAX)}$ – 1V	−120	−240	–360	µA
G1V2 Sink Current[1]	$I_{G1V2(SINK)}$	V_{1V2} = 1.5 V, V_{G1V2} = 6 V	0.5	3	–	mA
G1V2 Maximum Voltage	$V_{G1V2(MAX)}$	V_{1V2} = 0.9 V	9	–	15	V
G1V2 Minimum Voltage	$V_{G1V2(MIN)}$	V_{1V2} = 1.5 V	–	0.7	1.0	V
G1V2 Output Impedance[2]	$R_{OUT(G1V2)}$		–	175	–	Ω
1V2 External FET Gate Capacitance[2]	C_{ISS1V2}		250	–	3900	pF
Charge Pump (VCP)						
VCP Output Voltage	ΔV_{CP}	V_{CP} − V_{IN}	4.1	6.6	–	V
VCP Switching Frequency	$f_{SW(CP)}$		–	100	–	kHz

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued) Valid at 5.5 V < V_{IN} < 36 V, −40°C < T_J < 150°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Logic Enable Input (ENB)						
ENB Logic Input Threshold	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Logic Input Current[1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	100	µA
ENB Pulldown Resistance	R_{ENB}		–	60	–	kΩ
Ignition Enable Input (ENBAT) and Ignition Status Output (ENBATS)						
ENBAT and ENBATS Thresholds	$V_{IGN(H)}$	V_{IGN} rising via a 1 kΩ series resistance, measure V_{IGN} when IQ occurs	–	3.3	4.0	V
	$V_{IGN(L)}$	V_{IGN} falling via a 1 kΩ series resistance, measure V_{IGN} when $I_{Q(SLEEP)}$ occurs	2.2	2.7	–	V
ENBAT Input Current[1]	$I_{ENBAT(IN)}$	V_{IGN} = 5.5 V via a 1 kΩ series resistance	–	50	100	µA
		V_{IGN} = 0.8 V via a 1 kΩ series resistance	0.5	–	5	µA
ENBAT Input Resistance	R_{ENBAT}		–	650	–	kΩ
ENBATS Output Voltage	$V_{ENBATS(L)}$	I_{ENBATS} = 4 mA	–	–	400	mV
ENBATS Leakage Current[1]	$I_{ENBATS(LKG)}$	V_{ENBATS} = 3.3 V	–	–	1	µA
ENBATS Turn-On Delay	t_{ENBATS}	Sleep mode to V_{ENBATS} = 3.3 V	–	11	–	ms
TRACK Input						
TRACK Voltage Threshold	$V_{TRACK(H)}$	V_{TRACK} rising	–	–	2.0	V
	$V_{TRACK(L)}$	V_{TRACK} falling	0.8	–	–	V
TRACK Bias Current[1]	$I_{TRACK(BIAS)}$		–	−100	–	µA
NPOR Output						
NPOR Power-Up Delay	t_{NPOR}	C_{POR} = 0.22 µF	–	20	–	ms
NPOR Output Voltage	$V_{NPOR(L)}$	V_{ENB} = high or V_{ENBAT} = high, V_{REG} < $V_{REGUV(L)}$ or V_{3V3} < $V_{3V3UV(L)}$, I_{NPOR} ≤ 4mA	–	–	400	mV
		V_{ENBAT} = low, V_{ENB} transitioning low, V_{REG} = 5.45 V, I_{NPOR} ≤ 0.3 mA, 0.8 V < V_{3V3} < err_{3V3}, 0°C ≤ T_J ≤ 150°C	–	350	800	mV
		V_{ENBAT} = low, V_{ENB} transitioning low, V_{REG} = 5.45 V, I_{NPOR} ≤ 0.3 mA, 1.0 V < V_{3V3} < err_{3V3}, −40°C ≤ T_J ≤ 150°C	–	–	800	mV
NPOR Leakage Current[1]	$I_{NPOR(LEAK)}$	V_{NPOR} = 3.3 V	–	–	1	µA
CPOR Characteristics						
CPOR Charge Current[1]	$I_{CPOR(SRC)}$		–	−13	–	µA
CPOR Voltage Threshold	$V_{CPOR(H)}$	V_{CPOR} rising	1.0	1.2	1.4	V

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued) Valid at 5.5 V < V_{IN} < 36 V, −40°C < T_J < 150°C; unless otherwise specified

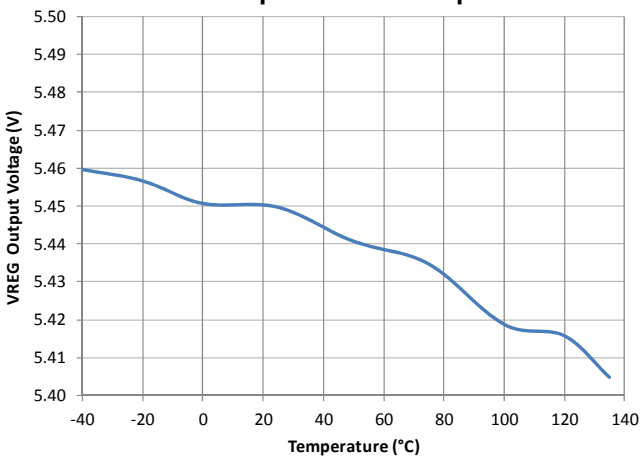
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR Thresholds						
VREG UVLO Thresholds	$V_{REGUV(H)}$	V_{REG} rising, NPOR transitions high	4.80	5.00	5.20	V
	$V_{REGUV(L)}$	V_{REG} falling, NPOR transitions low	4.75	4.94	5.14	V
VREG UVLO Hysteresis	$V_{REGUVHYS}$		–	60	–	mV
3V3 UVLO Thresholds	$V_{3V3UV(H)}$	V_{3V3} rising, NPOR transitions high	2.80	2.95	3.10	V
	$V_{3V3UV(L)}$	V_{3V3} falling, NPOR transitions low	–	2.83	–	V
3V3 UVLO Hysteresis	$V_{3V3UVHYS}$		–	125	–	mV
1V2 UVLO Thresholds	$V_{1V2UV(H)}$	Measured as percentage of err_{1V2}; V_{1V2} rising, NPOR transitions high	85	89	93	%
	$V_{1V2UV(L)}$	Measured as percentage of err_{1V2}; V_{1V2} falling, NPOR transitions low	–	84	–	%
1V2 UVLO Hysteresis	$V_{1V2UVHYS}$		–	5	–	%
Buck (VREG) Current Protection						
VREG ISEN Voltage Threshold	$V_{ISEN(th)}$	$V_{ISEN+} - V_{ISEN-}$	265	350	435	mV
VREG Valley Current Limit	$I_{LIM(VALLEY)}$	R_{SENSE} = 300 mΩ, $V_{IN} > V_{INSW(L)}$	883	1167	1450	mA
VREG Peak Current Limit	$I_{LIM(PEAK)}$		3.0	5.5	–	A
3.3 V Overcurrent Protection						
3V3 Overcurrent Threshold	V_{CL3V3}	$V_{REG} - V_{CL3V3}$	210	235	280	mV
3V3 Current Limit	I_{3V3LIM}	R_{CL3V3} = 300 mΩ	700	783	–	mA
3V3 Foldback Threshold	I_{3V3FB}	V_{3V3} = 0 V, $V_{REG} - V_{CL3V3}$	48	65	90	mV
1.2 V/1.5 V/1.8 V Overcurrent Protection						
1V2 Overcurrent Threshold	V_{CL1V2}	V_{1V2} = 1.2 V, $V_{3V3} - V_{CL1V2}$	179	218	245	mV
1V2 Current Limit	I_{1V2LIM}	R_{CL1V2} = 390 mΩ	459	559	–	mA
1V2 Foldback Threshold	I_{1V2FB}	V_{1V2} = 0 V, $V_{3V3} - V_{CL1V2}$	45	60	84	mV
5VP Overcurrent Protection						
V5P Current Limit[1]	I_{V5PLIM}	V_{V5P} = 5 V	−280	−415	–	mA
V5P Foldback Current[1]	I_{V5PFB}	V_{V5P} = 0 V	−70	−110	−150	mA
5V Overcurrent Protection						
V5 Current Limit[1]	I_{V5LIM}	V_{V5} = 5 V	−215	−310	–	mA
V5 Foldback Current[1]	I_{V5FB}	V_{V5} = 0 V	−74	−92	−135	mA
Thermal Protection						
Thermal Shutdown Threshold	T_{JTSD}	T_J rising	155	170	–	°C
Thermal Shutdown Hysteresis	$T_{JTSDHYS}$		–	20	–	°C

[1]For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2]Ensured by design and characterization, not production tested.
[3]–20°C ensured by design and characterization, not production tested.

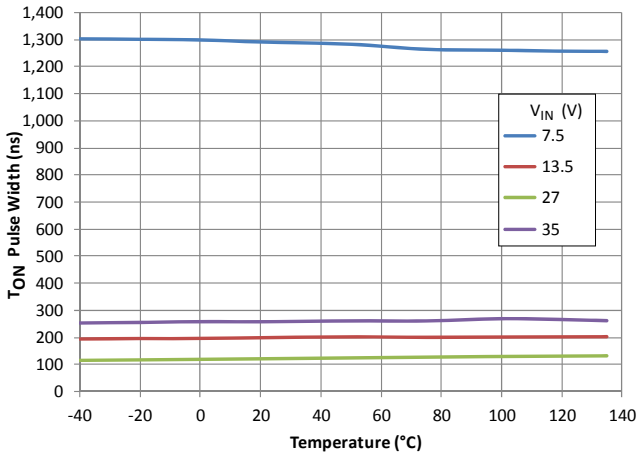
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Characteristic Performance

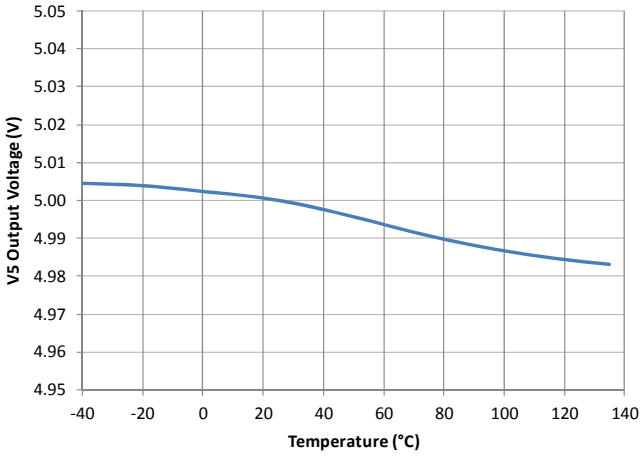
VREG Output versus Temperature



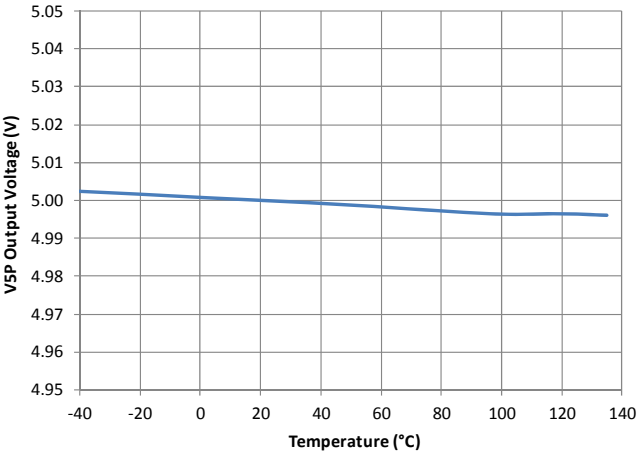
T_{ON} versus Temperature



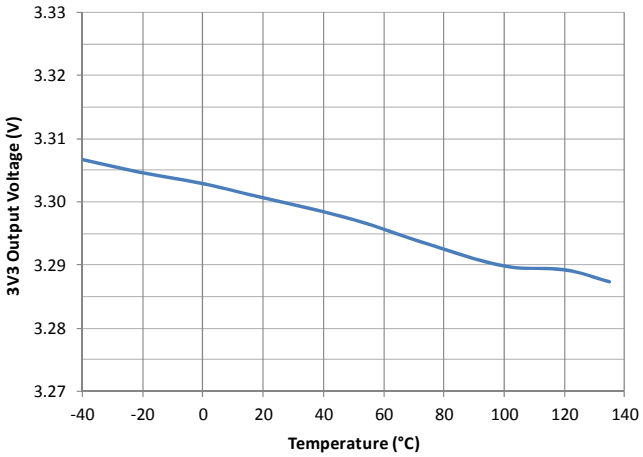
V5 Output versus Temperature



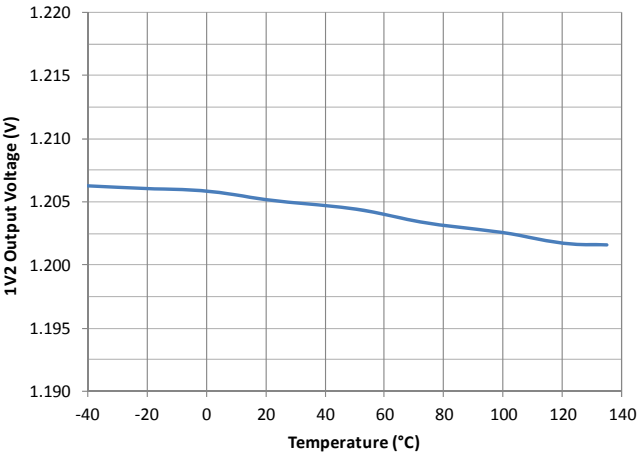
V5P Output versus Temperature



3V3 Output versus Temperature

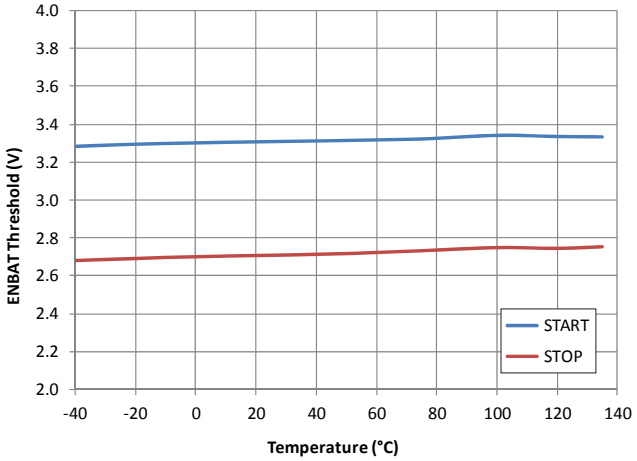


1V2 Output versus Temperature

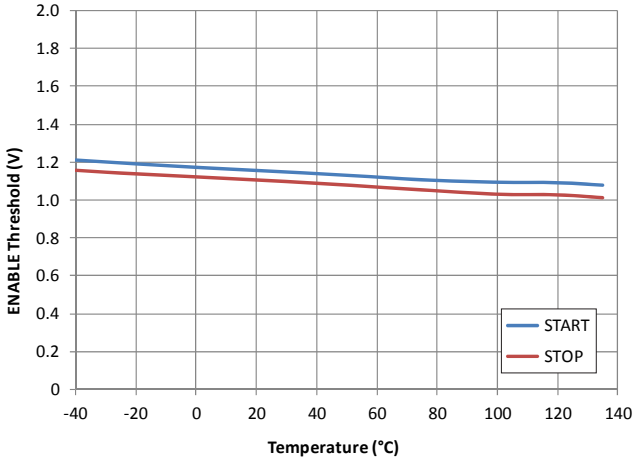


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

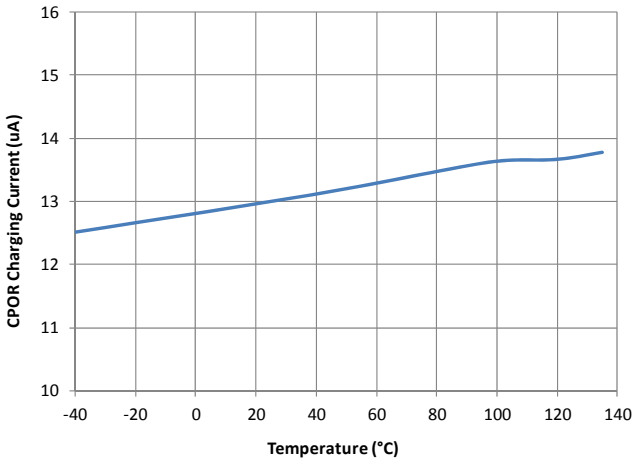
ENBAT Start / Stop Thresholds versus Temperature



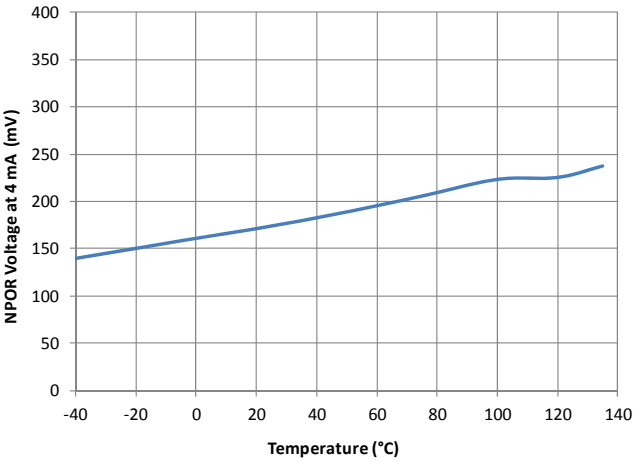
ENABLE Start / Stop Thresholds versus Temperature



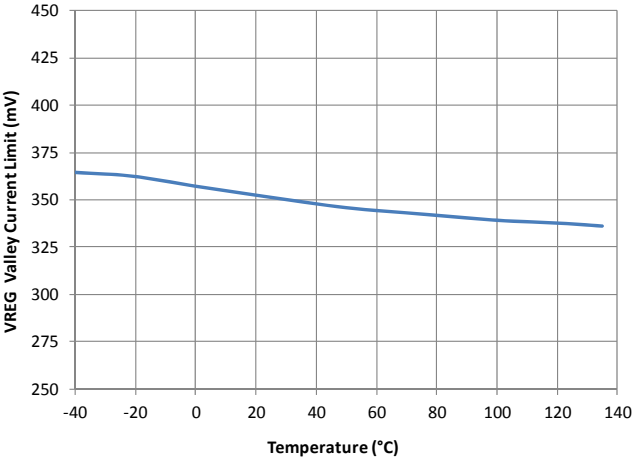
CPOR Charging Current versus Temperature



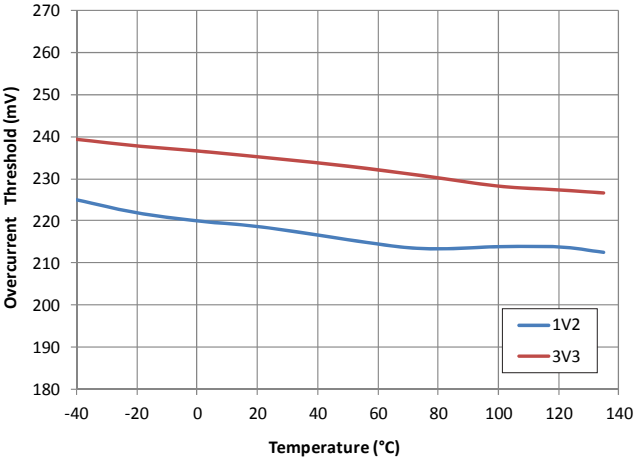
ENBATS (Low) Voltage versus Temperature



VREG Valley Current Limit versus Temperature



1V2 and 3V3 Overcurrent Threshold versus Temperature



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Functional Description

Overview

The A4407 contains a constant on-time (COT), buck switching pre-regulator with valley sensing current mode control, two integrated 5 V linear regulators, and two N-channel FET drivers: one for a 1.2 V, 1.5 V, or 1.8 V linear regulator, and the other for a 3.3 V linear regulator. The COT converter maintains a constant output frequency because the on-time is inversely proportional to the supply voltage. As the input voltage decreases, the on-time is increased, which maintains a relatively constant period and frequency. Valley mode current control allows the converter to achieve very short on-times because current is measured during the off-time, so there is no requirement for blanking.

With very low input voltages, the buck switch transitions to a 100% duty cycle. This turns the buck switch on 100% of the time (no switching), and allows the regulator to operate in dropout mode.

The device is enabled via the logic level input (ENB) or the high voltage ignition input (ENBAT). When the device is enabled, the converter starts up under the control of a 10 ms internal soft start ramp. The two enable inputs are logically ORed together, so either of the inputs can be used to enable the device. Both inputs must be low to disable the device.

Under light load conditions, the switch enters pulse-skipping mode to ensure regulation is maintained. In order to accept a wide input voltage range, the switcher period is extended when either the minimum on- or off-time is reached, or when the input supply is at either end of its range.

The A4407 features overcurrent protection on all regulators including the VREG pre-regulator. The buck switch current limit is determined by the selection of the sense resistor between the ISENx pins. Output current from the internal 5 V and 5 V protected linear regulators is also monitored, and if shorted the outputs would fold back. The external FET drivers have current limit sensing that can be used with a sense resistor to trigger fold back protection.

Buck Dropout Mode

The topology of a COT timer is ideal for systems that have high input voltages. Because current is measured during the off-time, very short on-times can be achieved. With low input voltages, the switcher must maintain very short off-times. To prevent the switcher from reaching its minimum off-time, the switcher is designed to enter a 100% duty cycle mode. This causes the switcher to stop acting as a buck switch. The voltage at the VREG pin then becomes simply the supply voltage minus the drop across the buck switch and inductor. In this mode, maximum available current may be lower, depending on ambient temperature and supply voltage while in dropout mode.

Soft Start

An internal ramp generator and counter allow the output voltages to ramp up. This limits the maximum demand on the external power supply by controlling the inrush current required to charge the external capacitor and any DC load at startup. Internally, the ramp is set to 10 ms typical. The following conditions are required to trigger a soft start:

- ENBAT or ENB transition high, and
- There is no thermal shutdown (TSD = 0), and
- 3V3 voltage is below its undervoltage lockout (UV) threshold, and
- 1V2 voltage is below its UV threshold, and
- VREG voltage is below its UV threshold

Buck Pulse Width (TON)

A resistor from the TON input to VIN sets the on-time of the converter for a given input voltage. When the supply voltage is between 8.6 and 31 V, the switcher period remains constant, based on the selected value of R_{TON}. At voltages lower than 6.5 V, the switch is in dropout mode (100% duty cycle). Within reasonable input voltage ranges, the period of the converter is held constant. This results in a constant operating frequency across the input supply range. More information on how to choose R_{TON} can be found in the Application Information section. The formula to calculate the on-time resistor value is:

$$t_{on} = (R_{TON} / V_{IN}) \times 6.36 \times 10^{-12} + 5 \times 10^{-9} \quad \text{(ns)} \qquad (1)$$

Buck Current Sense (ISEN+, ISEN–)

The sense inputs are used to sense the current in the buck regulator free-wheeling diode during the off-time. The value of the

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

sense resistor, R_{SENSE}, between the ISENx pins, can be calculated from:

$$R_{SENSE} = V_{ISEN} / I_{LIM(VALLEY)} \quad (2)$$

where V_{ISEN} is documented in the Electrical Characteristics table, 350 mV typical, and $I_{LIM(VALLEY)}$ is the lowest current measured during the off-time.

It is recommended that the current sense resistor be sized so that, at peak output current, the voltage at the ISEN– pin does not exceed –0.75 V during PWM operation (that is, a transient condition). Because the diode current is measured when the inductor current is at the valley, the average output current is greater than the $I_{LIM(VALLEY)}$ value. The value for $I_{LIM(VALLEY)}$ should be:

$$I_{LIM(VALLEY)} = I_{OUT(avg)} - 0.5 \times I_{RIPPLE} + K \quad (3)$$

where $I_{OUT(avg)}$ is the average of all the regulator outputs currents, I_{RIPPLE} is the inductor ripple current, and K is a design margin allowing for component tolerances.

The peak current in the switch is simply:

$$I_{PEAK} = I_{LIM(VALLEY)} + I_{RIPPLE} \quad (4)$$

Information on how to calculate the ripple current is included in the Application Information section.

Buck Overcurrent Protection

The converter utilizes pulse-by-pulse valley current limiting, which is activated when the current through the sense resistor (that is, the buck output current) is high enough to create –350 mV at the ISEN– pin. During an overload condition, the switch is turned on for a period determined by the constant on-time circuitry. The switch off-time is extended until the current decays to the current limit value set by the selection of the sense resistor, at which point the switch is allowed to turn-on again. Because no slope compensation is required in this control scheme, the current limit is maintained at a reasonably constant level across the input voltage range.

Figure 1 illustrates how the current is limited during an overload condition. The current decay (period with switch off) is proportional to the output voltage. As the overload is increased, the output voltage tends to decrease and the switching period increases.

LX Short Circuit Protection

If the LX node is shorted to ground, there would be a relatively high peak current in the buck MOSFET within a very short time. The A4407 protects itself by detecting the unusually high current, turning off the buck MOSFET, and latching itself off. To avoid false tripping, the current required to activate the peak current protection, $I_{LIM(PEAK)}$, 5.5 A typical, is set well above the normal range of currents. After peak current limiting is activated, the A4407 will be latched off until either: V_{IN} is cycled below its UVLO threshold, or the A4407 is disabled (both ENBAT and ENB must be brought low) and re-enabled. NPOR is not directly activated (pulled low) by the peak current protection circuitry. However, NPOR will be in the correct state depending on the VREG, 3V3, and 1V2 outputs.

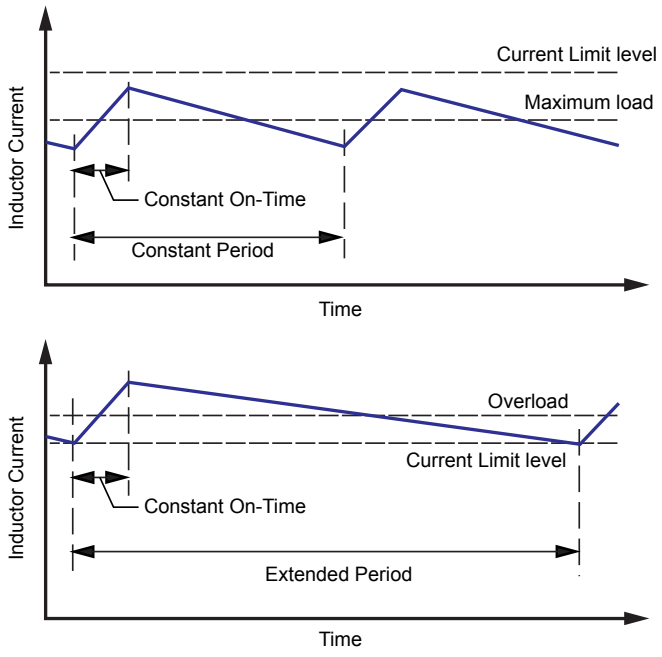


Figure 1. Buck current limiting during overload conditions: (upper) with inductor current operating at maximum load, and (lower) inductor current operating in a “soft” overload.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Missing Asynchronous Diode Protection

In most high voltage asynchronous buck regulators, if the asynchronous diode is missing or damaged the LX pin will transition to a very high negative voltage when the upper MOSFET turns off, resulting in damage to the regulator. The A4407 includes protection circuitry to detect when the asynchronous diode is missing or damaged. If the LX pin becomes more negative than 1.6 V at 25°C for more than 157 ns, the A4407 will latch itself in the off state to prevent damage. After a missing diode fault occurs, the latch must be reset by either cycling VIN or ENBAT or ENB. See figure 2 for the missing diode voltage threshold and time filtering versus temperature.

Thermal Shutdown

If the A4407 junction temperature becomes too high, a thermal shutdown circuit would disable the VREG output, thus protecting the A4407 from damage. When a thermal shutdown occurs, the buck regulator stops switching and the VREG voltage decays. When VREG crosses UVLO threshold for it, the NPOR signal is pulled low. Thermal shutdown is not a latched condition, so when the junction temperature cools to an acceptable level, the A4407 automatically restarts.

Power On Reset (NPOR)

The NPOR output is an open drain pin that can be used to signal a reset event to a DSP or microcontroller. The NPOR block actively monitors ENBAT, ENB, 3V3, 1V2, VCP, and VREG. During power-up, NPOR is held low for a programmable amount of time (t_{NPOR}) after VREG, 3V3, and 1V2 all transition above the upper UVLO threshold for each. The rising edge delay allows time for the regulators to be within specification when the DSP or microcontroller begins processing. The amount of the rising edge delay is determined by the value of the external capacitor from the CPOR pin to ground. The rising delay can be calculated from the following equation:

$$t_{NPOR} = 92.3 \times 10^3 \times C_{POR} \quad \text{(seconds)} \qquad (5)$$

Any of the following conditions forces NPOR to transition low immediately (within a few microseconds):

- 3V3 voltage falls below its UVLO threshold, or
- 1V2 voltage falls below its UVLO threshold, or
- VREG voltage falls below its UVLO threshold, or
- ENBAT and ENB are both low, or
- Charge pump voltage, V_{CP}, is too low, or
- Internal IC power rail voltage, V_{RAIL}, is too low

When a thermal shutdown (TSD) occurs: PWM switching terminates; VREG, or 3V3, or 1V2 decay below the UVLO threshold for it; and NPOR transitions low. Thus, a TSD event indirectly causes NPOR to transition low.

When the A4407 is disabled (ENB and ENBAT are both low or V_{IN} is removed) the NPOR output is held low until the voltage from the 3.3V regulator (3V3) falls below 1.0 V (see figure 3). This assumes maximum initial current (4 mA) in the NPOR open drain DMOS. The NPOR voltages would be somewhat lower for lower values of I_{NPOR}.

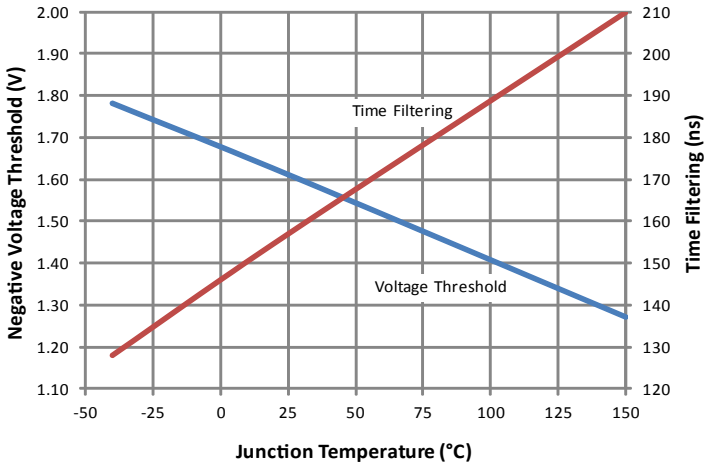


Figure 2. Missing diode protection versus device junction temperature

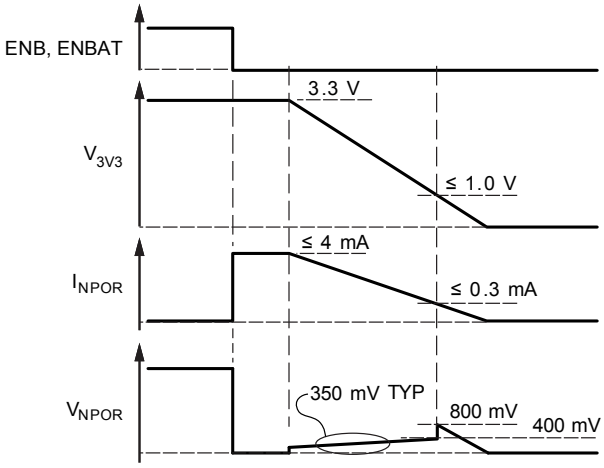


Figure 3. NPOR and 3V3 shutdown characteristics

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

5 V Regulator (V5)

The 5V linear regulator is provided to supply local circuitry. This regulator can deliver 310 mA typical, 215 mA minimum. When a direct short is applied to this regulator, the output current folds back to 0 V at approximately 92 mA typical (figure 4).

5 V Protected Tracking Regulator (V5P)

The 5VP linear tracking regulator is provided to supply remote circuitry such as off-board sensors. The output is monitored and in case of a short to battery condition the output is disabled and protected until the short is removed. The regulator can deliver 415 mA typical, 280 mA minimum. When a direct short is applied to this regulator, the output the current folds back to 0 V at approximately 110 mA typical (figure 5).

The V5P regulator is designed to track the either the 3V3 output or the V5 output. The V5P master reference is set by the status of the TRACK pin. The V5P regulator will track the 3.3V output to within ±0.5% and the V5 output to within ±25 mV under normal steady state operating conditions. If the master reference (either 3V3 or V5) is decreasing, the V5P regulator will accurately track the master reference down to the point at which the master reference crosses its undervoltage threshold (either $V_{3V3UV(L)}$ or $V_{1V2UV(L)}$ in the Electrical Characteristic tables).

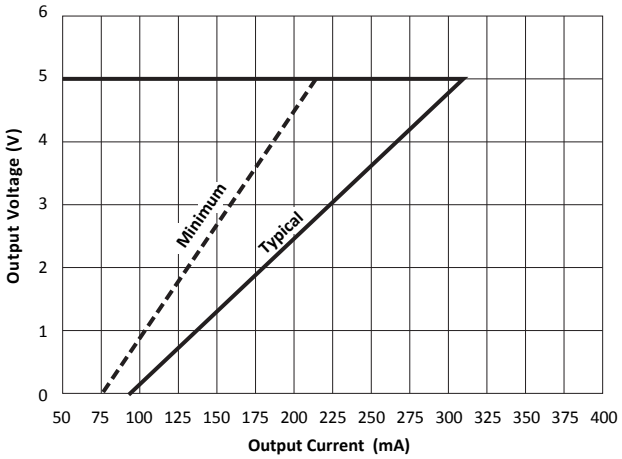


Figure 4. Fold back current limiting of the 5 V regulator

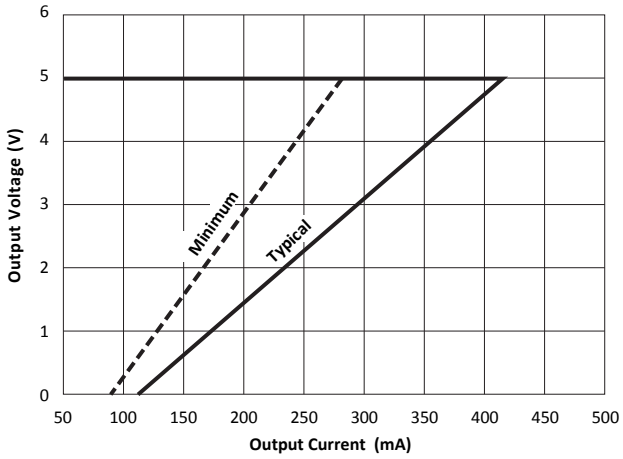


Figure 5. Fold back current limiting of the 5VP regulator

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Figures 6 and 7 show the A4407 operation when the V5P pin is shorted to ground and V_{IN} (battery). In both cases, the V5P output is disabled and/or disconnected while the other outputs (VREG, V5, V33, and 1V5) remain active.

Tracking Control

The TRACK input sets the master reference for the V5P tracking regulator. TRACK is meant to be either connected to ground or left unconnected by the PCB routing. When TRACK is left unconnected, it is pulled high by an internal current source and V5P tracks the 3V3 regulator. When TRACK is connected to ground, then V5P tracks the V5 regulator.

3V3 Linear Regulator (3V3)

A 3.3 V linear regulator can be implemented using an external MOSFET. In the event the 3.3 V regulator output is shorted to ground, the A4407 protects the external MOSFET by folding back when the programmed current limit, I_{3V3LIM}, is exceeded. The current limit is determined by the voltage developed across the external sense resistor, R_{CL1}, shown in the Functional Block diagram. The 3.3 V regulator current limit can be calculated using the following formula:

$$I_{3V3LIM} = V_{CL3V3} / R_{CL1} \quad (6)$$

where V_{CL3V3} is documented in the Electrical Characteristics table, 235 mV typical. Usually, R_{CL1} has a fairly low value so it will not dissipate significant power ($^1/_4$ W should be adequate) but the tolerance should be 1% or less. When I_{3V3LIM} is exceeded, the maximum load current through the external MOSFET is folded back to 27% typical of I_{3V3LIM} as shown in figure 8.

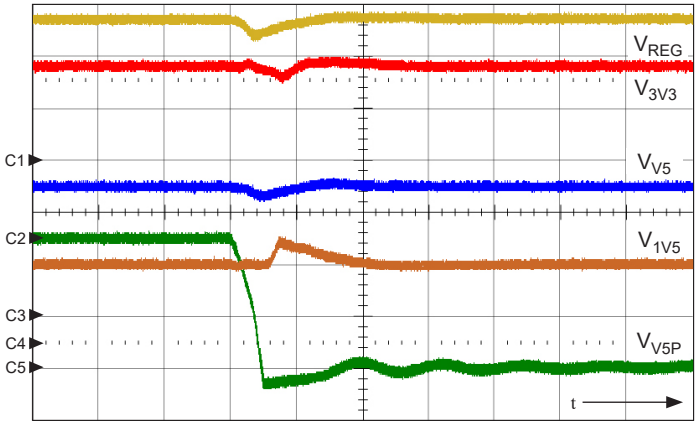


Figure 6. V5P shorted to ground in 5 µs (D_{V5P} is populated); shows V_{REG} (ch1, 2 V/div.), V_{3V3} (ch2, 1 V/div.), V_{V5} (ch3, 2 V/div.), V_{1V5} (ch4, 1 V/div.), V_{V5P} (ch5, 2 V/div.), t = 10 µs/div.

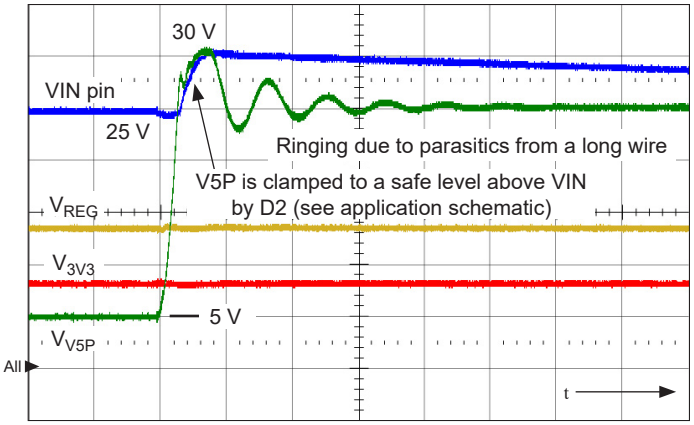


Figure 7. V5P is shorted to a 25 V battery; shows V_{VREG} (ch1, 2 V/div.), V_{3V3} (ch2, 2 V/div.), VIN pin (ch3, 5 V/div.), V_{V5P} (ch4, 5 V/div.), t = 10 µs/div.

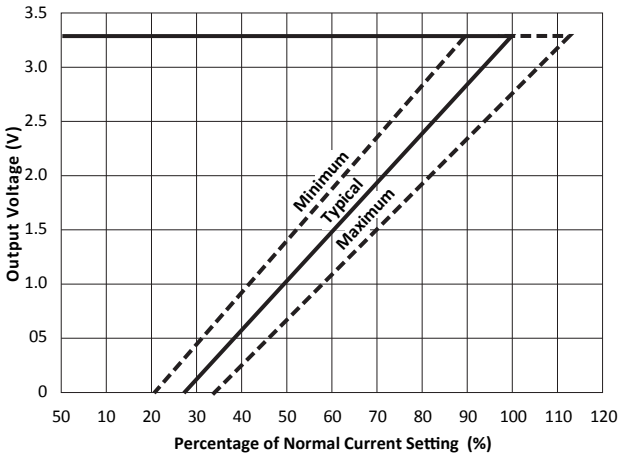


Figure 8. Fold back current limiting of the 3V3 regulator

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

1.2 V/1.5 V/1.8 V Linear Regulator (1V2)

A 1.2 V, 1.5 V, or 1.8 V linear regulator can be implemented using an external MOSFET. In the event this regulator output is shorted to ground, the A4407 protects the external MOSFET by folding back when the programmed current limit, I_{1V2LIM}, is exceeded. The current limit is determined by the voltage developed across the external sense resistor, R_{CL2}, shown in the Functional Block diagram. The 1.2 V/1.5 V/1.8 V regulator current limit can be calculated using the following formula:

$$I_{1V2LIM} = V_{CL1V2} / R_{CL2} \quad (7)$$

where V_{CL1V2} is documented in the Electrical Characteristic table, 218 mV typical. Usually R_{CL2} has a fairly low value so it will not dissipate significant power ($^1/_4$W should be adequate) but the tolerance should be 1% or less. When I_{1V2LIM} is exceeded, the maximum load current through the external MOSFET is folded back to 27% typical of I_{1V2LIM}, as shown in figure 9.

This regulator is designed to provide 1.2 V, but by using an external resistive divider between V_{OUT1V2} and the 1V2 pin, other voltages can be achieved, such as1.5 V or 1.8 V.

Charge Pump

The charge pump is used to generate a supply above V_{IN}. A 0.22 µF monolithic ceramic capacitor should be connected between VCP and VIN to act as a reservoir to run the internal DMOS and the external MOSFETs. The VCP voltage is internally monitored to ensure that the switching regulator would be disabled in the case of a fault condition. A 0.22 µF ceramic monolithic capacitor should be connected between CP1 and CP2.

ENBAT

ENBAT is a level-triggered enable input, used to enable the device based on a high voltage ignition or battery switch (via a 1 kΩ resistor). The ENBAT comparator thresholds are $V_{IGN(L)}$ = 2.2 V minimum and $V_{IGN(H)}$ = 4.0 V maximum. ENBAT is used only as a momentary switch to enable, or wake up, the A4407.

The ENB and ENBAT signals are logically ORed together internally, so individually either can wake up the A4407, that is, only one of these two inputs must be pulled high in order to enable the A4407. However, when ENBAT is removed, ENB must be high to keep the A4407 enabled. If there is no need for the ignition switch, ENBAT can be pulled low, making ENB a single reset control. Power-up and power-down scenarios using these inputs are shown in figures 10 and 11.

When an external resistor and capacitor are used to form a low-pass filter to the ENBAT pin, then a 100 Ω resistor must be used to prevent the external capacitor from discharging into and damaging the ENBAT pin. See the Functional Block diagram for connection of these three components.

ENBATS

When a logic high is sensed on the ENBAT input, the ENBATS open drain output goes high, signaling to the user that the ignition input is high. When a logic low is sensed on the ENBAT input, then ENBATS transitions low. The ENBATS input logic levels are identical to the ENBAT input logic levels.

ENB

This pin can be used as an enable input from either a DSP or a microcontroller. This input has an internal pull down resistor so it can be left unconnected if not needed.

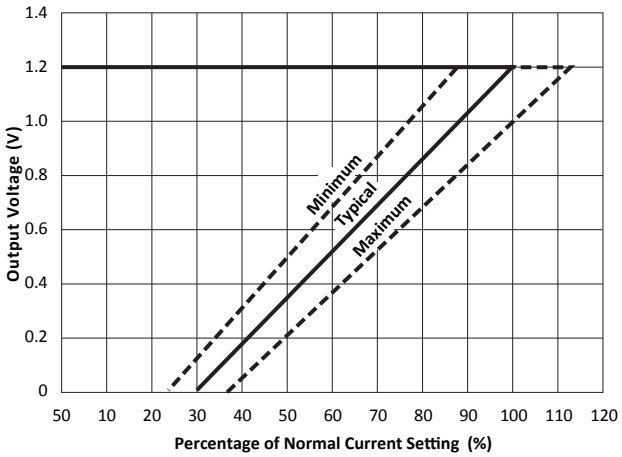


Figure 9. Fold back current limiting of the 1V2 regulator

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

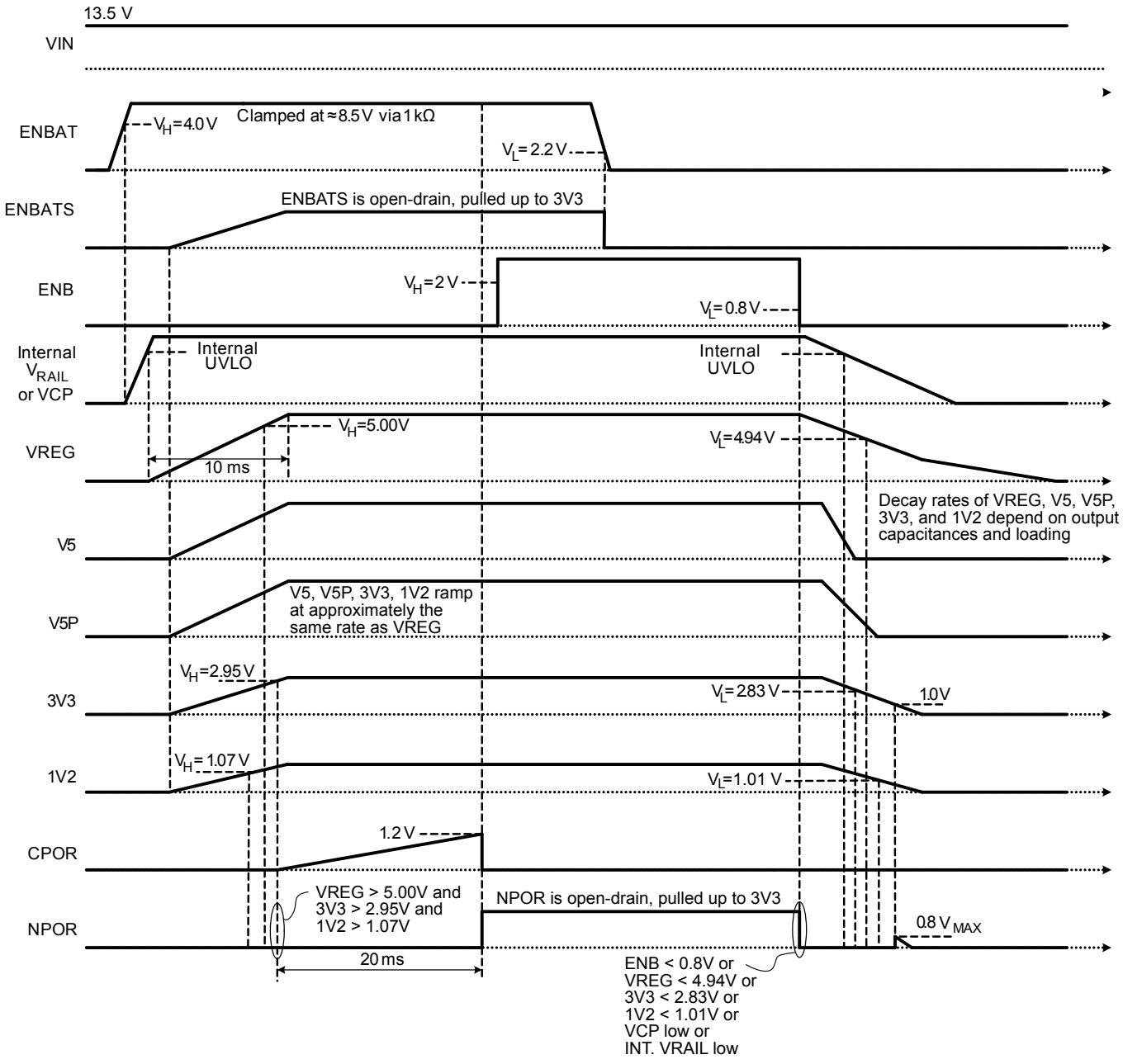


Figure 10. Typical power-up and power-down by ENBAT and ENB with V_{IN} = 13.5 V; ENBATS is assumed to be connected to 3V3 via a pull up resistor

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

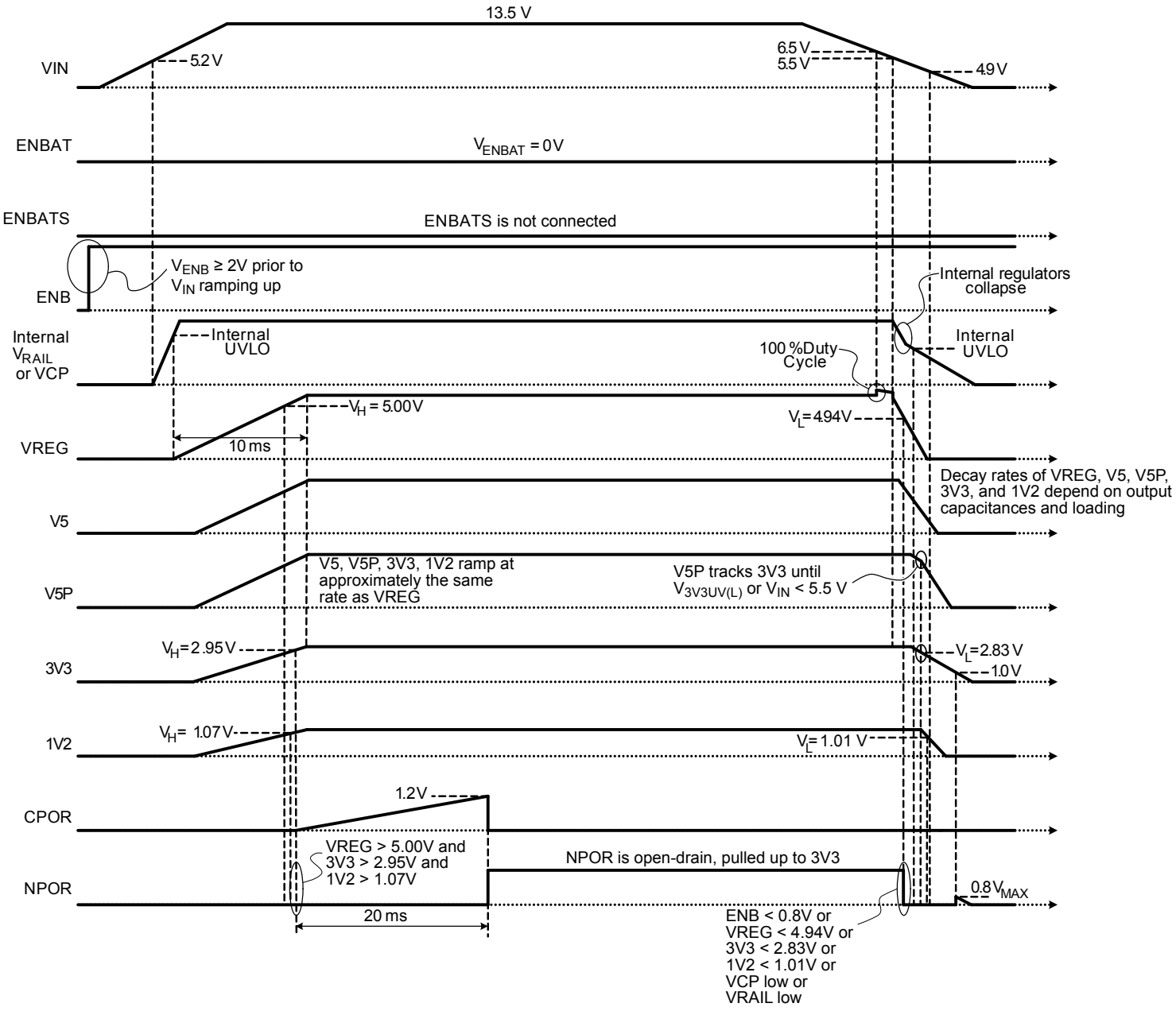


Figure 11. Typical power up and power down via VIN with ENB always logic high; ENBAT and ENBATS are not used

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application Information

Component Selection

Buck On-Time and Switching Frequency

In order for the switcher to maintain regulation, the energy that is transferred to the inductor during the on-time must be transferred to the capacitor during the off-time. Because of this relationship, the load current and IR drops, as well as the input and output voltages, affect the on-time of the converter. The equation that governs switcher on-time is:

$$t_{ON} = \frac{T_{SW}\,[V_{REG} + (R_L \times I_{peak}) + V_f + (R_{SENSE} \times I_{pe}}{V_{IN} + V_f - (R_{DS(on)} \times I_{peak})} \quad (8)$$

The effects of the voltage drop on the inductor and trace resistance affect the switching frequency. However, the frequency variation due to these factors is small, and is covered in the variation of the switcher period, which is ±25% of the target. Removing these current dependant terms simplifies the equation:

$$t_{ON} = \frac{V_{REG} + V_f + (R_{SENSE} \times I_{peak})}{V_{IN} + V_f - (R_{DS(on)} \times I_{peak})} \times \frac{1}{f_{SW}} \quad (9)$$

Be sure to use worst-case sense voltage and forward voltage of the diode including any effects due to temperature. For the example provided, assume a 1 A converter with a supply voltage of 13.5 V. The output voltage is 5.45 V, V_f is 0.45 V, $R_{SENSE} \times I_{peak}$ is 0.34 V, $R_{DS(on)} \times I_{peak}$ is 0.15 V, and the target frequency is 2.2 MHz. Applying equation 9, we can solve for t_{ON}:

$$t_{ON} = \frac{5.45\ (V) + 0.45\ (V) + 0.34\ (V)}{13.5\ (V) + 0.45\ (V) - 0.15\ (V)} \times \frac{1}{2.2\ (MHz)}$$

$$= 205\ ns$$

The formulas above describe how t_{ON} changes based on input and load conditions. Because load changes are minimal and the output voltage is fixed, the only factor that affects the on-time is the input voltage. The converter is able to maintain a constant period over a varying supply voltage because the on-time changes based on the input voltage. The current into the TON pin is derived from a resistor tied to VIN, which sets the on-time proportional to the supply voltage. Selecting the resistor value based on the t_{ON} calculated above is done using the following formula:

$$R_{TON} = \frac{V_{IN} \times (t_{ON} - 5\ (ns))}{6.36 \times 10^{-12}} \quad (10)$$

When the resistor is selected and a suitable t_{ON} is found, t_{ON} must be demonstrated that it does not, under worst-case conditions, exceed the minimum on-time or minimum off-time of the converter. The minimum on-time occurs at maximum input voltage and minimum load. The maximum off-time occurs at minimum supply voltage and maximum load. For supply voltages above 6.5 V but below 8.6 V, refer to the section entitled Low Voltage Operation.

Low Voltage Operation

The converter can run at very low input voltages; for example, with a 5.25 V output, the minimum input supply can be as low as 5.5 V. When operating at high frequencies, the on-time of the converter must be very short because the available period is short. At high input voltages the converter should not violate the minimum on-time, $t_{ON(min)}$, and at low input voltages the converter should not violate the minimum off-time, $t_{OFF(min)}$. Rather than limit the supply voltage range, the converter solves this problem by automatically increasing the period. With the period extended, the converter does not violate the minimum on-time or off-time specifications. If the input voltage is between 8.6 and 31 V, the converter will maintain a constant period. When calculating worst case on- and off-times, make sure to use the highest switching frequency if the supply voltage is in that range.

When operating at voltages below 8.6 V, additional care must be taken when selecting the inductor and diode. At low voltages the maximum current may be limited, due to the IR drops in the current path. When selecting external components for low voltage operation, the IR drops must be considered when determining on-time, so the complete formula (equation 8) should be used to make sure the converter does not violate the timing specification.

Inductor Selection

Choosing the proper inductor is critical to the correct operation of the switcher. The converter is capable of running at frequencies above 2 MHz, making it possible to use small inductor values and reducing cost and board area.

The inductor value determines the ripple current. It is important to size the inductor so that under worst-case conditions the overcurrent threshold equals the average current minus half the ripple current plus reasonable margin. When the ripple current is too large, the converter reaches current limit. Typically, peak-to-peak ripple current should be limited to 20% to 25% of the maximum average load current.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Worst-case ripple current occurs at maximum supply voltage. After calculating the duty cycle for this condition, the ripple current can be calculated:

$$D = \frac{V_{REG} + V_f + (R_{SENSE} \times I_{peak})}{V_{IN}(max) + V_f - (R_{DS(on)} \times I_{peak})} \quad (11)$$

Using the duty cycle, the inductor value can be calculated using the formula below:

$$L = \left(\frac{V_{IN} - V_{REG}}{I_{ripple}} \right) \times D \times \frac{1}{f_{SW}(min)} \quad (12)$$

Where I_{ripple} is 25% of the maximum load current, and $f_{SW}(min)$ is the minimum switching frequency, nominal frequency minus 25%. Continuing the example used above (using equation 9), a 1 A converter with a supply voltage of 13.5 V is the design objective. Assume the supply voltage can vary by ±10%, the output voltage is 5.45 V, V_f is 0.5 V, V_{SENSE} is 0.20, and the target frequency is 2.2 MHz. Using equation 11, the duty cycle is calculated to be 36.45%. Assume the worst-case frequency is 2.2 MHz minus 20%, or 1.76 MHz. Using these numbers in equation 12 shows that the minimum inductance for this converter is 9.6 µH.

Output Capacitor

The buck converter is designed to operate with a low-ESR ceramic output capacitor. When choosing a ceramic capacitor, make sure the rated voltage is at least 3 times the maximum output voltage of the converter. This is because the capacitance of a ceramic decreases the closer it is operated to its rated voltage. It is recommended that the output be decoupled with a 10 µF, 16 V, X7R ceramic capacitor. Larger capacitance may be required on the outputs if load surges dramatically influence the output voltage.

Output voltage ripple is determined by the output capacitance; and the effects of ESR and ESL can be ignored, assuming recommended layout techniques are followed. The output voltage ripple is approximated by:

$$V_{ripple} = I_{ripple} / (8 \times f_{sw} \times C_{OUT}) \quad (13)$$

Input Capacitor

The value of the input capacitance affects the amount of current ripple on the input. This current ripple is usually the source of supply-side EMI. The amount of interference depends on the impedance from the input capacitor and the bulk capacitance located on the supply bus. In addition to the two 4.7 µF capacitors, placing a small 0.1 µF ceramic capacitor very close to the input supply pin helps reduce EMI effects. The small capacitor helps reduce the very high frequency transient currents on the supply line.

Non-Synchronous Diode

The non-synchronous diode (D_{BUCK} in the Functional Block diagram) conducts the current during the off-time. A Schottky diode is required to minimize the forward drop and switching losses. In order to size the diode correctly, it is necessary to find the average diode conduction current using the following formula:

$$I_{D(avg)} = I_{load} \times (1 - D(min)) \quad (14)$$

where D(min) is the minimum duty cycle, defined as:

$$D(min) = (V_{REG} + V_f) / (V_{IN} + V_f) \quad (15)$$

where V_{IN} is the maximum input voltage and V_f is the maximum forward voltage of the diode.

The average power dissipation in the diode is:

$$P_{DBUCK(avg)} = I_{BUCK(avg)} \times D(min) \times V_f \quad (16)$$

The power dissipation in the sense resistor must also be considered using I^2R and the minimum duty cycle.

External MOSFET Selections

To choose an external MOSFET for the 3.3 V or for the 1.2 V/1.5 V/1.8 V linear regulator, consider: the maximum drain-to-source voltage, V_{DS}, the maximum continuous drain current, I_D, the threshold voltage, V_{GSTH}, the on-resistance ($R_{DS(on)(FET)}$), and the thermal resistance ($R_{\theta JC(FET)}$).

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The buck switcher pre-regulates the voltage to the external MOSFET, so even under worst-case conditions, it does not have to support more than 7 V from drain to source. Also, the external LDOs usually deliver 500 mA to 1 A. Numerous MOSFETs are available, with V_{DS} ratings of at least 20 V, that can support much more than 1A. These two goals should not be difficult to achieve.

The A4407 gate drive circuitry is guaranteed to pull the G3V3 and G1V2 voltage down to 1 V, maximum. Therefore, Allegro recommends using external MOSFETs with a V_{GS} threshold higher than 1 V. Do not use a MOSFET that will conduct significant current when V_{GS} is at 1 V and the system is at the highest expected ambient temperature.

One of the more critical specifications is the MOSFET on-resistance, $R_{DS(on)(FET)}$. If the on-resistance were too high, then the external regulator would not be able to maintain its output at the maximum load current. Calculate the typical $R_{DS(on)(FET)}$ (at 25°C) using the following formula:

$$R_{DS(on)(FET)25C} < 0.6 \times \left(\frac{1.56\ (V)}{I_{3V3LIM}} - R_{DROP1} \right) \qquad (17)$$

where I_{3V3LIM} is the maximum current from the 3.3 V regulator and R_{DROP1} is the value of the resistor connected from the CL3V3 pin to the drain of the MOSFET. The multiplier of 0.6 in the equation allows a 66% increase in $R_{DS(on)(FET)}$ when the MOSFET is very hot.

The necessity and value of R_{DROP1} is closely related to the thermal resistance of the MOSFET, $R_{\theta JC(FET)}$. For a medium size MOSFET (like a SOT-223) including R_{DROP1} in the PCB layout is highly recommended. For a large size MOSFET with a very low thermal resistance (like a D^2PAK) R_{DROP1} is probably not necessary.

The thermal resistance of a MOSFET is a function of die size, package size, and cost. So choosing R_{DROP1} and $R_{\theta JC(FET)}$ together should result in optimal performance, minimal component sizes, and lowest system cost. Determining the value and power dissipated by the series dropping resistor and MOSFET thermal resistance are addressed in detail in the next section.

3.3V Regulator External Resistors (R_{CL1}, R_{DROP1})

In the Functional Block diagram, there are two resistors, R_{CL1} and R_{DROP1} from the output of the buck regulator to the drain of the 3.3 V external MOSFET. R_{CL1} must always be present because it sets the 3.3 V regulator current limit threshold. However, R_{DROP1}, if used, prevents the external MOSFET from dissipating too much power during certain conditions. In particular, when the battery voltage is extremely low ($V_{BAT} \leq 6.5$ V) and the buck regulator transitions to dropout mode (100% duty cycle) then V_{REG} is approximately 1 V higher than normal. In this situation, without R_{DROP1}, the MOSFET could dissipate too much power.

The value of R_{DROP1} depends on the maximum PCB temperature, the maximum current load on the 3.3 V regulator, the maximum allowable junction temperature of the MOSFET, and the thermal resistance of the MOSFET. The 3.3 V regulator must conduct its own load current (250 mA in the Functional Block diagram) plus the load planned for the 1.2 V/1.5 V/1.8 V regulator (450 mA to 525 mA in the Functional Block diagram).

As the thermal resistance of the MOSFET decreases, the required value of R_{DROP1} also decreases. If the MOSFET is relatively large and has a very low thermal resistance then R_{DROP1} is not required (0 Ω).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Figure 12 shows recommended values of R_{DROP1} versus the MOSFET thermal resistance at various 3.3 V regulator maximum current settings, I_{3V3LIM}. This graph assumes: steady-state operation (that is, for t >> 50 ms), a PCB temperature of 135°C, a maximum MOSFET junction temperature of 175°C, a duty cycle for t_{ON} of 100% , a V_{BAT} of 6.69 V, and an output of 3.23 V from the 3.3 V linear regulator. This graph takes into account the voltage drop across the 3.3 V current limit resistor, R_{CL1}.

After a value for R_{DROP1} is determined, the designer should calculate its maximum power dissipation ($I^2 \times R$) and select an appropriate component, allowing adequate design margin. Assuming the R_{DROP1} value was chosen from figure 12, then figure 13 shows the power dissipated by R_{DROP1} versus the MOSFET thermal resistance at various 3.3 V regulator current settings.

The exact value of R_{DROP1} is not critical, so a component with 1% or 5% tolerance could be used.

1.2 V/1.5 V/1.8 V Regulator External Resistors (R_{CL2}, R_{DROP2})

In the Functional Block diagram, there are two resistors, R_{CL2} and R_{DROP2} from the output of the 3.3 V regulator to the drain of the 1.2 V/1.5 V/1.8 V external MOSFET. R_{CL2} must always be present because it sets the 1.2 V/1.5 V/1.8 V regulator current limit threshold. However, R_{DROP2}, if used, prevents the external MOSFET from dissipating too much power.

The value of R_{DROP2} depends on the maximum PCB temperature, the maximum current load on the 1.2 V/1.5 V/1.8 V regulator (I_{1V2LIM}), the maximum allowable junction temperature of the MOSFET, and the thermal resistance of the MOSFET.

As the thermal resistance of the MOSFET decreases, the required value of R_{DROP2} also decreases. If the MOSFET is relatively large and has a very low thermal resistance, then R_{DROP2} is not required (0 Ω).

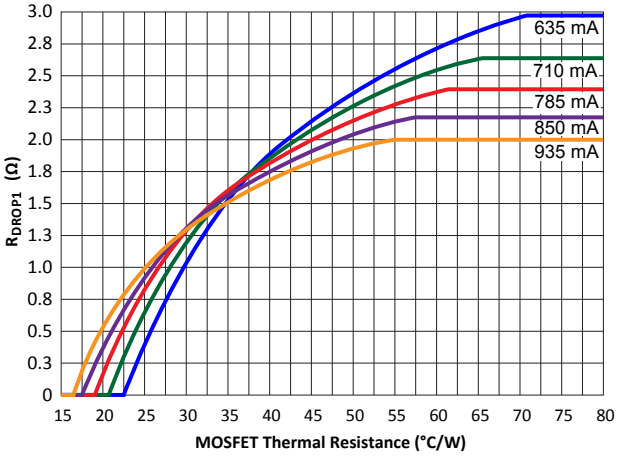


Figure 12. R_{DROP1} value versus 3.3 V MOSFET thermal resistance at various 3.3 V regulator maximum current settings

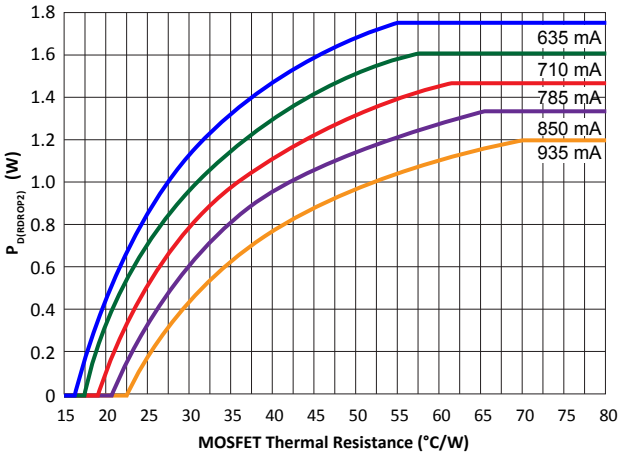


Figure 13. R_{DROP1} power dissipation versus 3.3 V MOSFET thermal resistance at various 3.3 V regulator maximum current settings

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Figure 14 shows recommended values of R_{DROP2} versus MOSFET thermal resistance at various 1.5 V regulator maximum current settings, I_{1V2LIM}. This graph assumes a PCB temperature of 135°C, a maximum MOSFET junction temperature of 175°C, and 3.37 V from the upstream (3.3 V) linear regulator. This graph takes into account the voltage drop across the 1.5 V current limit resistor, R_{CL2}.

After a value of R_{DROP2} is determined the designer should calculate its maximum power dissipation ($I^2 \times R$) and select an appropriate component, allowing adequate design margin. Assuming the R_{DROP2} value was chosen from figure 14, then figure 15 shows the power dissipated by R_{DROP2} versus the MOSFET thermal resistance at various 1.5 V regulator current settings.

The exact value of R_{DROP2} is not critical, so a component with 1% or 5% tolerance could be used.

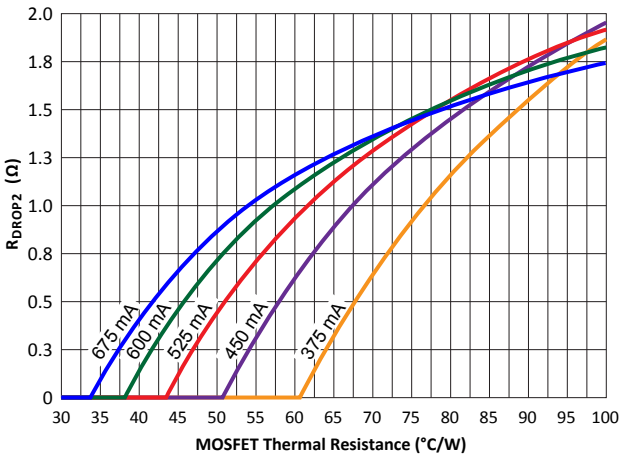


Figure 14. R_{DROP2} value versus 1.5 V MOSFET thermal resistance at various 1.5 V regulator maximum current settings

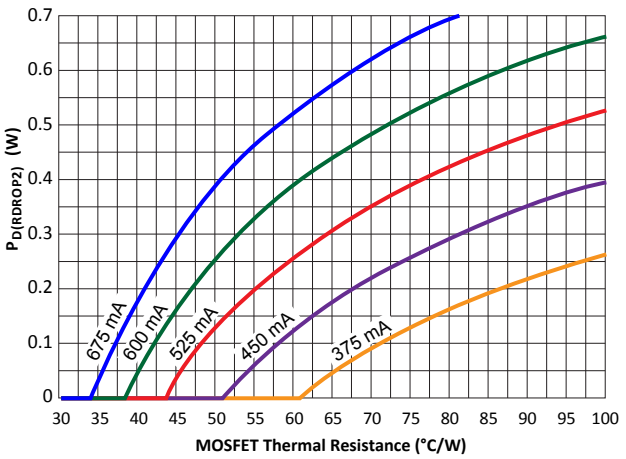


Figure 15. R_{DROP2} power dissipation versus 1.5 V MOSFET thermal resistance at various 1.5 V regulator maximum current settings

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PCB Component Placement and Routing

The board layout has a large impact on the performance of the device. It is important to isolate high current ground returns to minimize ground bounce that could produce reference errors in the device. The method used to isolate power ground from noise sensitive circuitry is to use a star ground. This approach makes sure that the high current components such as the input capacitor, output capacitor, and diode have very low impedance paths to each other. Figure 16 illustrates the technique.

The ground traces for each of the components should be very close to each other and should be connected to each other on the same surface as the components. Internal ground planes should not be used for the star ground connection, because vias add impedance to the current path.

In order to further reduce noise effects on the PCB, noise sensitive traces should not be connected to internal ground planes. The feedback network from the switcher output should have an independent ground trace that goes directly to the exposed pad underneath the device. The exposed pad should be connected to internal ground planes and to any exposed copper used for heat dissipation. If the grounds from the device are also connected directly to the exposed pad, the ground reference from the feedback network will be less susceptible to noise injection or ground bounce.

To reduce radiated emissions from the high frequency switching nodes, it is important to have an internal ground plane directly under the LX node. That ground plane should not be broken directly under the node, because the lowest impedance path back to the star ground is directly under the signal trace. If another trace does break the return path, the energy would have to find another path, which would be through radiated emissions.

The peak-to-peak amplitude of the buck current sense signal will typically be only tens of millivolts. The current sense pins, ISEN+ and ISEN–, and internal differential amplifier comprise a differential signal receiver, and balanced pair of traces should be routed from the pins of the buck current sense resistor, R_{SENSE}, as shown in figure 17 (upper panel). The ISEN+ pin and the sense resistor ground should not be separated by simply using local via connections to the ground plane (figure 17 lower panel). Incorrect routing of the ISEN+ pin would likely add an offset error to the buck current sense signal.

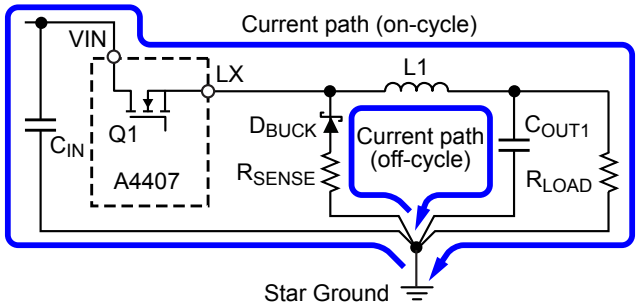


Figure 16. Illustration of star ground connection

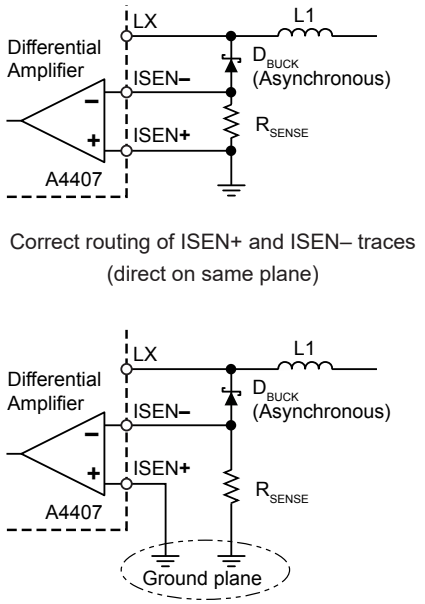


Figure 17. Comparison of routing paths for the traces between the A4407 ISEN+ and ISEN– traces and the sense resistor, R_{SENSE}

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application Circuit Performance

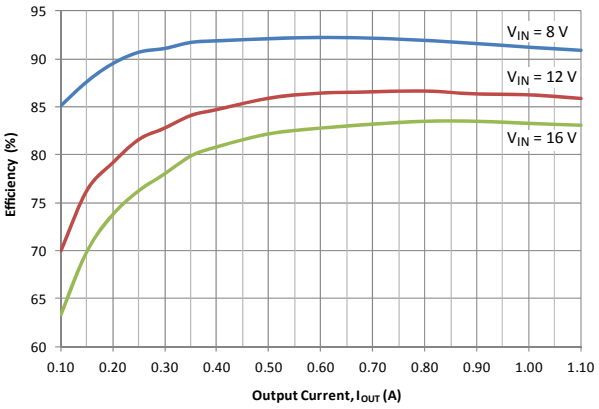
Application schematic is shown in Functional Block diagram.

Bill of Materials for Critical Components

This design is capable of full load, 135°C ambient, and 5.5 V_{BAT} indefinitely with an adequate thermal solution

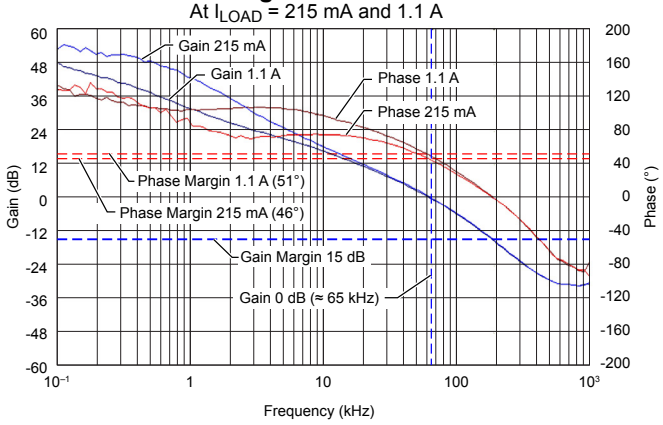
Component	Description	Package	Manufacturer	Part Number
Q_{3V3}	MOSFET, 40 V, 90 A, 4.3 mΩ, T_J 175°C	DPAK	Infineon	IPD90N04S3-04
Q_{1V5}	MOSFET, 30 V, 30 A, 13.5 Ω, T_J 175°C	DPAK	Infineon	IPD135N03LG
R_{SENSE}, R_{CL1}	Resistor, 0.300 Ω, 1/4 W, 1%	1206		
R_{CL2}	Resistor, 0.390 Ω, 1/4 W, 1%	1206		
R_{DROP1}	Resistor, 2.2 Ω total, 2 W total, 5%	Multiple SMT components may be used in parallel or series		
R_{DROP2}	Resistor, 1.5 Ω, 1 W, 5%	2512	Vishay/Dale	CRCW25121R50JNEG
C_{IN1}, C_{IN2}	Capacitor, Ceramic, 4.7 µF, 50 V, 10%, X7R	1210	Murata	GCM32ER71H475KA55L
C_{OUT1}	Capacitor, Ceramic, 10 µF, 16 V, 10%, X7R	1206	Kemet	C1206C106K4RACTU
C_{OUT2}	Capacitor, Ceramic, 0.47 µF, 16 V, 10%, X7R	0603		
C_{OUT3V3}, C_{OUT1V5}, C_{OUTV5}, C_{OUTV5P}	Capacitor, Ceramic, 2.2 µF, 16 V, 10%, X7R	1206	Murata	GRM31MR71C225KA35L
D_{BUCK}, D_{IN}	Diode, Schottky, 2 A, 40 V	SMA	Diodes, Inc.	B240A-13-F
L1	Inductor, 10 µH, 64 mΩ, 2.39 A_{sat}, 165°C	7.6 x 7.6 mm	Cooper/Bussman	DRA73-100-R

Buck Regulator (VREG) Efficiency

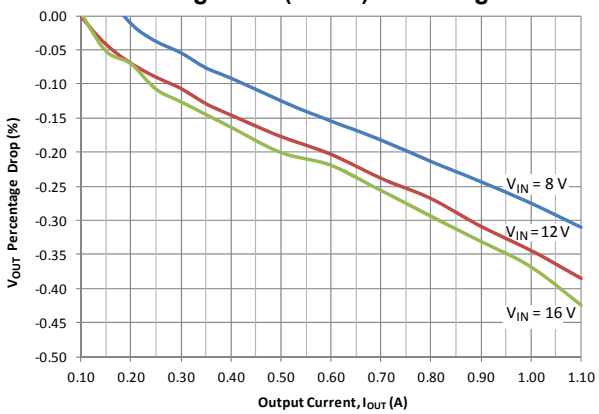


Buck Regulator Bode Plots

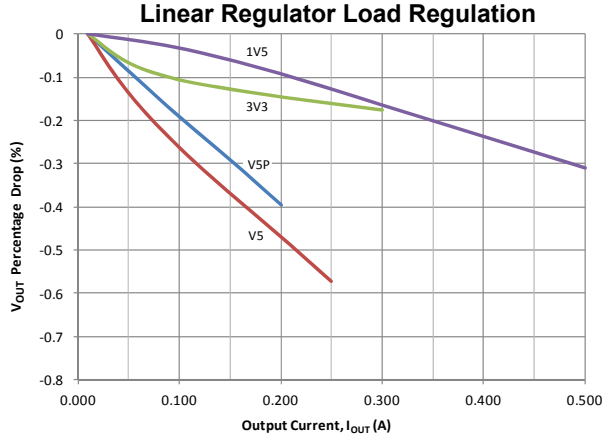
At I_{LOAD} = 215 mA and 1.1 A



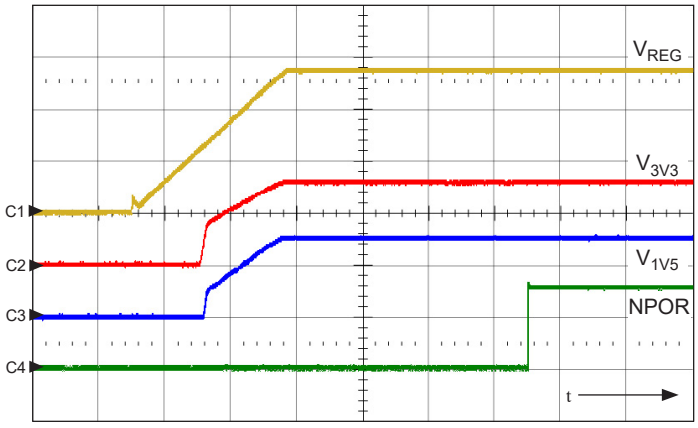
Buck Regulator (VREG) Load Regulation



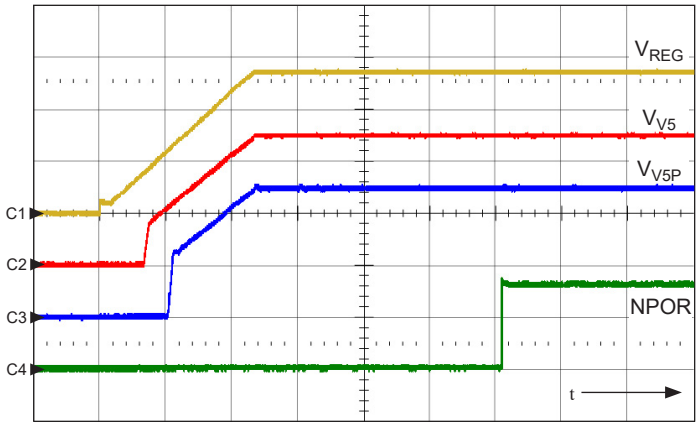
Linear Regulator Load Regulation



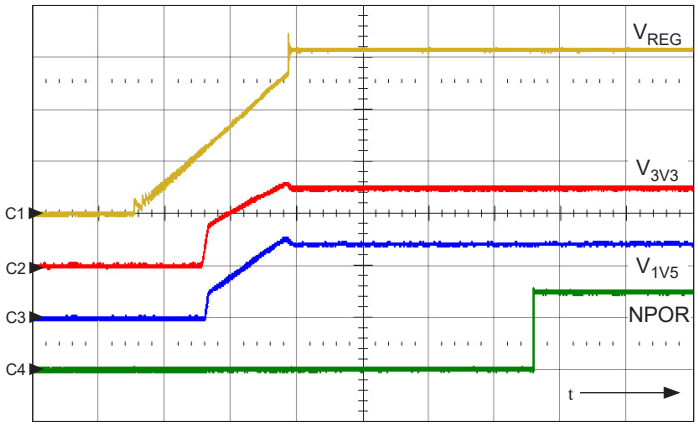
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



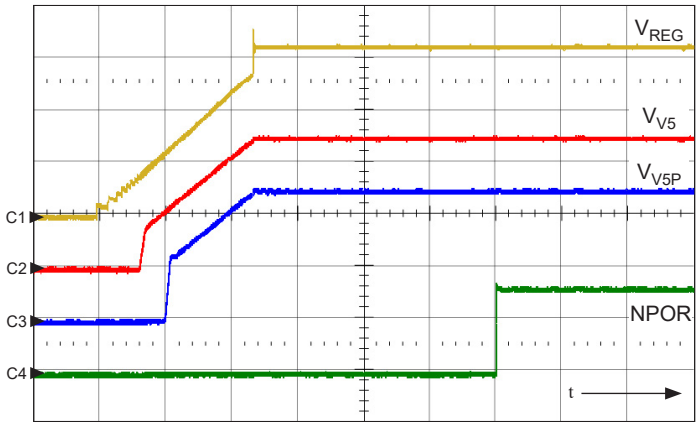
Startup at V_{BAT} = 13.5 V; shows V_{REG} (ch1, 2 V/div.), V_{3V3} (ch2, 2 V/div.), V_{1V5} (ch3, 1 V/div.), NPOR (ch4, 2 V/div.), t = 5 ms/div.



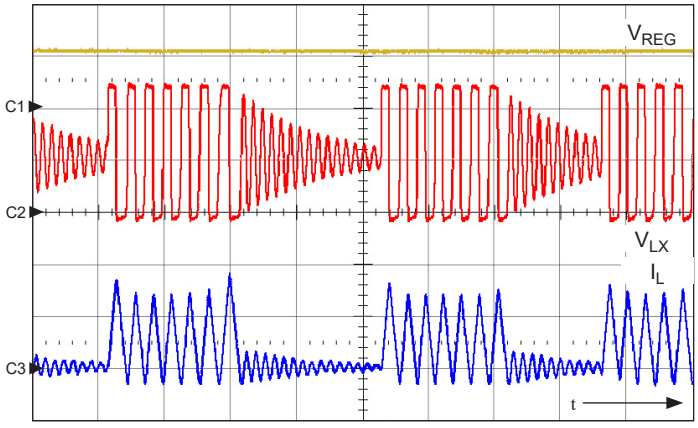
Startup at V_{BAT} = 13.5 V; shows V_{REG} (ch1, 2 V/div.), V_{V5} (ch2, 2 V/div.), V_{V5P} (ch3, 2 V/div.), NPOR (ch4, 2 V/div.), t = 5 ms/div.



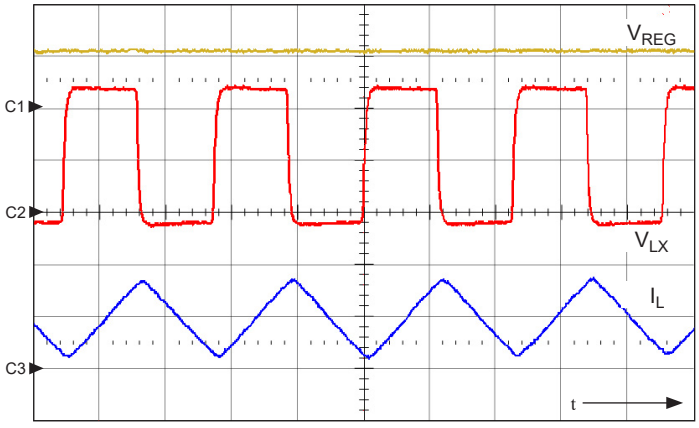
Startup at V_{BAT} = 6.5 V; shows V_{REG} (ch1, 2 V/div.), V_{3V3} (ch2, 2 V/div.), V_{1V5} (ch3, 1 V/div.), NPOR (ch4, 2 V/div.), t = 5 ms/div.



Startup at V_{BAT} = 6.5 V; shows V_{REG} (ch1, 2 V/div.), V_{V5} (ch2, 2 V/div.), V_{V5P} (ch3, 2 V/div.), NPOR (ch4, 2 V/div.), t = 5 ms/div.

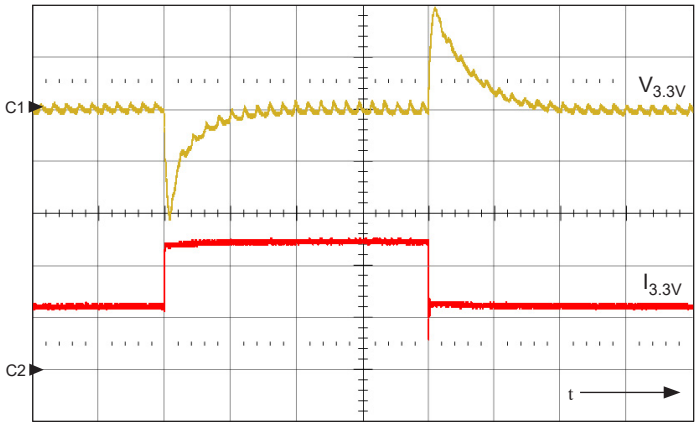


PWM at V_{BAT} = 12 V with a 25 mA load; shows V_{REG} (ch1, 5 V/div.), V_{LX} (ch2, 5 V/div.), I_L (ch3, 100 mA/div.), t = 2 µs/div.

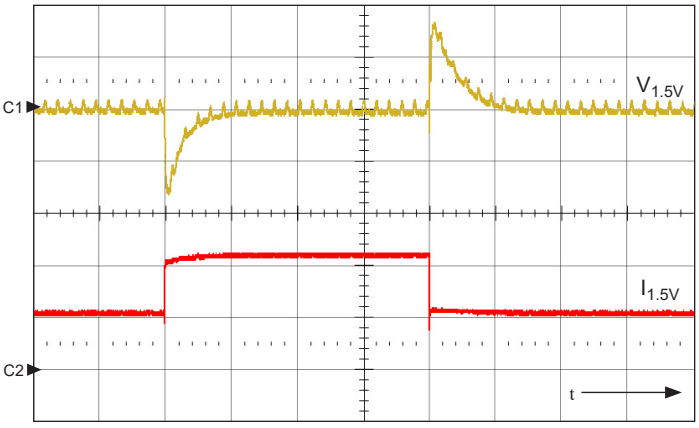


PWM at V_{BAT} = 12 V with a 1.0 A load; shows V_{REG} (ch1, 5 V/div.), V_{LX} (ch2, 5 V/div.), I_L (ch3, 100 mA/div.), t = 200 ns/div.

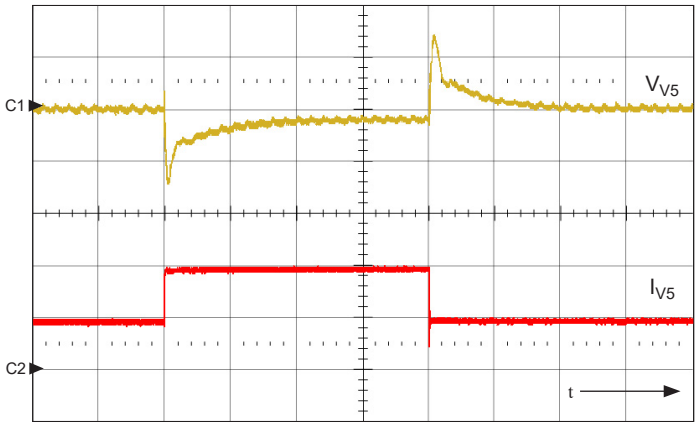
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



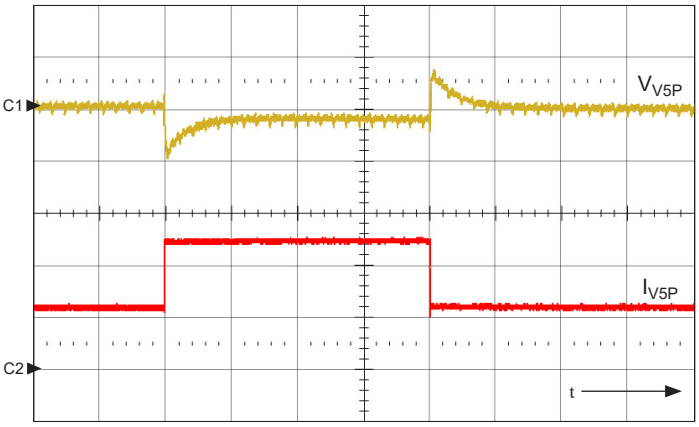
$V_{3.3V}$ transient response, 125 to 250 mA; shows $V_{3.3V}$ (ch1, 50 mV/div.), $I_{3.3V}$ (ch2, 100 mA/div.), t = 50 µs/div.



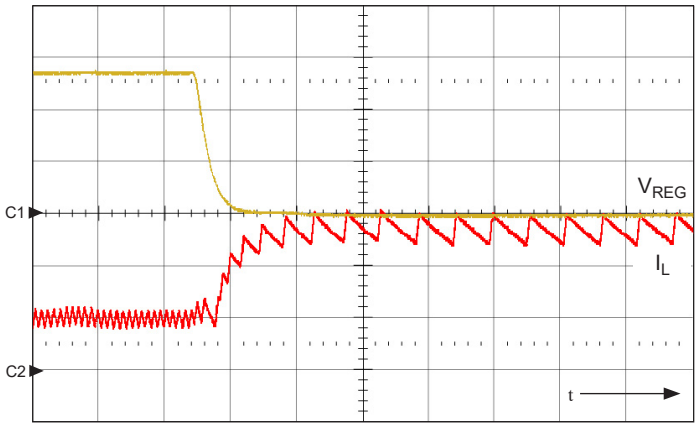
$V_{1.5V}$ transient response, 225 to 450 mA; shows $V_{1.5V}$ (ch1, 50 mV/div.), $I_{1.5V}$ (ch2, 200 mA/div.), t = 50 µs/div.



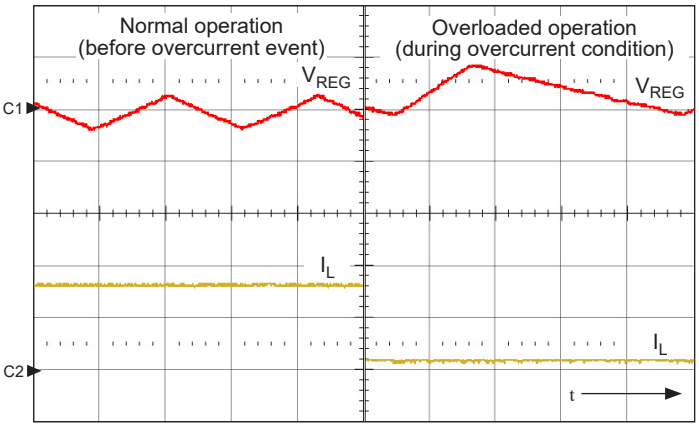
V_{V5} transient response, 100 to 200 mA; shows V_{V5} (ch1, 50 mV/div.), I_{V5} (ch2, 100 mA/div.), t = 50 µs/div.



V_{V5P} transient response, 125 to 250 mA; shows V_{V5P} (ch1, 50 mV/div.), I_{V5P} (ch2, 100 mA/div.), t = 50 µs/div.



V_{REG} short circuit operation at V_{IN} = 12 V; shows V_{REG} (ch1, 2 V/div.), I_L (ch2, 500 mA/div.), t = 5 µs/div.

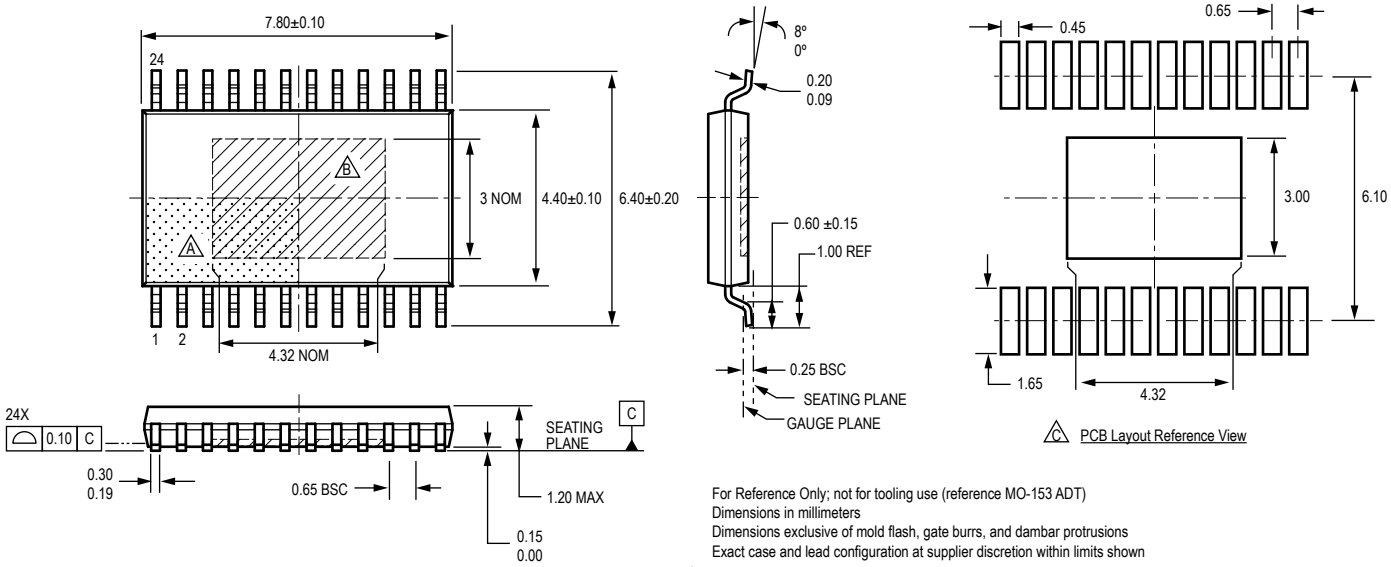


V_{REG} normal (left) and overload (right) operation at V_{IN} = 12 V; shows V_{REG} (ch1, 2 V/div.), I_L (ch2, 250 mA/div.)

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Package LP, 24-Pin TSSOP
with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
3	February 11, 2013	Update asynchronous diode description
4	December 13, 2019	Minor editorial updates

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com