

This IC, developed by CMOS technology, is a high-accuracy Hall IC that operates with a high-sensitivity, a high-speed detection and low current consumption.

The output voltage changes when this IC detects the intensity level of flux density. Using this IC with a magnet makes it possible to detect the open / close and rotation state in various devices. High-density mounting is possible by using the small SOT-23-3 package. Due to its high-accuracy magnetic characteristics, this IC can make operation's dispersion in the system combined with magnet smaller.

ABLIC Inc. offers a "magnetism simulation service" that provides the ideal combination of magnets and our Hall ICs for customer systems. Our magnetism simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.

For more information regarding our magnetism simulation service, contact our sales office.

## ■ Features

- |                                     |  |
|-------------------------------------|--|
| • Pole detection:                   | Detection of S pole  |
| • Detection logic for magnetism*1:  | Active "L", active "H"   |
| • Output form*1:                    | Nch open drain output, CMOS output   |
| • Magnetic sensitivity*1:           | $B_{OP} = 3.0 \text{ mT typ.}$<br>$B_{OP} = 4.5 \text{ mT typ.}$<br>$B_{OP} = 7.0 \text{ mT typ.}$ |
| • Operating cycle:                  | $t_{CYCLE} = 50 \mu\text{s typ.}$  |
| • Power supply voltage range:       | $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$   |
| • Operation temperature range:      | $T_a = -40^\circ\text{C to } +125^\circ\text{C}$   |
| • Lead-free (Sn 100%), halogen-free |  |

\*1. The Option can be selected.

## ■ Applications

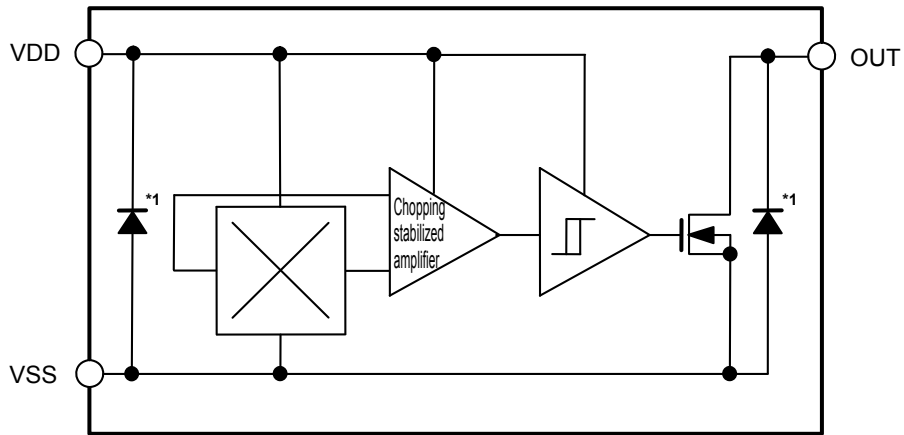
- Motor
- Housing equipment
- Industrial equipment

## ■ Package

- SOT-23-3

■ Block Diagrams

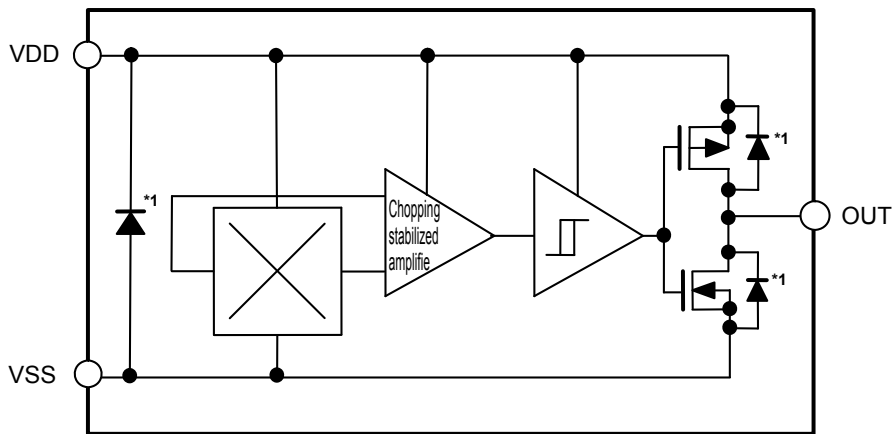
1. Nch open drain output product



\*1. Parasitic diode

Figure 1

2. CMOS output product

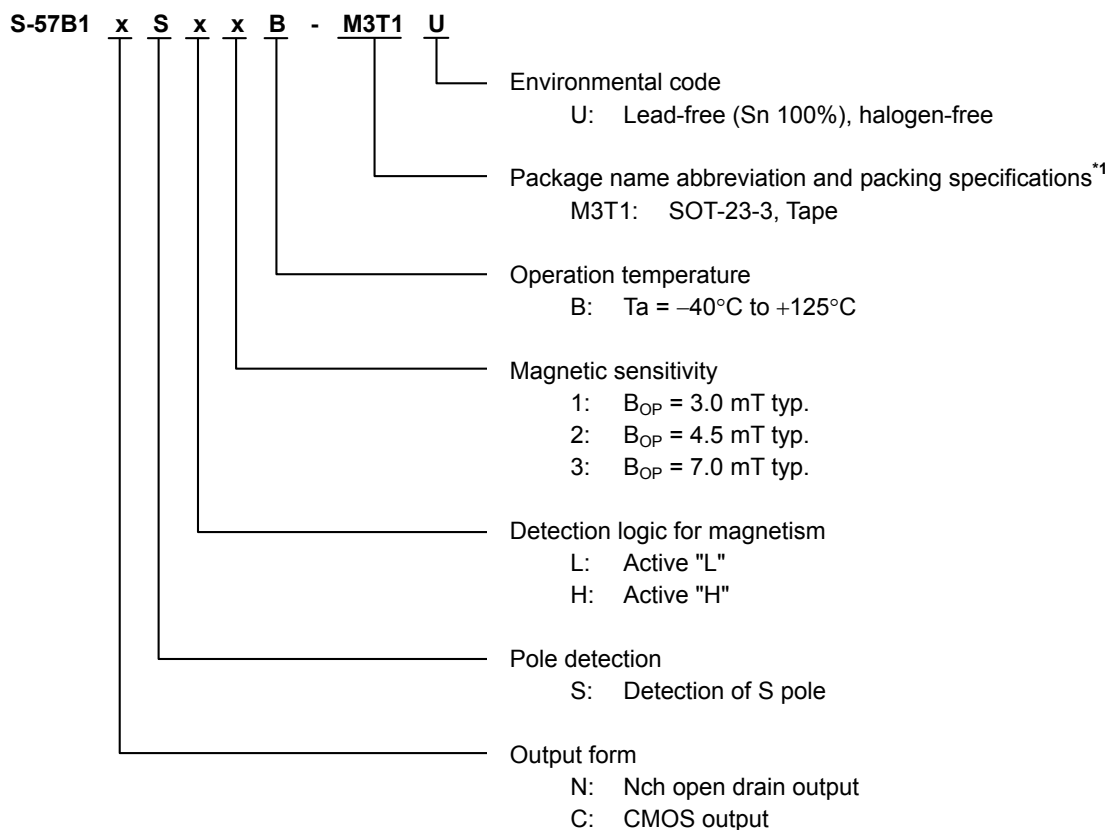


\*1. Parasitic diode

Figure 2

■ Product Name Structure

1. Product name



\*1. Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-3	MP003-C-P-SD	MP003-C-C-SD	MP003-Z-R-SD

3. Product name list

Table 2

Product Name	Output Form	Pole Detection	Detection Logic for Magnetism	Magnetic Sensitivity (B <sub>OP</sub> )
S-57B1NSL1B-M3T1U	Nch open drain output	S pole	Active "L"	3.0 mT typ.
S-57B1CSL3B-M3T1U	CMOS output	S pole	Active "L"	7.0 mT typ.

**Remark** Please contact our sales office for products other than the above.

■ Pin Configuration

1. SOT-23-3

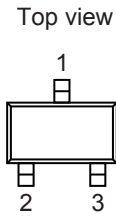


Figure 3

Table 3

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V <sub>DD</sub>	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 7.0	V
Output current	I <sub>OUT</sub>	±2.0	mA
Output voltage	Nch open drain output product	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 7.0	V
	CMOS output product	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Operation ambient temperature	T <sub>opr</sub>	-40 to +125	°C
Storage temperature	T <sub>stg</sub>	-40 to +150	°C

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Junction-to-ambient thermal resistance*1	θ <sub>JA</sub>	SOT-23-3	Board 1	-	200	-	°C/W
			Board 2	-	165	-	°C/W

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Thermal Characteristics" for details of power dissipation and test board.

## ■ Electrical Characteristics

Table 6

(Ta = +25°C, V<sub>DD</sub> = 5.0 V, V<sub>SS</sub> = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Power supply voltage	V <sub>DD</sub>	–	2.7	5.0	5.5	V	–	
Current consumption	I <sub>DD</sub>	Average value	–	1400	2000	μA	1	
Output voltage	V <sub>OUT</sub>	Nch open drain output product	Output transistor Nch, I <sub>OUT</sub> = 2 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I <sub>OUT</sub> = 2 mA	–	–	0.4	V	2
			Output transistor Pch, I <sub>OUT</sub> = –2 mA	V <sub>DD</sub> – 0.4	–	–	V	3
Leakage current	I <sub>LEAK</sub>	Nch open drain output product Output transistor Nch, V <sub>OUT</sub> = 5.5 V	–	–	1	μA	4	
Operating cycle	t <sub>CYCLE</sub>	–	–	50	100	μs	–	

■ Magnetic Characteristics

1. Product with  $B_{OP} = 3.0 \text{ mT typ.}$

Table 7

( $T_a = +25^\circ\text{C}$ ,  $V_{DD} = 5.0 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$  unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Operating point <sup>*1</sup>	S pole	$B_{OPS}$	–	1.4	3.0	4.0	mT	5
Release point <sup>*2</sup>	S pole	$B_{RPS}$	–	1.1	2.2	3.7	mT	5
Hysteresis width <sup>*3</sup>	S pole	$B_{HYSS}$	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	5

2. Product with  $B_{OP} = 4.5 \text{ mT typ.}$

Table 8

( $T_a = +25^\circ\text{C}$ ,  $V_{DD} = 5.0 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$  unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Operating point <sup>*1</sup>	S pole	$B_{OPS}$	–	2.5	4.5	6.0	mT	5
Release point <sup>*2</sup>	S pole	$B_{RPS}$	–	2.0	3.5	5.5	mT	5
Hysteresis width <sup>*3</sup>	S pole	$B_{HYSS}$	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.0	–	mT	5

3. Product with  $B_{OP} = 7.0 \text{ mT typ.}$

Table 9

( $T_a = +25^\circ\text{C}$ ,  $V_{DD} = 5.0 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$  unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Operating point <sup>*1</sup>	S pole	$B_{OPS}$	–	5.0	7.0	8.5	mT	5
Release point <sup>*2</sup>	S pole	$B_{RPS}$	–	3.7	5.2	7.2	mT	5
Hysteresis width <sup>*3</sup>	S pole	$B_{HYSS}$	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.8	–	mT	5

\*1.  $B_{OPS}$ : Operating point

$B_{OPS}$  is the value of magnetic flux density when the output voltage ( $V_{OUT}$ ) changes after the magnetic flux density applied to this IC by the magnet (S pole) is increased (the magnet is moved closer).

Even when the magnetic flux density exceeds  $B_{OPS}$ ,  $V_{OUT}$  retains the status.

\*2.  $B_{RPS}$ : Release point

$B_{RPS}$  is the value of magnetic flux density when the output voltage ( $V_{OUT}$ ) changes after the magnetic flux density applied to this IC by the magnet (S pole) is decreased (the magnet is moved further away).

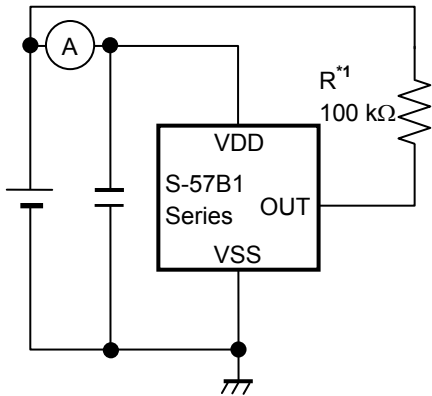
Even when the magnetic flux density falls below  $B_{RPS}$ ,  $V_{OUT}$  retains the status.

\*3.  $B_{HYSS}$ : Hysteresis width

$B_{HYSS}$  is the difference of magnetic flux density between  $B_{OPS}$  and  $B_{RPS}$ .

**Remark** The unit of magnetic flux density mT can be converted by using the formula  $1 \text{ mT} = 10 \text{ Gauss}$ .

■ Test Circuits



\*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 4 Test Circuit 1

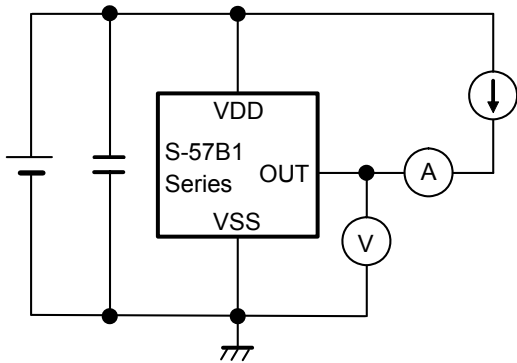


Figure 5 Test Circuit 2

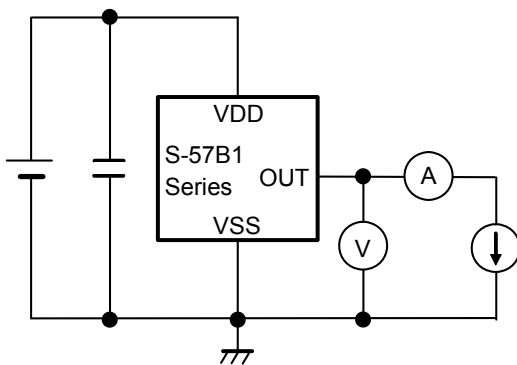


Figure 6 Test Circuit 3

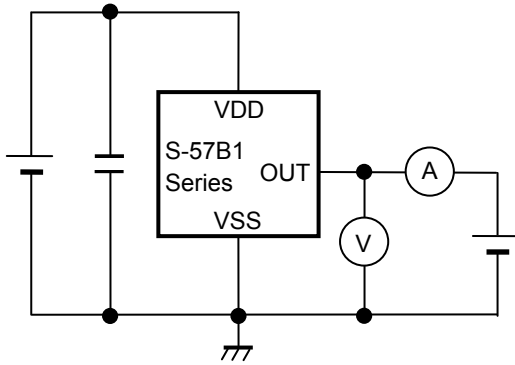
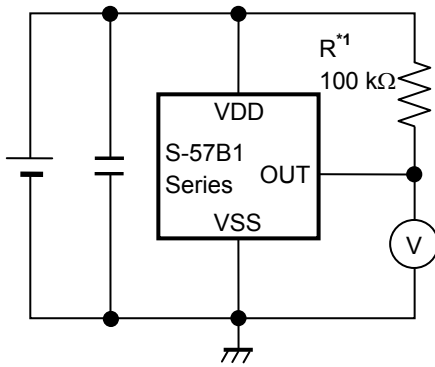


Figure 7 Test Circuit 4

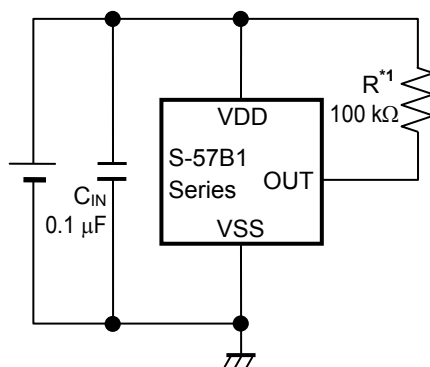


\*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 8 Test Circuit 5



## ■ Standard Circuit



\*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 9

**Caution** The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

## ■ Operation

### 1. Direction of applied magnetic flux

This IC detects the magnetic flux density which is vertical to the marking surface.  
The output voltage ( $V_{OUT}$ ) is inverted when the S pole is moved closer to the marking surface.  
**Figure 10** shows the direction in which magnetic flux is being applied.

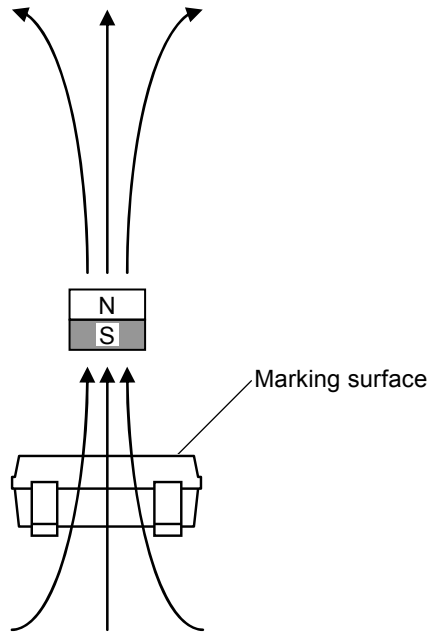


Figure 10

### 2. Position of Hall sensor

**Figure 11** shows the position of Hall sensor.  
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.  
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

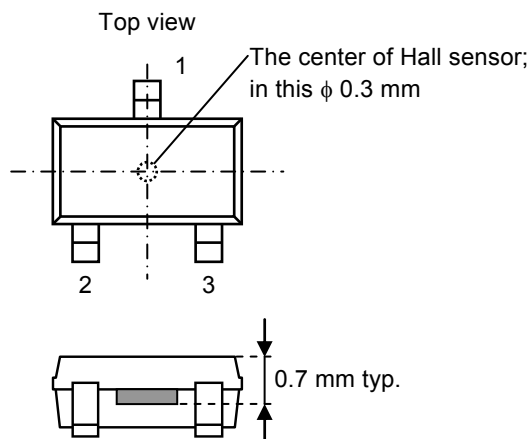


Figure 11

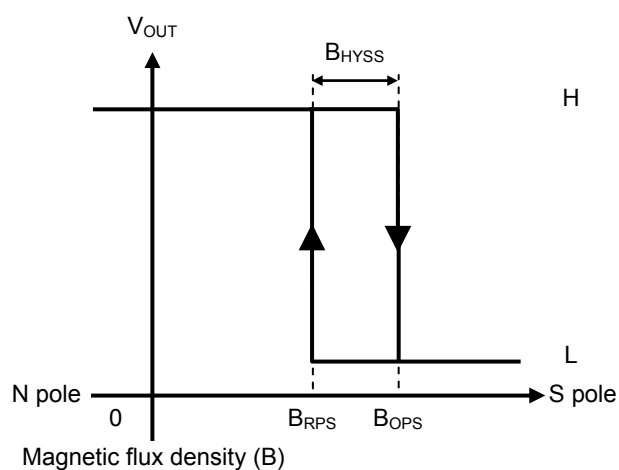
### 3. Basic operation

This IC changes the output voltage level ( $V_{OUT}$ ) according to the level of the magnetic flux density (S pole) applied by a magnet.

The following explains the operation when the magnetism detection logic is active "L".

When the magnetic flux density vertical to the marking surface exceeds the operation point ( $B_{OPS}$ ) after the south pole of a magnet is moved closer to the marking surface of this IC,  $V_{OUT}$  changes from "H" to "L". When the south pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than the release point ( $B_{RPS}$ ),  $V_{OUT}$  changes from "L" to "H".

**Figure 12** shows the relationship between the magnetic flux density and  $V_{OUT}$ .



**Figure 12**

4. Timing chart

Figure 13 shows the operation timing of this IC. This IC always operates on awake mode.  $V_{OUT}$  is refreshed to the level according to the result of the magnetic flux density judgment for each period the operating cycle ( $t_{CYCLE}$ ) elapses.

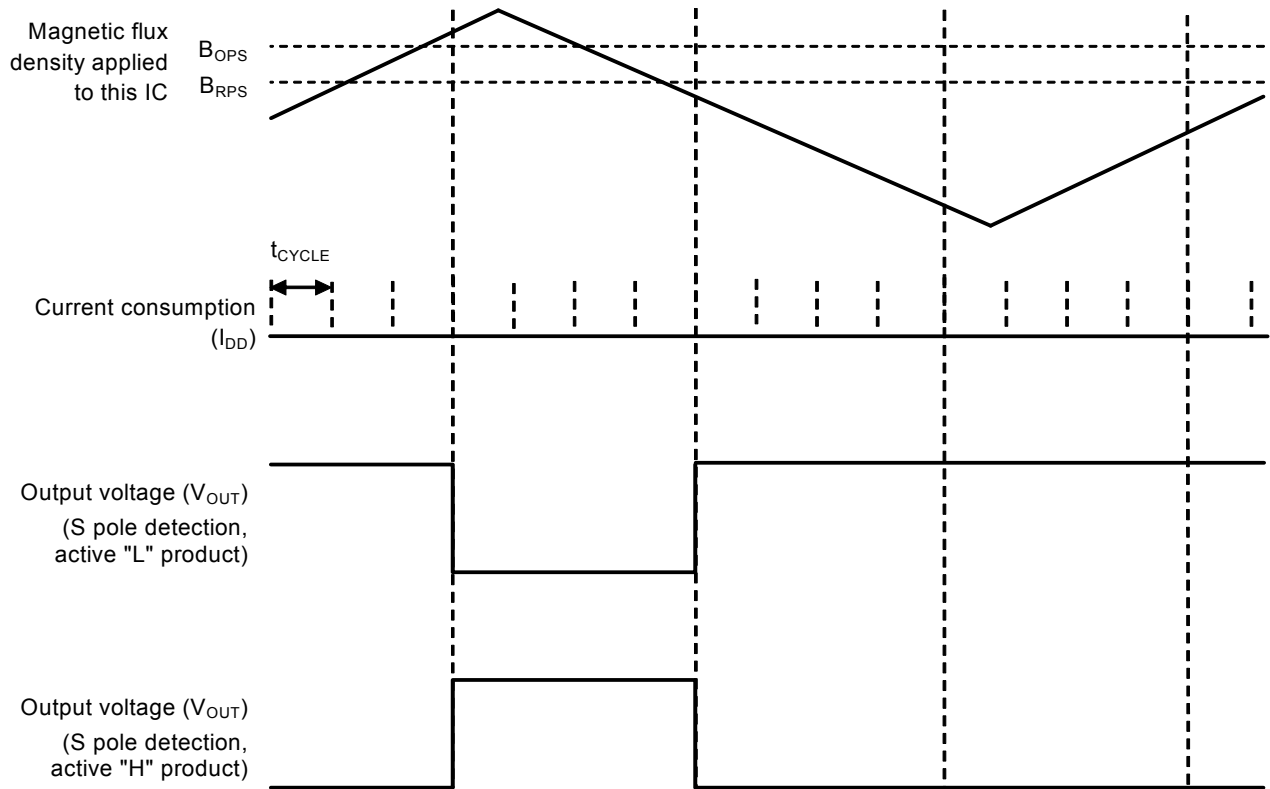


Figure 13

5. Start-up response

Figure 14, Figure15 show the start-up response of this IC. After rising of  $V_{DD}$  for this IC,  $V_{OUT}$  changes to the level according to the result of the magnetic flux density judgment after  $80 \mu\text{s}$  typ. is elapsed.

Thereafter  $V_{OUT}$  is refreshed to the level according to the result of the magnetic flux density judgment for each period the  $t_{\text{CYCLE}}$  elapses.

5.1  $B > B_{\text{OPS}}$

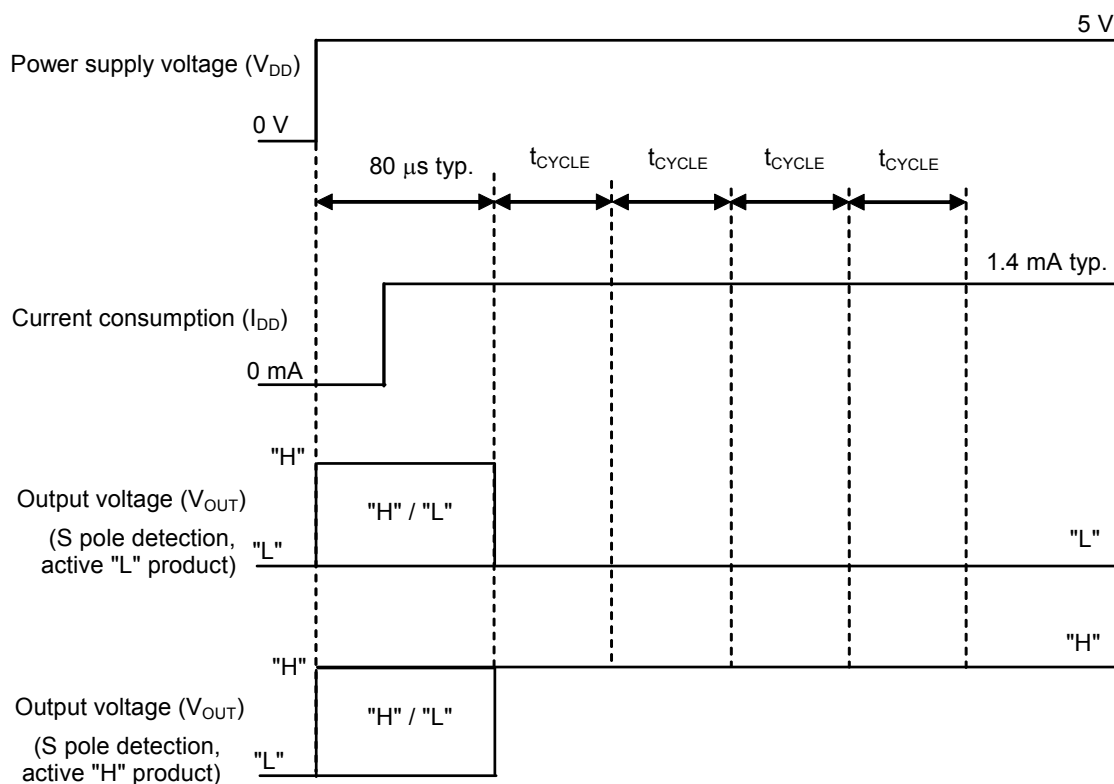


Figure 14

5.2  $B < B_{RPS}$

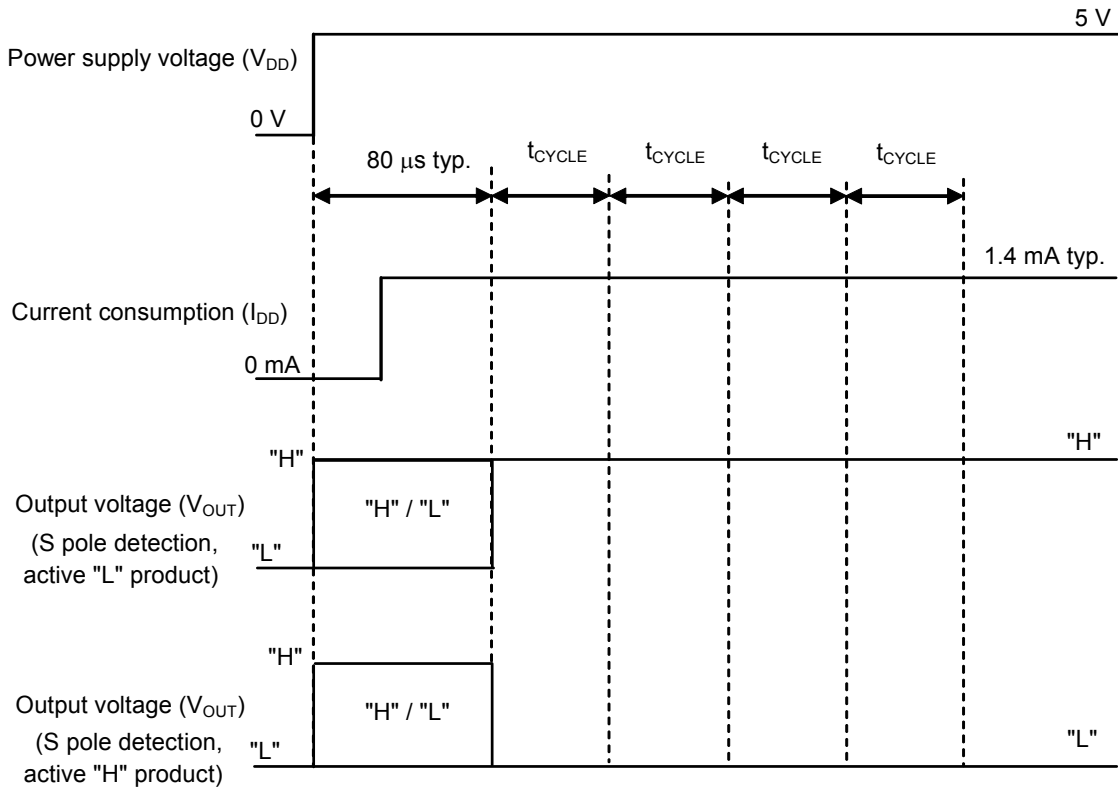


Figure 15

## ■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by through-type current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Large stress on this IC may affect on the magnetic characteristics. Avoid large stress which is caused by bend and distortion during mounting the IC on a board or handle after mounting.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Thermal Characteristics

1. SOT-23-3

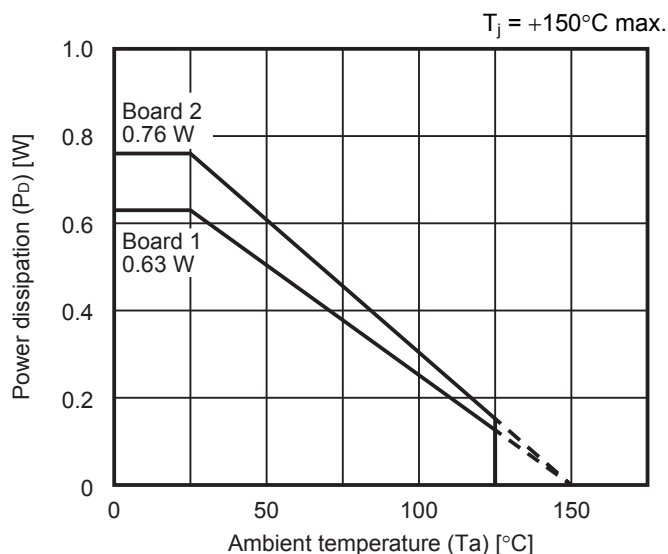


Figure 16 Power Dissipation of Package (When Mounted on Board)

1.1 Board 1\*1

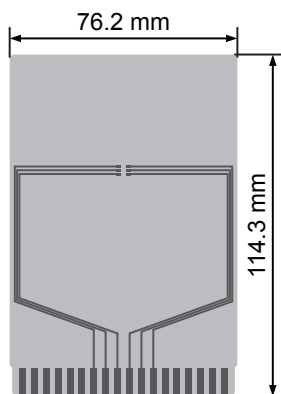


Figure 17

Table 10

Item	Specification
Thermal resistance value ( $\theta_{ja}$ )	200°C/W
Size	114.3 mm × 76.2 mm × t1.6 mm
Material	FR-4
Number of copper foil layer	2
Copper foil layer	1 Land pattern and wiring for testing: t0.070 mm
	2 -
	3 -
	4 74.2 mm × 74.2 mm × t0.070 mm
Thermal via	-

1.2 Board 2\*1

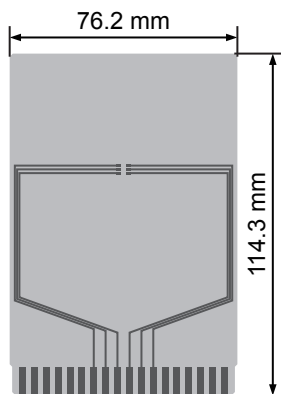


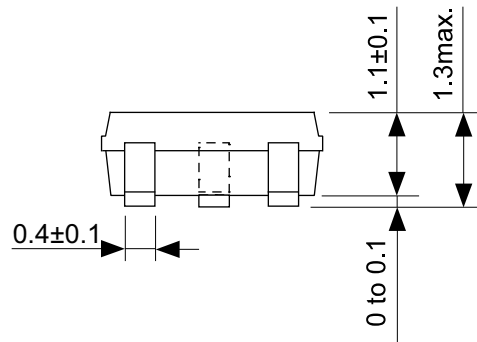
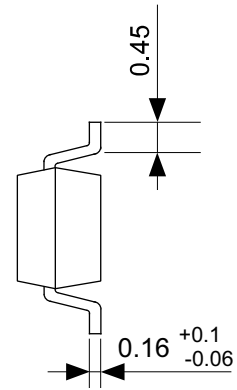
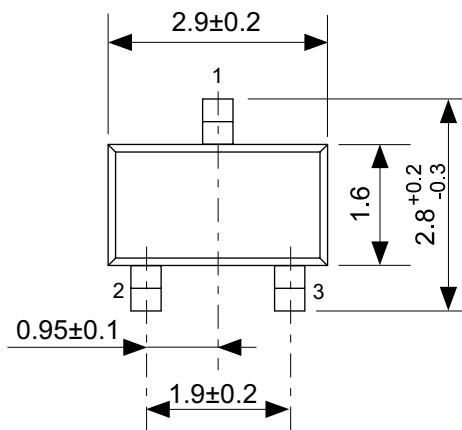
Figure 18

Table 11

Item	Specification
Thermal resistance value ( $\theta_{ja}$ )	165°C/W
Size	114.3 mm × 76.2 mm × t1.6 mm
Material	FR-4
Number of copper foil layer	4
Copper foil layer	1 Land pattern and wiring for testing: t0.070 mm
	2 74.2 mm × 74.2 mm × t0.035 mm
	3 74.2 mm × 74.2 mm × t0.035 mm
	4 74.2 mm × 74.2 mm × t0.070 mm
Thermal via	-

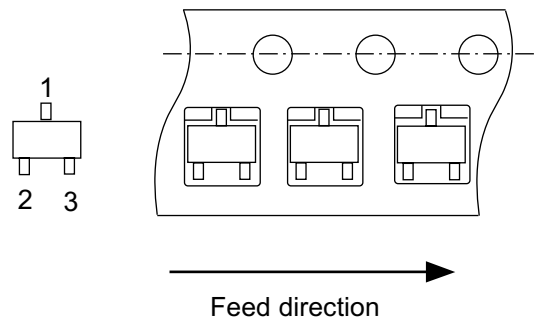
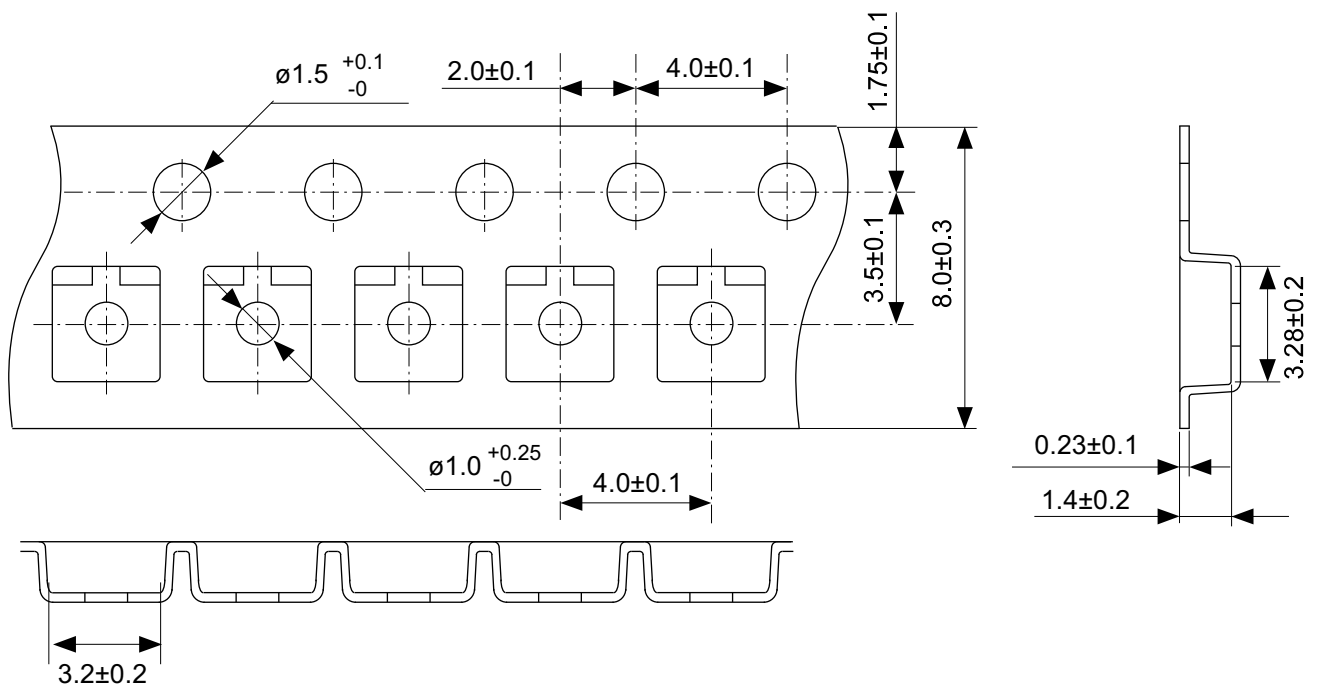
\*1. The board is same in SOT-23-3, SOT-23-5 and SOT-23-6.





No. MP003-C-P-SD-1.1

TITLE	SOT233-C-PKG Dimensions
No.	MP003-C-P-SD-1.1
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



No. MP003-C-C-SD-2.0

TITLE	SOT233-C-Carrier Tape
No.	MP003-C-C-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



Enlarged drawing in the central part



No. MP003-Z-R-SD-1.0

TITLE	SOT233-C-Reel		
No.	MP003-Z-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
<b>ABLIC Inc.</b>			

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