

ZGM130S Z-Wave 700 SiP Module Data Sheet



The Silicon Labs Z-Wave 700 SiP Module, ZGM130S, is a fully integrated Z-Wave module, enabling rapid development of Z-Wave solutions.

It is an ideal solution for energy-friendly smart home control applications such as motion sensors, door/window sensors, access control, appliance control, building automation, energy management, lighting, and security networks in the “Internet of Things”.

Built with low-power Gecko technology, which includes innovative low energy techniques, fast wake-up times and energy saving modes, the ZGM130S reduces overall power consumption and maximizes battery life.

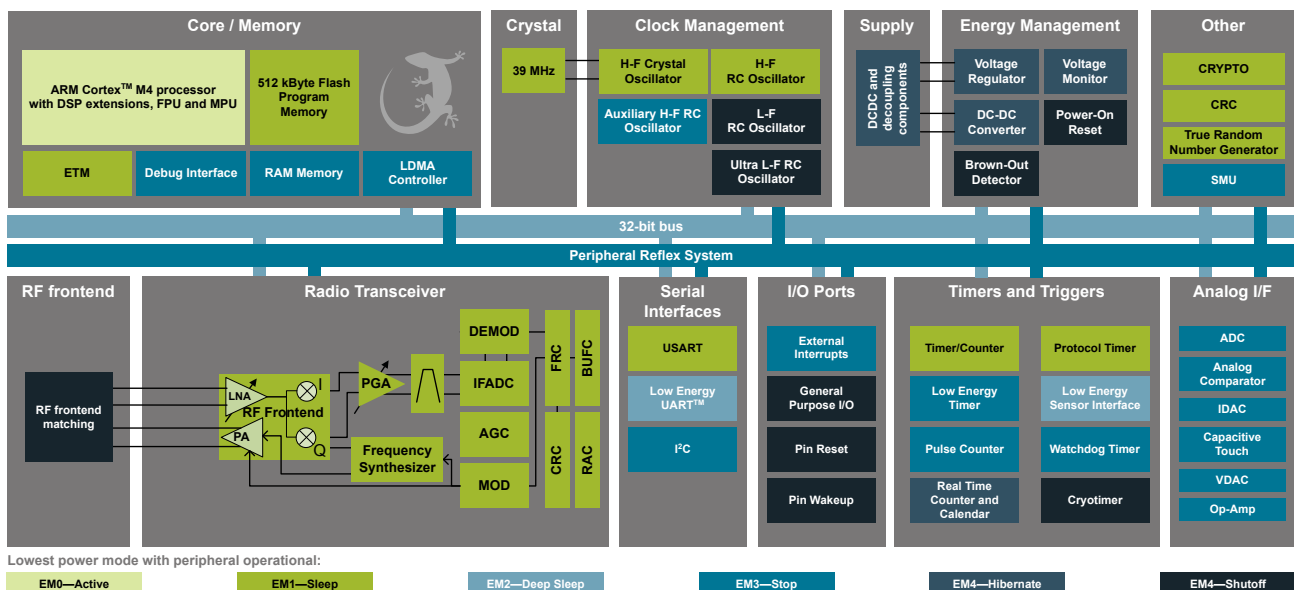
The module contains a native security stack and a comprehensive set of hardware peripherals usable for advanced device functionality, and offers 64 kB of flash memory for OEM applications.

Z-Wave 700 ZGM130S modules can be used in a wide variety of applications:

- Smart Home
- Security
- Lighting
- Health and Wellness
- Metering
- Building Automation

KEY FEATURES

- TX power up to 14 dBm
- RX sensitivity @ 100 kbps: -103.9 dBm
- Range: up to 1 mile
- 9.8 mA RX current at 100 kbps, GFSK, 868 MHz
- 13.3 mA TX current at 0 dBm output power at 908 MHz
- 0.8 μ A EM4H current (128 Byte RAM retention and RTCC running from LFRCO)
- 32-bit ARM® Cortex®-M4 core at 39 MHz
- Flash memory: 512 kB (64 kB Application)
- RAM: 64 kB (8 kB Application)
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated DC-DC Converter
- Robust peripheral set and up to 32 GPIO
- External SAW filter optional



1. Feature List

The ZGM130S highlighted features are listed below.

- **Low Power Wireless System-on-Chip.**
 - High Performance 32-bit, 39 MHz ARM Cortex[®]-M4 with DSP instruction and floating-point unit for efficient signal processing
 - Embedded Trace Macrocell (ETM) for advanced debugging
 - 512 kB flash program memory (64 kB available for user applications)
 - 64 kB RAM data memory (8kB available for user applications)
 - TX power up to 14 dBm
 - Supports optional external SAW filter
- **Low Energy Consumption**
 - 9.8 mA RX current at 100 kbps, GFSK, 868 MHz
 - 40.1 mA TX current at 14 dBm output power at 912 MHz
 - 40.7 mA TX current at 13 dBm output power at 868 MHz
 - 13.3 mA TX current at 0 dBm output power at 908 MHz
 - 69 μ A/MHz in Active Mode (EM0)
 - 0.8 μ A EM4 current (128 Byte RAM retention and RTCC running from LFRCO)
- **High Receiver Performance**
 - -97.9 dBm sensitivity at 100 kbit/s GFSK, 868 MHz
 - -97.5 dBm sensitivity at 100 kbit/s GFSK, 915 MHz
 - -103.9 dBm sensitivity at 100 kbit/s DSSS O-QPSK, 912 MHz
- **Supported Protocols:**
 - Z-Wave
 - Z-Wave Long Range
- **Support for Internet Security**
 - General Purpose CRC
 - True Random Number Generator (TRNG)
 - 2 \times Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide selection of MCU peripherals**
 - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
 - 2 \times Analog Comparator (ACMP)
 - 2 \times Digital to Analog Converter (VDAC)
 - 3 \times Operational Amplifier (Opamp)
 - Digital to Analog Current Converter (IDAC)
 - Low-Energy Sensor Interface (LESENSE)
 - Multi-channel Capacitive Sense Interface (CSEN)
 - 32 pins connected to analog channels (APORT) shared between analog peripherals
 - 32 General Purpose I/O pins with output state retention and asynchronous interrupts
 - 8 Channel DMA Controller
 - 12 Channel Peripheral Reflex System (PRS)
 - 2 \times 16-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
 - 1 \times 32-bit Timer/Counter
 - 3 Compare/Capture/PWM channels
 - 32-bit Real Time Counter and Calendar
 - 16-bit Low Energy Timer for waveform generation
 - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
 - 16-bit Pulse Counter with asynchronous operation
 - 2 \times Watchdog Timer
 - 3 \times Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I²S)
 - Low Energy UART (LEUART[™])
 - 2 \times I²C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
 - 1.8 V to 3.8 V single power supply
 - Integrated DC-DC
 - -40 $^{\circ}$ C to 85 $^{\circ}$ C
- **Dimensions**
 - 9 \times 9 \times 1.21 mm

2. Ordering Information

Table 2.1. Ordering Information

| Ordering Code | Protocol Stack | Max TX Power | Antenna | Flash (kB) | RAM (kB) | GPIO | Carrier |
|-----------------|----------------|--------------|---------|------------|----------|------|-------------|
| ZGM130S037HGN2 | Z-Wave | 14 dBm | RF pin | 512 | 64 | 32 | Tray |
| ZGM130S037HGN2R | Z-Wave | 14 dBm | RF pin | 512 | 64 | 32 | Tape & Reel |

Table of Contents

| | |
|---|----------|
| 1. Feature List | 2 |
| 2. Ordering Information | 3 |
| 3. System Overview | 7 |
| 3.1 Introduction | 7 |
| 3.2 Radio | 7 |
| 3.2.1 Antenna Interface | 7 |
| 3.2.2 RFSENSE | 8 |
| 3.2.3 Packet and State Trace | 8 |
| 3.2.4 Random Number Generator | 8 |
| 3.3 Power | 9 |
| 3.3.1 Energy Management Unit (EMU) | 9 |
| 3.3.2 DC-DC Converter | 9 |
| 3.3.3 Power Domains | 9 |
| 3.4 General Purpose Input/Output (GPIO) | 9 |
| 3.5 Clocking | 9 |
| 3.5.1 Clock Management Unit (CMU) | 9 |
| 3.5.2 Internal Oscillators and Crystals | 10 |
| 3.6 Counters/Timers and PWM | 10 |
| 3.6.1 Timer/Counter (TIMER) | 10 |
| 3.6.2 Wide Timer/Counter (WTIMER) | 10 |
| 3.6.3 Real Time Counter and Calendar (RTCC) | 10 |
| 3.6.4 Low Energy Timer (LETIMER) | 10 |
| 3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER) | 10 |
| 3.6.6 Pulse Counter (PCNT) | 11 |
| 3.6.7 Watchdog Timer (WDOG) | 11 |
| 3.7 Communications and Other Digital Peripherals | 11 |
| 3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) | 11 |
| 3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART) | 11 |
| 3.7.3 Inter-Integrated Circuit Interface (I ² C) | 11 |
| 3.7.4 Peripheral Reflex System (PRS) | 11 |
| 3.7.5 Low Energy Sensor Interface (LESENSE) | 11 |
| 3.8 Security Features | 11 |
| 3.8.1 GPCRC (General Purpose Cyclic Redundancy Check) | 11 |
| 3.8.2 Crypto Accelerator (CRYPTO) | 12 |
| 3.8.3 True Random Number Generator (TRNG) | 12 |
| 3.8.4 Security Management Unit (SMU) | 12 |
| 3.9 Analog | 12 |
| 3.9.1 Analog Port (APORT) | 12 |
| 3.9.2 Analog Comparator (ACMP) | 12 |
| 3.9.3 Analog to Digital Converter (ADC) | 12 |
| 3.9.4 Capacitive Sense (CSEN) | 12 |
| 3.9.5 Digital to Analog Current Converter (IDAC) | 13 |

| | | |
|-----------|---|-----------|
| 3.9.6 | Digital to Analog Converter (VDAC) | .13 |
| 3.9.7 | Operational Amplifiers | .13 |
| 3.10 | Reset Management Unit (RMU) | .13 |
| 3.11 | Core and Memory | .13 |
| 3.11.1 | Processor Core | .13 |
| 3.11.2 | Memory System Controller (MSC) | .13 |
| 3.11.3 | Linked Direct Memory Access Controller (LDMA) | .13 |
| 3.12 | Memory Map | .14 |
| 3.13 | Configuration Summary | .15 |
| 4. | Electrical Specifications | 16 |
| 4.1 | Electrical Characteristics | .16 |
| 4.1.1 | Absolute Maximum Ratings | .16 |
| 4.1.2 | Operating Conditions | .17 |
| 4.1.3 | DC-DC Converter | .18 |
| 4.1.4 | Current Consumption | .20 |
| 4.1.5 | Wake Up Times | .23 |
| 4.1.6 | Brown Out Detector (BOD) | .23 |
| 4.1.7 | Frequency Synthesizer | .24 |
| 4.1.8 | Sub-GHz RF Transceiver Characteristics | .25 |
| 4.1.9 | Oscillators | .33 |
| 4.1.10 | Flash Memory Characteristics | .35 |
| 4.1.11 | General-Purpose I/O (GPIO) | .36 |
| 4.1.12 | Voltage Monitor (VMON) | .38 |
| 4.1.13 | Analog to Digital Converter (ADC) | .39 |
| 4.1.14 | Analog Comparator (ACMP) | .41 |
| 4.1.15 | Digital to Analog Converter (VDAC) | .44 |
| 4.1.16 | Current Digital to Analog Converter (IDAC) | .47 |
| 4.1.17 | Capacitive Sense (CSEN) | .49 |
| 4.1.18 | Operational Amplifier (OPAMP) | .51 |
| 4.1.19 | Pulse Counter (PCNT) | .54 |
| 4.1.20 | Analog Port (APORT) | .54 |
| 4.1.21 | I2C | .55 |
| 4.1.22 | USART SPI Master Timing | .58 |
| 4.1.23 | USART SPI Slave Timing | .59 |
| 4.2 | Typical Performance Curves | .59 |
| 4.2.1 | Zwave Radio | .60 |
| 5. | Typical Connection Diagrams | 61 |
| 5.1 | Typical ZGM130S Connections | .61 |
| 6. | Pin Definitions | 62 |
| 6.1 | ZGM130S Device Pinout | .62 |
| 6.2 | GPIO Functionality Table | .65 |
| 6.3 | Alternate Functionality Overview | .93 |
| 6.4 | Analog Port (APORT) Client Maps | .105 |

- 7. LGA64 Package Specifications. 114**
 - 7.1 LGA64 Package Dimensions 115
 - 7.2 LGA64 PCB Land Pattern 117
 - 7.3 LGA64 Package Marking 118
- 8. Certifications 119**
- 9. Revision History 120**

3. System Overview

3.1 Introduction

The ZGM130S product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application, as well as other system where ultra-small size, reliable high performance RF, low-power consumption and easy application development are key requirements. This section gives a short introduction to the full radio and MCU system.

Note: The hardware functions available to application code are strictly affected by the services enabled in the Z-Wave protocol stack and the version of the stack that is used. The software release note (SRN) for the used Z-Wave protocol version should be consulted to determine whether a specific hardware block is made available by the stack through the Z-Wave API for end-application use.

A detailed block diagram of the ZGM130S module is shown in the figure below.

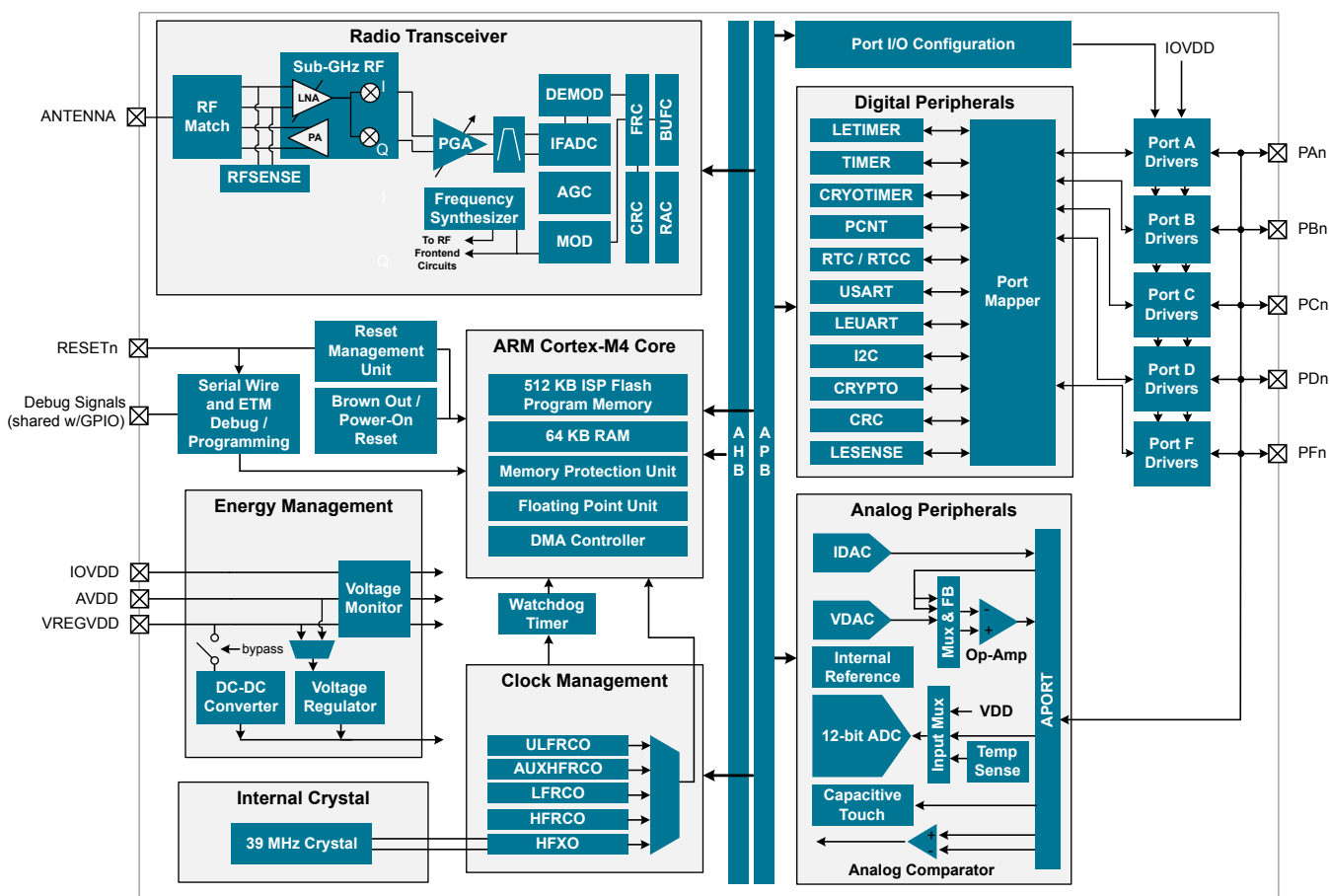


Figure 3.1. ZGM130S Block Diagram

3.2 Radio

The ZGM130S features a radio transceiver supporting Z-Wave protocol.

3.2.1 Antenna Interface

The antenna interface consists of a single pin, connected to internal balun and matching network.

3.2.2 RFSENSE

The RFSENSE block generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.3 Packet and State Trace

The ZGM130S Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.4 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The ZGM130S has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The dc-dc buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the dc-dc converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The dc-dc converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the dc-dc input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3.3 Power Domains

The ZGM130S has two peripheral power domains for operation in EM2 and EM3. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.1. Peripheral Power Subdomains

| Peripheral Power Domain 1 | Peripheral Power Domain 2 |
|---------------------------|---------------------------|
| ACMP0 | ACMP1 |
| PCNT0 | CSEN |
| ADC0 | VDAC0 |
| LETIMER0 | LEUART0 |
| LESENSE | I2C0 |
| APOINT | I2C1 |
| - | IDAC |

3.4 General Purpose Input/Output (GPIO)

ZGM130S has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the ZGM130S. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal Oscillators and Crystals

The ZGM130S fully integrates several oscillator sources and a high frequency crystal.

- The high-frequency crystal oscillator (HFXO) and integrated 39 MHz crystal provide a precise timing reference for the MCU and radio.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz RC oscillator (LFRCO) or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The peripheral may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I²C)

The I²C interface enables communication between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C peripheral allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function supporting a fully-programmable 16-bit polynomial.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO1 block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

3.8.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Capacitive Sense (CSEN)

The CSEN peripheral is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN peripheral uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The peripheral can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.9.5 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC peripheral or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the ZGM130S. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 512 kB flash program memory
- Up to 64 kB RAM data memory
- Configuration and event handling of all peripherals
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The ZGM130S memory map is shown in the figures below. Note that 64 kB of flash in code space is available for user code. The remainder of the code flash area is reserved for the software stack.

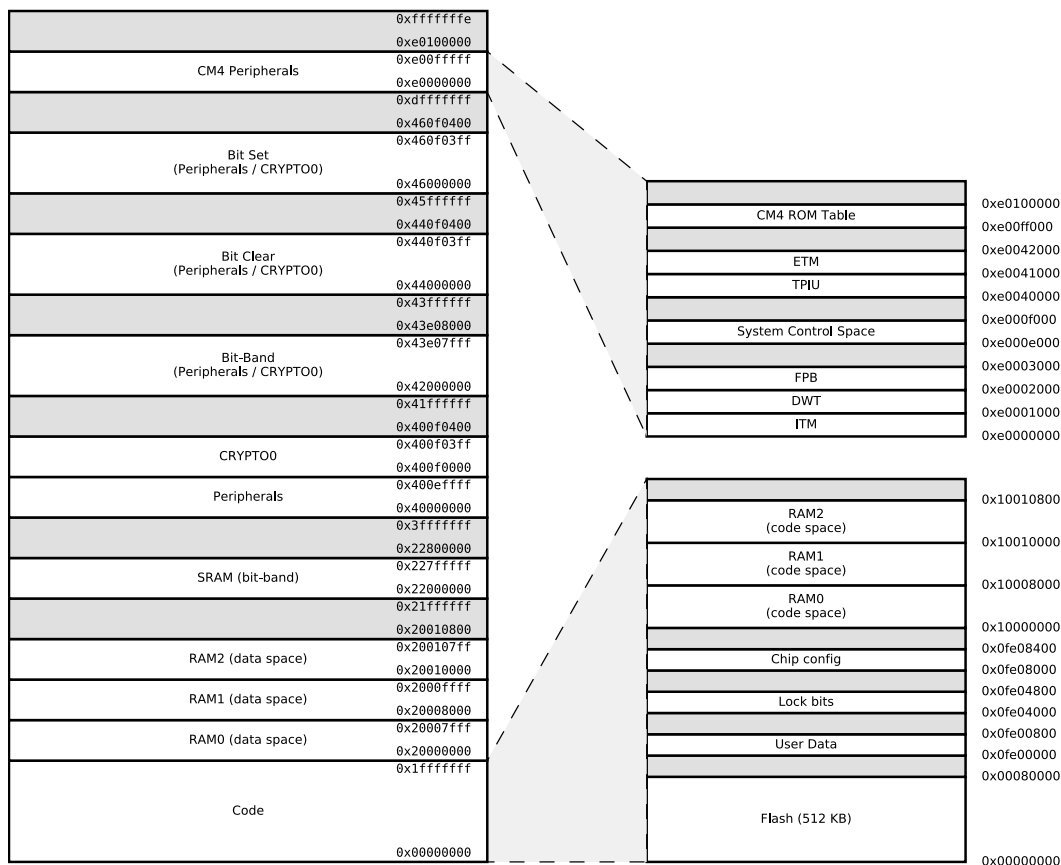


Figure 3.2. ZGM130S Memory Map — Core Peripherals and Code Space

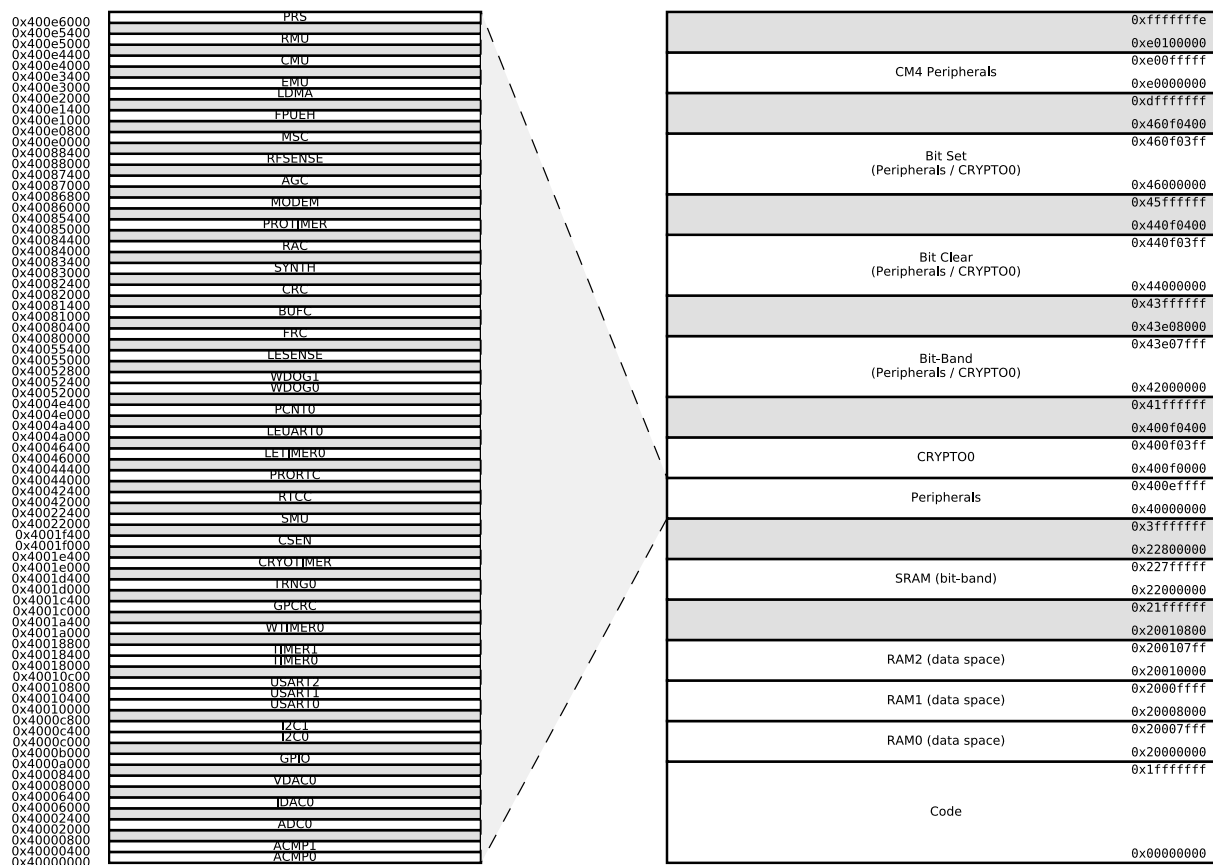


Figure 3.3. ZGM130S Memory Map — Peripherals

3.13 Configuration Summary

The features of the ZGM130S are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining peripherals support full configuration.

Table 3.2. Configuration Summary

| Peripheral | Configuration | Pin Connections |
|------------|----------------------------|---------------------------------|
| USART0 | IrDA SmartCard | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | I ² S SmartCard | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | IrDA SmartCard | US2_TX, US2_RX, US2_CLK, US2_CS |
| TIMER0 | with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | - | TIM1_CC[3:0] |
| WTIMER0 | with DTI | WTIM0_CC[2:0], WTIM0_CDTI[2:0] |

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25\text{ }^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a $50\ \Omega$ antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|-----------------|--|------|-----|--------------------------|--------------------|
| Storage temperature range | T_{STG} | | -40 | — | 85 | $^{\circ}\text{C}$ |
| Voltage on any supply pin | V_{DDMAX} | | -0.3 | — | 3.8 | V |
| Voltage ramp rate on any supply pin | $V_{DDRAMPMAX}$ | | — | — | 1 | V / μs |
| DC voltage on any GPIO pin | V_{DIGPIN} | 5V tolerant GPIO pins ^{1 2 3} | -0.3 | — | Min of 5.25 and IOVDD +2 | V |
| | | Standard GPIO pins | -0.3 | — | IOVDD+0.3 | V |
| Total current into supply pins | I_{VDDMAX} | Source | — | — | 200 | mA |
| Total current into VSS ground lines | I_{VSSMAX} | Sink | — | — | 200 | mA |
| Current per I/O pin | I_{IOMAX} | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | $I_{IOALLMAX}$ | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |
| Junction temperature | T_J | | -40 | — | 105 | $^{\circ}\text{C}$ |

Note:

1. When a GPIO pin is routed to the analog block through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD = AVDD
- IOVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|-----------------------------|------|-----|----------------------|------|
| Operating ambient temperature range | T _A | -G temperature grade | -40 | 25 | 85 | °C |
| AVDD supply voltage ¹ | V _{AVDD} | | 1.8 | 3.3 | 3.8 | V |
| VREGVDD operating supply voltage ^{1 2} | V _{VREGVDD} | DCDC in regulation | 2.4 | 3.3 | 3.8 | V |
| | | DCDC in bypass, 50mA load | 1.8 | 3.3 | 3.8 | V |
| VREGVDD current | I _{VREGVDD} | DCDC in bypass, T ≤ 85 °C | — | — | 200 | mA |
| IOVDD operating supply voltage | V _{IOVDD} | All IOVDD pins ³ | 1.62 | — | V _{VREGVDD} | V |
| HFCORECLK frequency | f _{CORE} | VSCALE2, MODE = WS1 | — | — | 39 | MHz |
| HFCLK frequency | f _{HFCLK} | VSCALE2 | — | — | 39 | MHz |

Note:

1. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
2. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as V_{DVDD_min} + I_{LOAD} * R_{BYP_max}.
3. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.

4.1.3 DC-DC Converter

Test conditions: $V_{DCDC_I}=3.3\text{ V}$, $V_{DCDC_O}=1.8\text{ V}$, $I_{DCDC_LOAD}=50\text{ mA}$, Heavy Drive configuration, $F_{DCDC_LN}=7\text{ MHz}$, unless otherwise indicated.

Table 4.3. DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------|---|------|-----|--------------------|------|
| Input voltage range | V_{DCDC_I} | Bypass mode, $I_{DCDC_LOAD} = 50\text{ mA}$ | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | Low noise (LN) mode, 1.8 V output, $I_{DCDC_LOAD} = 100\text{ mA}$, or Low power (LP) mode, 1.8 V output, $I_{DCDC_LOAD} = 10\text{ mA}$ | 2.4 | — | $V_{VREGVDD_MAX}$ | V |
| Output voltage programmable range ¹ | V_{DCDC_O} | | 1.8 | — | $V_{VREGVDD}$ | V |
| Regulation DC accuracy | ACC_{DC} | Low Noise (LN) mode, 1.8 V target output | 1.7 | — | 1.9 | V |
| Regulation window ² | WIN_{REG} | Low Power (LP) mode, $LPCMPBIASEM_{xx^3} = 0$, 1.8 V target output, $I_{DCDC_LOAD} \leq 75\text{ }\mu\text{A}$ | 1.63 | — | 2.2 | V |
| | | Low Power (LP) mode, $LPCMPBIASEM_{xx^3} = 3$, 1.8 V target output, $I_{DCDC_LOAD} \leq 10\text{ mA}$ | 1.63 | — | 2.1 | V |
| Steady-state output ripple | V_R | Radio disabled | — | 3 | — | mVpp |
| Output voltage under/overshoot | V_{OV} | CCM Mode ($LNFORCECCM^3 = 1$), Load changes between 0 mA and 100 mA | — | 25 | 60 | mV |
| | | DCM Mode ($LNFORCECCM^3 = 0$), Load changes between 0 mA and 10 mA | — | 45 | 90 | mV |
| | | Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode | — | 200 | — | mV |
| | | Undershoot during BYP/LP to LN CCM ($LNFORCECCM^3 = 1$) mode transitions compared to DC level in LN mode | — | 40 | — | mV |
| | | Undershoot during BYP/LP to LN DCM ($LNFORCECCM^3 = 0$) mode transitions compared to DC level in LN mode | — | 100 | — | mV |
| DC line regulation | V_{REG} | Input changes between $V_{VREGVDD_MAX}$ and 2.4 V | — | 0.1 | — | % |
| DC load regulation | I_{REG} | Load changes between 0 mA and 100 mA in CCM mode | — | 0.1 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|-----------------------|---|-----|-----|-----|------|
| Max load current | I _{LOAD_MAX} | Low noise (LN) mode, Medium or Heavy Drive ⁴ | — | — | 80 | mA |
| | | Low noise (LN) mode, Light Drive ⁴ | — | — | 50 | mA |
| | | Low power (LP) mode, LPCMPBIASEMxx ³ = 0 | — | — | 75 | μA |
| | | Low power (LP) mode, LPCMPBIASEMxx ³ = 3 | — | — | 10 | mA |

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VREGVDD}.
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, 1V8 = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.4. Current Consumption 3.3 V using DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|--|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹ | I _{ACTIVE_DCM} | 39 MHz crystal, CPU running while loop from flash ² | — | 87 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 69 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 70 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 82 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 76 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 615 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode ³ | I _{ACTIVE_CCM} | 39 MHz crystal, CPU running while loop from flash ² | — | 97 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 80 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 81 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 92 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 94 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1145 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ³ | I _{ACTIVE_CCM_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 101 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1124 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹ | I _{EM1_DCM} | 39 MHz crystal ² | — | 56 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 39 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 46 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 588 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ¹ | I _{EM1_DCM_VS} | 19 MHz HFRCO | — | 50 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 572 | — | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|---|-----|------|-----|------|
| Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode ⁴ | I _{EM2_VS} | Full 64 kB RAM retention and RTCC running from LFRCO | — | 1.5 | — | μA |
| | | 1 bank RAM retention and RTCC running from LFRCO ⁵ | — | 1.3 | — | μA |
| Current consumption in EM3 mode, with voltage scaling enabled | I _{EM3_VS} | Full 64 kB RAM retention and CRYOTIMER running from ULFR-CO | — | 1.14 | — | μA |
| Current consumption in EM4H mode, with voltage scaling enabled | I _{EM4H_VS} | 128 byte RAM retention, RTCC running from LFRCO | — | 0.8 | — | μA |

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
2. CMU_HFXOCTRL_LOWPOWER=0.
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
4. DCDC Low Power Mode = Medium Drive, LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.4.2 Current Consumption Using Radio 3.3 V with DC-DC

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V. DC-DC on. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.5. Current Consumption Using Radio 3.3 V with DC-DC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|--|-----|------|------|------|
| Current consumption in receive mode, active packet reception (MCU in EM1 @ 39 MHz, peripheral clocks disabled) | I _{RX_ACTIVE} | 40 kbit/s, 2FSK, F=868.4 MHz | — | 9.6 | 10 | mA |
| | | 9.6 kbit/s, Manchester, 2FSK, F=868.42 MHz | — | 9.6 | 10 | mA |
| | | 100 kbit/s, 2GFSK, F=916.0 MHz | — | 9.9 | 10.3 | mA |
| | | 40 kbit/s, 2FSK, F=908.4 MHz | — | 9.7 | 10.1 | mA |
| | | 9.6 kbit/s, Manchester, 2FSK, F=908.42 MHz | — | 9.5 | 9.9 | mA |
| | | 100 kbit/s, 2GFSK, F=869.85 MHz | — | 9.8 | 10.3 | mA |
| | | 100 kbit/s, O-QPSK, F=912 MHz | — | 10.9 | — | mA |
| Current consumption in receive mode, listening for packet (MCU in EM1 @ 39 MHz, peripheral clocks disabled) | I _{RX_LISTEN} | 100 kbit/s, 2GFSK, F=869.85 MHz | — | 9.9 | 10.3 | mA |
| | | 40 kbit/s, 2FSK, F=868.4 MHz | — | 9.7 | 10.1 | mA |
| | | 9.6 kbit/s, Manchester, 2FSK, F=868.42 MHz | — | 9.6 | 10 | mA |
| | | 100 kbit/s, 2GFSK, F=916.0 MHz | — | 9.9 | 10.4 | mA |
| | | 40 kbit/s, 2FSK, F=908.40 MHz | — | 9.7 | 10.1 | mA |
| | | 9.6 kbit/s, Manchester, 2FSK, F=908.42 MHz | — | 9.5 | 9.9 | mA |
| | | 100 kbit/s, O-QPSK, F=912 MHz | — | 10.9 | — | mA |
| Current consumption in transmit mode (MCU in EM1 @ 39 MHz, peripheral clocks disabled) | I _{TX} | F=868.4 MHz, CW, 13 dBm output power | — | 40.7 | — | mA |
| | | F=908.4 MHz, CW, 4 dBm output power | — | 17.9 | — | mA |
| | | F=908.4 MHz, CW, 0 dBm output power | — | 13.3 | — | mA |
| | | F=912 MHz, CW, 14 dBm output power | — | 40.1 | — | mA |

4.1.5 Wake Up Times

Table 4.6. Wake Up Times

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|---|-----|------|-----|------------|
| Wake up time from EM1 | t _{EM1_WU} | | — | 3 | — | AHB Clocks |
| Wake up from EM2 | t _{EM2_WU} | Code execution from flash | — | 10.9 | — | μs |
| | | Code execution from RAM | — | 3.8 | — | μs |
| Wake up from EM3 | t _{EM3_WU} | Code execution from flash | — | 10.9 | — | μs |
| | | Code execution from RAM | — | 3.8 | — | μs |
| Wake up from EM4H ¹ | t _{EM4H_WU} | Executing from flash | — | 90 | — | μs |
| Wake up from EM4S ¹ | t _{EM4S_WU} | Executing from flash | — | 300 | — | μs |
| Time from release of reset source to first instruction execution | t _{RESET} | Soft Pin Reset released | — | 51 | — | μs |
| | | Any other reset released | — | 358 | — | μs |
| Power mode scaling time | t _{SCALE} | VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{2 3} | — | 31.8 | — | μs |
| | | VSCALE2 to VSCALE0, HFCLK = 19 MHz ⁴ | — | 4.3 | — | μs |

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.
3. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/μs for approximately 20 μs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
4. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.

4.1.6 Brown Out Detector (BOD)

Table 4.7. Brown Out Detector (BOD)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------|----------------------------|------------------------------|------|-----|-----|------|
| AVDD BOD threshold | V _{AVDDBOD} | AVDD rising | — | — | 1.8 | V |
| | | AVDD falling (EM0/EM1) | 1.62 | — | — | V |
| | | AVDD falling (EM2/EM3) | 1.53 | — | — | V |
| AVDD BOD hysteresis | V _{AVDDBOD_HYST} | | — | 20 | — | mV |
| AVDD BOD response time | t _{AVDDBOD_DELAY} | Supply drops at 0.1V/μs rate | — | 2.4 | — | μs |
| EM4 BOD threshold | V _{EM4BOD} | AVDD rising | — | — | 1.7 | V |
| | | AVDD falling | 1.45 | — | — | V |
| EM4 BOD hysteresis | V _{EM4BOD_HYST} | | — | 25 | — | mV |
| EM4 BOD response time | t _{EM4BOD_DELAY} | Supply drops at 0.1V/μs rate | — | 300 | — | μs |

4.1.7 Frequency Synthesizer

Table 4.8. Frequency Synthesizer

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|----------------|-----|-----|-----|------|
| RF synthesizer frequency range | f_{RANGE} | 779 - 956 MHz | 779 | — | 956 | MHz |
| LO tuning frequency resolution with 39 MHz crystal | f_{RES} | 779 - 956 MHz | — | — | 24 | Hz |
| Frequency deviation resolution with 39 MHz crystal | df_{RES} | 779 - 956 MHz | — | — | 24 | Hz |
| Maximum frequency deviation with 39 MHz crystal | df_{MAX} | 779 - 956 MHz | — | — | 559 | kHz |

4.1.8 Sub-GHz RF Transceiver Characteristics

4.1.8.1 Sub-GHz RF Transmitter characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V. Crystal frequency = 39 MHz. RF frequency band 915 MHz.

Table 4.9. Sub-GHz RF Transmitter characteristics for 915 MHz Band

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|------|-----|----------|
| RF tuning frequency range | F _{RANGE} | | 902 | — | 930 | MHz |
| Maximum TX Power ¹ | POUT _{MAX} | 4 dBm output power setting | — | 4 | — | dBm |
| Minimum active TX Power | POUT _{MIN} | | — | -30 | — | dBm |
| Output power step size | POUT _{STEP} | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply at POUT _{MAX} | POUT _{VAR_V} | 1.8 V < V _{VREGVDD} < 3.3 V, T = 25 °C | — | 2.72 | — | dB |
| Output power variation vs temperature, peak to peak | POUT _{VAR_T} | -40 to +85 °C | — | 1.79 | — | dB |
| Output power variation vs RF frequency | POUT _{VAR_F} | T = 25 °C, Over specified RF tuning frequency range | — | 1.11 | — | dB |
| Spurious emissions of harmonics at 3 dBm output power, Conducted measurement, 3dBm match, Test Frequency = 908.4 MHz | SPUR _{HARM_FCC_4} | In restricted bands, per FCC Part 15.205 / 15.209 | — | -49 | -42 | dBm |
| | | In non-restricted bands, per FCC Part 15.249 | — | -53 | -20 | dBc |
| Spurious emissions out-of-band at 3 dBm output power, Conducted measurement, 3dBm match, Test Frequency = 908.4 MHz | SPUR _{OOB_FCC_4} | In non-restricted bands, per FCC Part 15.249 | — | -70 | -20 | dBc |
| | | In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209 | — | -58 | -46 | dBm |
| | | In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209 | — | -70 | -56 | dBm |
| | | In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209 | — | -70 | -52 | dBm |
| | | In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209 | — | -66 | -42 | dBm |
| Power spectral density limit | PSD ₄ | PSD per FCC Part 15.249, 9.6Kbps | — | -0.7 | — | dBm/3kHz |
| | | PSD per FCC Part 15.249, 40Kbps | — | 2.3 | — | dBm/3kHz |
| | | PSD per FCC Part 15.249, 100Kbps | — | -4.1 | — | dBm/3kHz |

Note:

1. If a SAW filter is used, the output power is 2 - 3 dBm lower due to insertion loss. Always adjust the output power to match the limits set by the RF regulatory authorities for the region in which the device is used.

4.1.8.2 Sub-GHz RF Transmitter characteristics for 915 MHz Band, +14 dBm

This table is for the O-QPSK PHY only at +14 dBm. Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3V. Crystal frequency = 39 MHz. RF Center frequency 912 MHz.

Table 4.10. Sub-GHz RF Transmitter characteristics for 915 MHz Band, +14 dBm

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------------------------|--|-----|------|-----|----------|
| RF tuning frequency range | F _{RANGE} | | 902 | — | 930 | MHz |
| Maximum TX Power | POUT _{MAX} | 14 dBm output power setting ^{1 2} | — | 13.9 | — | dBm |
| Minimum active TX Power | POUT _{MIN} | | — | -30 | — | dBm |
| Output power step size | POUT _{STEP} | output power > 0 dBm | — | 0.3 | — | dB |
| Output power variation vs supply at POUT _{MAX} | POUT _{VAR_V} | 2.0 V < V _{VREGVDD} < 3.3 V, T = 25 °C ³ | — | 1.9 | — | dB |
| Output power variation vs temperature, peak to peak | POUT _{VAR_T} | -40 to +85 °C | — | 1.1 | — | dB |
| Output power variation vs RF frequency | POUT _{VAR_F} | T = 25 °C, Over specified RF tuning frequency range | — | 0.3 | — | dB |
| Spurious emissions of harmonics at +14 dBm output power, Conducted measurement, +14 dBm match, Test Frequency = 912 MHz | SPUR _{HARM_FCC_14} | In restricted bands, per FCC 47 CFR §15.205 & §15.209 ⁴⁵ | — | -48 | -42 | dBm |
| | | In non-restricted bands, per FCC 47 CFR §15.247 ⁶ | — | -40 | -20 | dBc |
| Spurious emissions out-of-band at +14 dB output power, Conducted measurement, +14 dB match, Test Frequency = 912 MHz | SPUR _{OOB_FCC_14} | In non-restricted bands, per FCC 47 CFR §15.247 ⁶ | — | -66 | -20 | dBc |
| | | In restricted bands (30-88 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5} | — | -58 | -46 | dBm |
| | | In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5} | — | -68 | -56 | dBm |
| | | In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5} | — | -61 | -52 | dBm |
| | | In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5} | — | -61 | -42 | dBm |
| Power spectral density limit | PSD ₁₄ | PSD per FCC Part 15.247, 100 kbps O-QPSK | — | -1.1 | — | dBm/3kHz |
| Error Vector Magnitude, per 802.15.4-2006 | EVM | Signal is 100 kbps DSSS-OQPSK reference packet. Modulated according to 802.15.4-2006 OQPSK-BPSK in the 915 MHz band, with pseudo-random packet data content. POUT = +14 dBm. | — | 5.0 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The 14 dBm match is optimized for best efficiency at 14 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 14 dBm.
3. Due to supply current limitations of the DCDC circuit, POUTmax is only achievable at $V_VREGVDD > 2.0\text{ V}$
4. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
5. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements
6. FCC Title 47 CFR Part 15 Section 15.247 Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz.

4.1.8.3 Sub-GHz RF Receiver Characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V. Crystal frequency = 39 MHz. RF frequency band 915 MHz.

Table 4.11. Sub-GHz RF Receiver Characteristics for 915 MHz Band

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|--------|-----|------|
| Tuning frequency range | F _{RANGE} | | 902 | — | 930 | MHz |
| Max usable input level, 1% FER | SAT _{100K} | Desired is reference 100 kbps GFSK signal ¹ | — | 10 | — | dBm |
| Sensitivity ^{2 3} | SENS | Desired is reference 100 kbps GFSK signal ¹ , 1% FER, frequency = 916 MHz, T ≤ 85 °C | — | -97.5 | — | dBm |
| | | Desired is reference 100 kbps O-QPSK signal ⁴ , 1% FER, frequency = 912 MHz, T ≤ 85 °C | — | -103.9 | — | dBm |
| | | Desired is reference 40 kbps 2FSK signal ⁵ , 1% FER, frequency = 908.4 MHz, T ≤ 85 °C | — | -101.3 | — | dBm |
| | | Desired is reference 9.6 kbps 2FSK signal ⁶ , 1% FER, frequency = 908.42 MHz, T ≤ 85 °C | — | -102.5 | — | dBm |
| Level above which RFSENSE will trigger ⁷ | RFSENSE _{TRIG} | CW at 915 MHz | — | -28.1 | — | dBm |
| Image rejection, Interferer is CW at image frequency | C/I _{IMAGE} | Desired is reference 100 kbps O-QPSK signal ⁴ , 1% FER, frequency = 912 MHz | — | 40.1 | — | dB |
| | | Desired is reference 40 kbps 2FSK signal ⁵ at 3dB above sensitivity level, 1% FER, frequency = 908.4 MHz | — | 36.2 | — | dB |
| | | Desired is 100 kbps GFSK signal ¹ at 3dB above sensitivity level, 1% FER, frequency = 916 MHz | — | 34.7 | — | dB |
| | | Desired is reference 9.6 kbps 2FSK signal ⁶ at 3dB above sensitivity level, 1% FER, frequency = 908.42 MHz | — | 36.1 | — | dB |
| Level below which RFSENSE will not trigger ⁷ | RFSENSE _{THRES} | CW at 915 MHz | — | -50 | — | dBm |
| Blocking selectivity, 1% FER. Desired is 100 kbps GFSK signal ¹ at 3dB above sensitivity level, frequency = 916 MHz | C/I _{BLOCKER_100} | Interferer CW at Desired ± 1 MHz | — | 48.7 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 54.8 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 64.1 | — | dB |
| | | Interferer CW at Desired ± 10 MHz ⁸ | — | 67.7 | — | dB |
| | | Interferer CW at Desired ± 100 MHz ⁸ | — | 78.8 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------------|--|-----|--------|-------|------|
| Blocking selectivity, 1% FER. Desired is 40 kbps 2FSK signal ⁵ at 3dB above sensitivity level, frequency = 908.4 MHz | C/I _{BLOCKER_40} | Interferer CW at Desired ± 1 MHz | — | 53.0 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 58.9 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 71.4 | — | dB |
| | | Interferer CW at Desired ± 10 MHz ⁸ | — | 79.2 | — | dB |
| | | Interferer CW at Desired ± 100 MHz ⁸ | — | 82.8 | — | dB |
| Blocking selectivity, 1% FER. Desired is 9.6 kbps 2FSK signal ⁶ at 3dB above sensitivity level, frequency = 908.42 MHz | C/I _{BLOCKER_9p6} | Interferer CW at Desired ± 1 MHz | — | 54.2 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 62.9 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 72.4 | — | dB |
| | | Interferer CW at Desired ± 10 MHz ⁸ | — | 80.4 | — | dB |
| | | Interferer CW at Desired ± 100 MHz ⁸ | — | 84.0 | — | dB |
| Blocking selectivity, 1% FER. Desired is reference 100 kbps O-QPSK signal ⁴ at -89 dBm level 1% FER, frequency = 912 MHz | C/I _{BLOCKER_OQPSK} | Interferer CW at Desired ± 2 MHz | — | 54.2 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 59.4 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 67.0 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 78.9 | — | dB |
| Intermod selectivity, 1% FER. CW interferers at 400 kHz and 800 kHz offsets | C/I _{IM} | Desired is 100 kbps GFSK signal ¹ at 3dB above sensitivity level, frequency = 916 MHz | — | 31.6 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | RSSI _{MAX} | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | RSSI _{MIN} | | -98 | — | — | dBm |
| RSSI resolution | RSSI _{RES} | Over RSSI _{MIN} to RSSI _{MAX} range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | SPUR _{RX_FCC} | 216-960 MHz | — | -82.25 | -49.2 | dBm |
| | | Above 960 MHz | — | -68.41 | -41.2 | dBm |
| Max spurious emissions during active receive mode, per ARIB STD-T108 Section 3.3 | SPUR _{RX_ARIB} | Below 710 MHz, RBW=100kHz | — | -69.17 | -54 | dBm |
| | | 710-900 MHz, RBW=1MHz | — | -71.76 | -55 | dBm |
| | | 900-915 MHz, RBW=100kHz | — | -72.55 | -55 | dBm |
| | | 915-930 MHz, RBW=100kHz | — | -73.07 | -55 | dBm |
| | | 930-1000 MHz, RBW=100kHz | — | -72.84 | -55 | dBm |
| | | Above 1000 MHz, RBW=1MHz | — | -71.49 | -47 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, $\Delta f = 58$ kHz, NRZ, '0' = $F_{center} + \Delta f/2$, '1' = $F_{center} - \Delta f/2$ | | | | | | |
| 2. Minimum Packet Error Rate floor will be ~0.5% for desired input signal levels between specified datasheet sensitivity level and -10dBm. | | | | | | |
| 3. Minimum Packet Error Rate floor will be ~ 1% for desired input signal levels > -10dBm. | | | | | | |
| 4. Definition of reference signals is 100 kbps O-QPSK, 800 kcps chip rate, 8x spreading factor, 32 bit chip length, 4 bits per symbol | | | | | | |
| 5. Definition of reference signal is 40 kbps 2FSK, $\Delta f = 40$ kHz, NRZ, '0' = $F_{center} + \Delta f/2$, '1' = $F_{center} - \Delta f/2$ | | | | | | |
| 6. Definition of reference signal is 9.6 kbps 2FSK, $\Delta f = 40$ kHz, Manchester, '0' = Transition from ($F_{center} + 20k + \Delta f/2$), '1' = Transition from ($F_{center} + 20k - \Delta f/2$) | | | | | | |
| 7. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range. | | | | | | |
| 8. Minimum Packet Error Rate floor for signals in preseceene of blocker will increase above 1% for blocker levels above -30dBm. | | | | | | |

4.1.8.4 Sub-GHz RF Transmitter characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V. Crystal frequency = 39 MHz. RF frequency band 868 MHz.

Table 4.12. Sub-GHz RF Transmitter characteristics for 868 MHz Band

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|--|-----|-----|-----|------|
| RF tuning frequency range | F_{RANGE} | | 863 | — | 876 | MHz |
| Maximum TX Power ¹ | $POUT_{MAX}$ | 13 dBm output power setting | — | 13 | — | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -30 | — | dBm |
| Output power step size | $POUT_{STEP}$ | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | $1.8\text{ V} < V_{VREGVDD} < 3.3\text{ V}$, T = 25 °C | — | 2.6 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | -40 to +85 °C | — | 1.4 | — | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | T = 25 °C, Over specified RF tuning frequency range | — | 0.5 | — | dB |
| Spurious emissions of harmonics, Conducted measurement, Test Frequency = 868.4 MHz | $SPUR_{HARM_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 | — | -39 | -30 | dBm |
| Spurious emissions out-of-band, Conducted measurement, Test Frequency = 868.4 MHz | $SPUR_{OOB_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) | — | -69 | -54 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz) | — | -70 | -36 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz) | — | -66 | -30 | dBm |

| | | | | | | |
|--|--|--|--|--|--|--|
| Note: | | | | | | |
| 1. If a SAW filter is used, the output power is 2 - 3 dBm lower due to insertion loss. Always adjust the output power to match the limits set by the RF regulatory authorities for the region in which the device is used. | | | | | | |

4.1.8.5 Sub-GHz RF Receiver Characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V. Crystal frequency = 39 MHz. RF frequency band 868 MHz.

Table 4.13. Sub-GHz RF Receiver Characteristics for 868 MHz Band

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|--------|-----|------|
| Tuning frequency range | F _{RANGE} | | 863 | — | 876 | MHz |
| Max usable input level, 1% FER | SAT _{100k} | Desired is reference 100 kbps GFSK signal ¹ | — | 10 | — | dBm |
| Sensitivity ^{2 3} | SENS | Desired is reference 100 kbps GFSK signal ¹ , 1% FER, frequency = 869.85 MHz, T ≤ 85 °C | — | -97.9 | — | dBm |
| | | Desired is reference 40 kbps 2FSK signal ⁴ , 1% FER, frequency = 868.4 MHz, T ≤ 85 °C | — | -101.5 | — | dBm |
| | | Desired is reference 9.6 kbps 2FSK signal ⁵ , 1% FER, frequency = 868.42 MHz, T ≤ 85 °C | — | -102.6 | — | dBm |
| Level above which RFSENSE will trigger ⁶ | RFSENSE _{TRIG} | CW at 868 MHz | — | -28.1 | — | dBm |
| Level below which RFSENSE will not trigger ⁶ | RFSENSE _{THRES} | CW at 868 MHz | — | -50 | — | dBm |
| Image rejection, Interferer is CW at image frequency | C/I _{IMAGE} | Desired is 100kbps GFSK signal ¹ at 3dB above sensitivity level, 1% FER, frequency = 869.85 MHz | — | 33.4 | — | dB |
| | | Desired is reference 40 kbps 2FSK signal ⁴ at 3dB above sensitivity level, 1% FER, frequency = 868.4 MHz | — | 34.5 | — | dB |
| | | Desired is reference 9.6 kbps 2FSK signal ⁵ at 3dB above sensitivity level, 1% FER, frequency = 868.42 MHz | — | 35.3 | — | dB |
| Blocking selectivity, 1% FER. Desired is 100 kbps GFSK signal ¹ at 3 dB above sensitivity level, frequency = 869.85 MHz | C/I _{BLOCKER_100} | Interferer CW at Desired ± 1 MHz | — | 49.6 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 55.6 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 68.1 | — | dB |
| | | Interferer CW at Desired ± 10 MHz ⁷ | — | 75.1 | — | dB |
| | | Interferer CW at Desired ± 100 MHz ⁷ | — | 77.4 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|--------|-----|------|
| Blocking selectivity, 1% FER. Desired is 40 kbps 2FSK signal ⁴ at 3 dB above sensitivity level, frequency = 868.4 MHz | C/I _{BLOCKER_40} | Interferer CW at Desired \pm 1 MHz | — | 53.4 | — | dB |
| | | Interferer CW at Desired \pm 2 MHz | — | 59.8 | — | dB |
| | | Interferer CW at Desired \pm 5 MHz | — | 71.9 | — | dB |
| | | Interferer CW at Desired \pm 10 MHz ⁷ | — | 79.5 | — | dB |
| | | Interferer CW at Desired \pm 100 MHz ⁷ | — | 81.1 | — | dB |
| Blocking selectivity, 1% FER. Desired is 9.6 kbps 2FSK signal ⁵ at 3 dB above sensitivity level, frequency = 868.42 MHz | C/I _{BLOCKER_9p6} | Interferer CW at Desired \pm 1 MHz | — | 54.8 | — | dB |
| | | Interferer CW at Desired \pm 2 MHz | — | 60.7 | — | dB |
| | | Interferer CW at Desired \pm 5 MHz | — | 72.8 | — | dB |
| | | Interferer CW at Desired \pm 10 MHz ⁷ | — | 80.3 | — | dB |
| | | Interferer CW at Desired \pm 100 MHz ⁷ | — | 82.1 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | RSSI _{MAX} | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | RSSI _{MIN} | | -98 | — | — | dBm |
| RSSI resolution | RSSI _{RES} | Over RSSI _{MIN} to RSSI _{MAX} range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode | SPUR _{RX} | 30 MHz to 1 GHz | — | -67.46 | -57 | dBm |
| | | 1 GHz to 12 GHz | — | -69.7 | -47 | dBm |

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, $\Delta f = 58$ kHz, NRZ, '0' = $F_{center} + \Delta f/2$, '1' = $F_{center} - \Delta f/2$
2. Minimum Packet Error Rate floor will be ~0.5% for desired input signal levels between specified datasheet sensitivity level and -10dBm.
3. Minimum Packet Error Rate floor will be ~ 1% for desired input signal levels > -10dBm.
4. Definition of reference signal is 40 kbps 2FSK, $\Delta f = 40$ kHz, NRZ, '0' = $F_{center} + \Delta f/2$, '1' = $F_{center} - \Delta f/2$
5. Definition of reference signal is 9.6 kbps 2FSK, $\Delta f = 40$ kHz, Manchester, '0' = Transition from ($F_{center} + 20k + \Delta f/2$), '1' = Transition from ($F_{center} + 20k - \Delta f/2$)
6. RFSense performance is only valid from 0 to 85 °C. RFSense should be disabled outside this temperature range.
7. Minimum Packet Error Rate floor for signals in presence of blocker will increase above 1% for blocker levels above -30dBm.

4.1.9 Oscillators

4.1.9.1 High-Frequency Crystal Oscillator (HFXO)

Internal crystal = TXC P/N 8Y39072002

Table 4.14. High-Frequency Crystal Oscillator (HFXO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------|------------------------------|---|-----|-----|-----|------|
| Crystal frequency | f_{HFXO} | 39 MHz required for radio transceiver operation | — | 39 | — | MHz |
| Calibrated precision | $\text{PREC}_{\text{HFXO}}$ | | -2 | — | 2 | ppm |
| 5-year aging | $\text{AGING}_{\text{HFXO}}$ | | -3 | — | 3 | ppm |
| Temperature drift | $\text{DRIFT}_{\text{HFXO}}$ | -40 °C to 85 °C | -13 | — | 13 | ppm |

4.1.9.2 Low-Frequency RC Oscillator (LFRCO)

Table 4.15. Low-Frequency RC Oscillator (LFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------|-----------------------------|------|--------|------|------|
| Oscillation frequency | f_{LFRCO} | ENVREF ¹ = 1 | 31.3 | 32.768 | 33.6 | kHz |
| | | ENVREF ¹ = 0 | 31.3 | 32.768 | 33.4 | kHz |
| Startup time | t_{LFRCO} | | — | 500 | — | µs |
| Current consumption ² | I_{LFRCO} | ENVREF = 1 in CMU_LFRCOCTRL | — | 342 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 494 | — | nA |

Note:

1. In CMU_LFRCOCTRL register.
2. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.

4.1.9.3 High-Frequency RC Oscillator (HFRCO)

Table 4.16. High-Frequency RC Oscillator (HFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|-----------------------------|---|-------|-----|-------|---------------|
| Frequency accuracy | $f_{\text{HFRCO_ACC}}$ | At production calibrated frequencies, across supply voltage and temperature | -2.5 | — | 2.5 | % |
| Start-up time | t_{HFRCO} | $f_{\text{HFRCO}} \geq 19$ MHz | — | 300 | — | ns |
| | | $4 < f_{\text{HFRCO}} < 19$ MHz | — | 1 | — | μs |
| | | $f_{\text{HFRCO}} \leq 4$ MHz | — | 2.5 | — | μs |
| Current consumption on all supplies | I_{HFRCO} | $f_{\text{HFRCO}} = 38$ MHz | — | 267 | 299 | μA |
| | | $f_{\text{HFRCO}} = 32$ MHz | — | 224 | 248 | μA |
| | | $f_{\text{HFRCO}} = 26$ MHz | — | 189 | 211 | μA |
| | | $f_{\text{HFRCO}} = 19$ MHz | — | 154 | 172 | μA |
| | | $f_{\text{HFRCO}} = 16$ MHz | — | 133 | 148 | μA |
| | | $f_{\text{HFRCO}} = 13$ MHz | — | 118 | 135 | μA |
| | | $f_{\text{HFRCO}} = 7$ MHz | — | 89 | 100 | μA |
| | | $f_{\text{HFRCO}} = 4$ MHz | — | 34 | 44 | μA |
| | | $f_{\text{HFRCO}} = 2$ MHz | — | 29 | 40 | μA |
| | | $f_{\text{HFRCO}} = 1$ MHz | — | 26 | 36 | μA |
| Coarse trim step size (% of period) | $SS_{\text{HFRCO_COARSE}}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{\text{HFRCO_FINE}}$ | | — | 0.1 | — | % |
| Period jitter | PJ_{HFRCO} | | — | 0.2 | — | % RMS |
| Frequency limits | $f_{\text{HFRCO_BAND}}$ | FREQRANGE = 0, FINETUNING = 0 | 3.47 | — | 6.15 | MHz |
| | | FREQRANGE = 3, FINETUNING = 0 | 6.24 | — | 11.45 | MHz |
| | | FREQRANGE = 6, FINETUNING = 0 | 11.3 | — | 19.8 | MHz |
| | | FREQRANGE = 7, FINETUNING = 0 | 13.45 | — | 22.8 | MHz |
| | | FREQRANGE = 8, FINETUNING = 0 | 16.5 | — | 29.0 | MHz |
| | | FREQRANGE = 10, FINETUNING = 0 | 23.11 | — | 40.63 | MHz |
| | | FREQRANGE = 11, FINETUNING = 0 | 27.27 | — | 48 | MHz |
| | | FREQRANGE = 12, FINETUNING = 0 | 33.33 | — | 54 | MHz |

4.1.9.4 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.17. Ultra-low Frequency RC Oscillator (ULFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------|--------------|----------------|------|-----|------|------|
| Oscillation frequency | f_{ULFRCO} | | 0.95 | 1 | 1.07 | kHz |

4.1.10 Flash Memory Characteristics¹Table 4.18. Flash Memory Characteristics¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------|---|-------|------|-----|---------|
| Flash erase cycles before failure | EC_{FLASH} | | 10000 | — | — | cycles |
| Flash data retention | RET_{FLASH} | | 10 | — | — | years |
| Word (32-bit) programming time | t_{W_PROG} | Burst write, 128 words, average time per word | 20 | 26.3 | 30 | μ s |
| | | Single word | 62 | 68.9 | 80 | μ s |
| Page erase time ² | t_{PERASE} | | 20 | 29.5 | 40 | ms |
| Mass erase time ³ | t_{MERASE} | | 20 | 30 | 40 | ms |
| Device erase time ^{4 5} | t_{DERASE} | | — | 56.2 | 70 | ms |
| Erase current ⁶ | I_{ERASE} | Page Erase | — | — | 2.0 | mA |
| Write current ⁶ | I_{WRITE} | | — | — | 3.5 | mA |
| Supply voltage during flash erase and write | V_{FLASH} | | 1.62 | — | 3.6 | V |

Note:

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- Mass erase is issued by the CPU and erases all flash.
- Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
- From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- Measured at 25 °C.

4.1.11 General-Purpose I/O (GPIO)

Table 4.19. General-Purpose I/O (GPIO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|---|-----------|-----|-----------|------|
| Input low voltage ¹ | V _{IL} | GPIO pins | — | — | IOVDD*0.3 | V |
| Input high voltage ¹ | V _{IH} | GPIO pins | IOVDD*0.7 | — | — | V |
| Output high voltage relative to IOVDD | V _{OH} | Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ² = WEAK | IOVDD*0.8 | — | — | V |
| | | Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ² = WEAK | IOVDD*0.6 | — | — | V |
| | | Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ² = STRONG | IOVDD*0.8 | — | — | V |
| | | Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ² = STRONG | IOVDD*0.6 | — | — | V |
| Output low voltage relative to IOVDD | V _{OL} | Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ² = WEAK | — | — | IOVDD*0.2 | V |
| | | Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ² = WEAK | — | — | IOVDD*0.4 | V |
| | | Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ² = STRONG | — | — | IOVDD*0.2 | V |
| | | Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ² = STRONG | — | — | IOVDD*0.4 | V |
| Input leakage current | I _{IOLEAK} | All GPIO pins except PB14 and PB15, GPIO ≤ IOVDD | — | 0.1 | 30 | nA |
| | | PB14 and PB15, GPIO ≤ IOVDD | — | 0.1 | 50 | nA |
| Input leakage current on 5VTOL pads above IOVDD | I _{5VTOLLEAK} | IOVDD < GPIO ≤ IOVDD + 2 V | — | 3.3 | 15 | μA |
| I/O pin pull-up/pull-down resistor ³ | R _{PUD} | | 30 | 40 | 65 | kΩ |
| Pulse width of pulses removed by the glitch suppression filter | t _{IOGLITCH} | | 15 | 25 | 45 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------|---|-----|-----|-----|------|
| Output fall time, From 70% to 30% of V_{IO} | t_{IOF} | $C_L = 50$ pF, DRIVESTRENGTH ² = STRONG, SLEWRATE ² = 0x6 | — | 1.8 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ² = WEAK, SLEWRATE ² = 0x6 | — | 4.5 | — | ns |
| Output rise time, From 30% to 70% of V_{IO} | t_{IOR} | $C_L = 50$ pF, DRIVESTRENGTH ² = STRONG, SLEWRATE = 0x6 ² | — | 2.2 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ² = WEAK, SLEWRATE ² = 0x6 | — | 7.4 | — | ns |

Note:

1. GPIO input threshold are proportional to the IOVDD supply, except for RESETn which is proportional to AVDD.
2. In GPIO_Pn_CTRL register.
3. GPIO pull-ups are referenced to the IOVDD supply, except for RESETn, which connects to AVDD.

4.1.12 Voltage Monitor (VMON)

Table 4.20. Voltage Monitor (VMON)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|---|------|------|-----|------|
| Supply current (including I _{SENSE}) | I _{VMON} | In EM0 or EM1, 1 active channel | — | 6.3 | 8 | μA |
| | | In EM0 or EM1, All channels active | — | 12.5 | 15 | μA |
| | | In EM2, EM3 or EM4, 1 channel active and above threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 1 channel active and below threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, All channels active and above threshold | — | 99 | — | nA |
| | | In EM2, EM3 or EM4, All channels active and below threshold | — | 99 | — | nA |
| Loading of monitored supply | I _{SENSE} | In EM0 or EM1 | — | 2 | — | μA |
| | | In EM2, EM3 or EM4 | — | 2 | — | nA |
| Threshold range | V _{VMON_RANGE} | | 1.62 | — | 3.4 | V |
| Threshold step size | N _{VMON_STESP} | Coarse | — | 200 | — | mV |
| | | Fine | — | 20 | — | mV |
| Response time | t _{VMON_RES} | Supply drops at 1V/μs rate | — | 460 | — | ns |
| Hysteresis | V _{VMON_HYST} | | — | 26 | — | mV |

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.21. Analog to Digital Converter (ADC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------------------|---|---------------------|-----|--------------------|------|
| Resolution | V _{RESOLUTION} | | 6 | — | 12 | Bits |
| Input voltage range ¹ | V _{ADCIN} | Single ended | — | — | V _{FS} | V |
| | | Differential | -V _{FS} /2 | — | V _{FS} /2 | V |
| Input range of external reference voltage, single ended and differential | V _{ADCREFIN_P} | | 1 | — | V _{AVDD} | V |
| Power supply rejection ² | PSRR _{ADC} | At DC | — | 80 | — | dB |
| Analog input common mode rejection ratio | CMRR _{ADC} | At DC | — | 80 | — | dB |
| Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ³ = KEEPADC-WARM | I _{ADC_CONTINUOUS_LP} | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴ | — | 270 | 290 | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 ⁴ | — | 125 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 ⁴ | — | 80 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ³ = NORMAL | I _{ADC_NORMAL_LP} | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴ | — | 45 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 ⁴ | — | 8 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEPINSTANDBY or KEEPINSLOWACC | I _{ADC_STANDBY_LP} | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴ | — | 105 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴ | — | 70 | — | μA |
| Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ³ = KEEPADC-WARM | I _{ADC_CONTINUOUS_HP} | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴ | — | 325 | — | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 ⁴ | — | 175 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 ⁴ | — | 125 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ³ = NORMAL | I _{ADC_NORMAL_HP} | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴ | — | 85 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 ⁴ | — | 16 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEPINSTANDBY or KEEPINSLOWACC | I _{ADC_STANDBY_HP} | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴ | — | 160 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴ | — | 125 | — | μA |
| Current from HFPERCLK | I _{ADC_CLK} | HFPERCLK = 16 MHz | — | 140 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|--|-----|-------|-----|---------------|
| ADC clock frequency | f_{ADCCLK} | | — | — | 16 | MHz |
| Throughput rate | f_{ADCRATE} | | — | — | 1 | Msp/s |
| Conversion time ⁵ | t_{ADCCONV} | 6 bit | — | 7 | — | cycles |
| | | 8 bit | — | 9 | — | cycles |
| | | 12 bit | — | 13 | — | cycles |
| Startup time of reference generator and ADC core | t_{ADCSTART} | WARMUPMODE ³ = NORMAL | — | — | 5 | μs |
| | | WARMUPMODE ³ = KEEPIN-STANDBY | — | — | 2 | μs |
| | | WARMUPMODE ³ = KEEPINSLOWACC | — | — | 1 | μs |
| SNDR at 1Msp/s and $f_{\text{IN}} = 10\text{kHz}$ | SNDR _{ADC} | Internal reference ⁶ , differential measurement | 58 | 67 | — | dB |
| | | External reference ⁷ , differential measurement | — | 68 | — | dB |
| Spurious-free dynamic range (SFDR) | SFDR _{ADC} | 1 MSamples/s, 10 kHz full-scale sine wave | — | 75 | — | dB |
| Differential non-linearity (DNL) | DNL _{ADC} | 12 bit resolution, No missing codes | -1 | — | 2 | LSB |
| Integral non-linearity (INL), End point method | INL _{ADC} | 12 bit resolution | -6 | — | 6 | LSB |
| Offset error | $V_{\text{ADCOFFSETERR}}$ | | -3 | 0 | 3 | LSB |
| Gain error in ADC | V_{ADCGAIN} | Using internal reference | — | -0.2 | 3.5 | % |
| | | Using external reference | — | -1 | — | % |
| Temperature sensor slope | $V_{\text{TS_SLOPE}}$ | | — | -1.84 | — | mV/°C |

Note:

1. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_CTRL register.
4. In ADCn_BIASPROG register.
5. Derived from ADCCLK.
6. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is $\pm 1.25\text{ V}$. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.
7. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is $\pm 1.25\text{ V}$.

4.1.14 Analog Comparator (ACMP)

Table 4.22. Analog Comparator (ACMP)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------|--|-----|-----|--------------------|------|
| Input voltage range | V_{ACMPIN} | ACMPVDD = ACMPn_CTRL_PWRSEL ¹ | — | — | $V_{ACMPVDD}$ | V |
| Supply voltage | $V_{ACMPVDD}$ | BIASPROG ² ≤ 0x10 or FULL- BIAS ² = 0 | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | 0x10 < BIASPROG ² ≤ 0x20 and FULLBIAS ² = 1 | 2.1 | — | $V_{VREGVDD_MAX}$ | V |
| Active current not including voltage reference ³ | I_{ACMP} | BIASPROG ² = 1, FULLBIAS ² = 0 | — | 50 | — | nA |
| | | BIASPROG ² = 0x10, FULLBIAS ² = 0 | — | 306 | — | nA |
| | | BIASPROG ² = 0x02, FULLBIAS ² = 1 | — | 6.1 | 11 | μA |
| | | BIASPROG ² = 0x20, FULLBIAS ² = 1 | — | 74 | 92 | μA |
| Current consumption of inter- nal voltage reference ³ | $I_{ACMPREF}$ | VLP selected as input using 2.5 V Reference / 4 (0.625 V) | — | 50 | — | nA |
| | | VLP selected as input using VDD | — | 20 | — | nA |
| | | VBDIV selected as input using 1.25 V reference / 1 | — | 4.1 | — | μA |
| | | VADIV selected as input using VDD/1 | — | 2.4 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------|--|------|----------|------|---------------|
| Hysteresis ($V_{CM} = 1.25\text{ V}$, $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 1$) | $V_{ACMPHYST}$ | $HYSTSEL^4 = HYST0$ | -3 | 0 | 3 | mV |
| | | $HYSTSEL^4 = HYST1$ | 5 | 18 | 27 | mV |
| | | $HYSTSEL^4 = HYST2$ | 12 | 33 | 50 | mV |
| | | $HYSTSEL^4 = HYST3$ | 17 | 46 | 67 | mV |
| | | $HYSTSEL^4 = HYST4$ | 23 | 57 | 86 | mV |
| | | $HYSTSEL^4 = HYST5$ | 26 | 68 | 104 | mV |
| | | $HYSTSEL^4 = HYST6$ | 30 | 79 | 130 | mV |
| | | $HYSTSEL^4 = HYST7$ | 34 | 90 | 155 | mV |
| | | $HYSTSEL^4 = HYST8$ | -3 | 0 | 3 | mV |
| | | $HYSTSEL^4 = HYST9$ | -27 | -18 | -5 | mV |
| | | $HYSTSEL^4 = HYST10$ | -50 | -33 | -12 | mV |
| | | $HYSTSEL^4 = HYST11$ | -67 | -45 | -17 | mV |
| | | $HYSTSEL^4 = HYST12$ | -86 | -57 | -23 | mV |
| | | $HYSTSEL^4 = HYST13$ | -104 | -67 | -26 | mV |
| | | $HYSTSEL^4 = HYST14$ | -130 | -78 | -30 | mV |
| $HYSTSEL^4 = HYST15$ | -155 | -88 | -34 | mV | | |
| Comparator delay ⁵ | $t_{ACMPDELAY}$ | $BIASPROG^2 = 1$, $FULLBIAS^2 = 0$ | — | 30 | 95 | μs |
| | | $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 0$ | — | 3.7 | 10 | μs |
| | | $BIASPROG^2 = 0x02$, $FULLBIAS^2 = 1$ | — | 360 | 1000 | ns |
| | | $BIASPROG^2 = 0x20$, $FULLBIAS^2 = 1$ | — | 35 | — | ns |
| Offset voltage | $V_{ACMPOFFSET}$ | $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 1$ | -35 | — | 35 | mV |
| Reference voltage | $V_{ACMPREF}$ | Internal 1.25 V reference | 1 | 1.25 | 1.47 | V |
| | | Internal 2.5 V reference | 1.98 | 2.5 | 2.8 | V |
| Capacitive sense internal resistance | R_{CSRES} | $CSRESSEL^6 = 0$ | — | infinite | — | k Ω |
| | | $CSRESSEL^6 = 1$ | — | 15 | — | k Ω |
| | | $CSRESSEL^6 = 2$ | — | 27 | — | k Ω |
| | | $CSRESSEL^6 = 3$ | — | 39 | — | k Ω |
| | | $CSRESSEL^6 = 4$ | — | 51 | — | k Ω |
| | | $CSRESSEL^6 = 5$ | — | 102 | — | k Ω |
| | | $CSRESSEL^6 = 6$ | — | 164 | — | k Ω |
| | | $CSRESSEL^6 = 7$ | — | 239 | — | k Ω |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. | | | | | | |
| 2. In ACMPn_CTRL register. | | | | | | |
| 3. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. | | | | | | |
| 4. In ACMPn_HYSTERESIS registers. | | | | | | |
| 5. ± 100 mV differential drive. | | | | | | |
| 6. In ACMPn_INPUTSEL register. | | | | | | |

4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.23. Digital to Analog Converter (VDAC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|---|--------------------|------|-------------------|--------|
| Output voltage | V _{DACOUT} | Single-Ended | 0 | — | V _{VREF} | V |
| | | Differential ¹ | -V _{VREF} | — | V _{VREF} | V |
| Current consumption including references (2 channels) ² | I _{DAC} | 500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4 | — | 396 | — | μA |
| | | 44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4 | — | 72 | — | μA |
| | | 200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, REFSEL = 4, SETTLETIME = 0x02, WARMUP-TIME = 0x0A | — | 1.2 | — | μA |
| Current from HFPERCLK ³ | I _{DAC_CLK} | | — | 5.8 | — | μA/MHz |
| Sample rate | SR _{DAC} | | — | — | 500 | ksps |
| DAC clock frequency | f _{DAC} | | — | — | 1 | MHz |
| Conversion time | t _{DACCONV} | f _{DAC} = 1MHz | 2 | — | — | μs |
| Settling time | t _{DACSETTLE} | 50% fs step settling to 5 LSB | — | 2.5 | — | μs |
| Startup time | t _{DACSTARTUP} | Enable to 90% fs output, settling to 10 LSB | — | — | 12 | μs |
| Output impedance | R _{OUT} | DRIVESTRENGTH = 2, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 2, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Full supply range | — | 2 | — | Ω |
| Power supply rejection ratio ⁴ | PSRR | V _{out} = 50% fs. DC | — | 65.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|---|-------|------|-----|------|
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz | SNDR _{DAC} | 500 ksps, single-ended, internal 1.25V reference | — | 60.4 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 61.6 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 64.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 63.3 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 64.4 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 65.8 | — | dB |
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz | SNDR _{DAC_BAND} | 500 ksps, single-ended, internal 1.25V reference | — | 65.3 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 66.7 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 70.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 67.8 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 69.0 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 68.5 | — | dB |
| Total harmonic distortion | THD | | — | 70.2 | — | dB |
| Differential non-linearity ⁵ | DNL _{DAC} | | -0.99 | — | 1 | LSB |
| Integral non-linearity | INL _{DAC} | | -4 | — | 4 | LSB |
| Offset error ⁶ | V _{OFFSET} | T = 25 °C | -8 | — | 8 | mV |
| | | Across operating temperature range | -25 | — | 25 | mV |
| Gain error ⁶ | V _{GAIN} | T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -2.5 | — | 2.5 | % |
| | | T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5) | -5 | — | 5 | % |
| | | T = 25 °C, External reference (REFSEL = VDD or EXT) | -1.8 | — | 1.8 | % |
| | | Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -3.5 | — | 3.5 | % |
| | | Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5) | -7.5 | — | 7.5 | % |
| | | Across operating temperature range, External reference (REFSEL = VDD or EXT) | -2.0 | — | 2.0 | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|-------------------|----------------|-----|-----|-----|------|
| External load capacitance, OUTSCALE=0 | C _{LOAD} | | — | — | 75 | pF |

Note:

1. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
2. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
3. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC peripheral is enabled in the CMU.
4. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$, VDAC output at 90% of full scale
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.

4.1.16 Current Digital to Analog Converter (IDAC)

Table 4.24. Current Digital to Analog Converter (IDAC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|--|------|------|-----|--------|
| Number of ranges | N_{IDAC_RANGES} | | — | 4 | — | ranges |
| Output current | I_{IDAC_OUT} | RANGESEL ¹ = RANGE0 | 0.05 | — | 1.6 | μA |
| | | RANGESEL ¹ = RANGE1 | 1.6 | — | 4.7 | μA |
| | | RANGESEL ¹ = RANGE2 | 0.5 | — | 16 | μA |
| | | RANGESEL ¹ = RANGE3 | 2 | — | 64 | μA |
| Linear steps within each range | N_{IDAC_STEPS} | | — | 32 | — | steps |
| Step size | SS_{IDAC} | RANGESEL ¹ = RANGE0 | — | 50 | — | nA |
| | | RANGESEL ¹ = RANGE1 | — | 100 | — | nA |
| | | RANGESEL ¹ = RANGE2 | — | 500 | — | nA |
| | | RANGESEL ¹ = RANGE3 | — | 2 | — | μA |
| Total accuracy, STEPSEL ¹ = 0x10 | ACC_{IDAC} | EM0 or EM1, AVDD=3.3 V, T = 25 °C | -3 | — | 3 | % |
| | | EM0 or EM1, Across operating temperature range | -18 | — | 22 | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -2 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -1.7 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.8 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -0.7 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -0.6 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|---|-----|-------|-----|---------|
| Start up time | t_{IDAC_SU} | Output within 1% of steady state value | — | 5 | — | μs |
| Settling time, (output settled within 1% of steady state value), | t_{IDAC_SETTLE} | Range setting is changed | — | 5 | — | μs |
| | | Step value is changed | — | 1 | — | μs |
| Current consumption ² | I_{IDAC} | EM0 or EM1 Source mode, excluding output current, Across operating temperature range | — | 11 | 15 | μA |
| | | EM0 or EM1 Sink mode, excluding output current, Across operating temperature range | — | 13 | 18 | μA |
| | | EM2 or EM3 Source mode, excluding output current, T = 25 °C | — | 0.023 | — | μA |
| | | EM2 or EM3 Sink mode, excluding output current, T = 25 °C | — | 0.041 | — | μA |
| | | EM2 or EM3 Source mode, excluding output current, T \geq 85 °C | — | 11 | — | μA |
| | | EM2 or EM3 Sink mode, excluding output current, T \geq 85 °C | — | 13 | — | μA |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | I_{COMP_SRC} | RANGESEL ¹ = RANGE0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$ | — | 0.11 | — | % |
| | | RANGESEL ¹ = RANGE1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$ | — | 0.06 | — | % |
| | | RANGESEL ¹ = RANGE2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$ | — | 0.04 | — | % |
| | | RANGESEL ¹ = RANGE3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$ | — | 0.03 | — | % |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD | I_{COMP_SINK} | RANGESEL ¹ = RANGE0, output voltage = 100 mV | — | 0.12 | — | % |
| | | RANGESEL ¹ = RANGE1, output voltage = 100 mV | — | 0.05 | — | % |
| | | RANGESEL ¹ = RANGE2, output voltage = 150 mV | — | 0.04 | — | % |
| | | RANGESEL ¹ = RANGE3, output voltage = 250 mV | — | 0.03 | — | % |

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.17 Capacitive Sense (CSEN)

Table 4.25. Capacitive Sense (CSEN)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|--|-----|------|-----|------|
| Single conversion time (1x accumulation) | t _{CNV} | 12-bit SAR Conversions | — | 20.2 | — | μs |
| | | 16-bit SAR Conversions | — | 26.4 | — | μs |
| | | Delta Modulation Conversion (single comparison) | — | 1.55 | — | μs |
| Maximum external capacitive load | C _{EXTMAX} | IREFPROG=7 (Gain = 1x), including routing parasitics | — | 68 | — | pF |
| | | IREFPROG=0 (Gain = 10x), including routing parasitics | — | 680 | — | pF |
| Maximum external series impedance | R _{EXTMAX} | | — | 1 | — | kΩ |
| Supply current, EM2 bonded conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0 | I _{CSEN_BOND} | 12-bit SAR conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 326 | — | nA |
| | | Delta Modulation conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 226 | — | nA |
| | | 12-bit SAR conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 33 | — | nA |
| | | Delta Modulation conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 25 | — | nA |
| Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0 | I _{CSEN_EM2} | 12-bit SAR conversions, 20 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 690 | — | nA |
| | | Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 515 | — | nA |
| | | 12-bit SAR conversions, 200 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 79 | — | nA |
| | | Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 57 | — | nA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|------|-----|--------|
| Supply current, continuous conversions, WARMUP-MODE=KEEP_CSEN_WARM | I _{CSEN_ACTIVE} | SAR or Delta Modulation conversions of 33 pF capacitor, IRE-FPROG=0 (Gain = 10x), always on | — | 90.5 | — | μA |
| HFPERCLK supply current | I _{CSEN_HFPERCLK} | Current contribution from HFPERCLK when clock to CSEN block is enabled. | — | 2.25 | — | μA/MHz |

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the peripheral is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.18 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{1 2}.

Table 4.26. Operational Amplifier (OPAMP)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-------------------|--|------------------|------|-----------------------|------|
| Supply voltage (from AVDD) | V _{OPA} | HCMDIS = 0, Rail-to-rail input range | 2 | — | 3.8 | V |
| | | HCMDIS = 1 | 1.62 | — | 3.8 | V |
| Input voltage | V _{IN} | HCMDIS = 0, Rail-to-rail input range | V _{VSS} | — | V _{OPA} | V |
| | | HCMDIS = 1 | V _{VSS} | — | V _{OPA} -1.2 | V |
| Input impedance | R _{IN} | | 100 | — | — | MΩ |
| Output voltage | V _{OUT} | | V _{VSS} | — | V _{OPA} | V |
| Load capacitance ³ | C _{LOAD} | OUTSCALE = 0 | — | — | 75 | pF |
| | | OUTSCALE = 1 | — | — | 37.5 | pF |
| Output impedance | R _{OUT} | DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Buffer connection, Full supply range | — | 0.25 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Buffer connection, Full supply range | — | 0.6 | — | Ω |
| | | DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Buffer connection, Full supply range | — | 0.4 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Buffer connection, Full supply range | — | 1 | — | Ω |
| Internal closed-loop gain | G _{CL} | Buffer connection | 0.99 | 1 | 1.01 | - |
| | | 3x Gain connection | 2.93 | 2.99 | 3.05 | - |
| | | 16x Gain connection | 15.07 | 15.7 | 16.33 | - |
| Active current ⁴ | I _{OPA} | DRIVESTRENGTH = 3, OUTSCALE = 0 | — | 580 | — | μA |
| | | DRIVESTRENGTH = 2, OUTSCALE = 0 | — | 176 | — | μA |
| | | DRIVESTRENGTH = 1, OUTSCALE = 0 | — | 13 | — | μA |
| | | DRIVESTRENGTH = 0, OUTSCALE = 0 | — | 4.7 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|------------------|---|-----|------|-----|-------|
| Open-loop gain | G _{OL} | DRIVESTRENGTH = 3 | — | 135 | — | dB |
| | | DRIVESTRENGTH = 2 | — | 137 | — | dB |
| | | DRIVESTRENGTH = 1 | — | 121 | — | dB |
| | | DRIVESTRENGTH = 0 | — | 109 | — | dB |
| Loop unit-gain frequency ⁵ | UGF | DRIVESTRENGTH = 3, Buffer connection | — | 3.38 | — | MHz |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 0.9 | — | MHz |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 132 | — | kHz |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 34 | — | kHz |
| | | DRIVESTRENGTH = 3, 3x Gain connection | — | 2.57 | — | MHz |
| | | DRIVESTRENGTH = 2, 3x Gain connection | — | 0.71 | — | MHz |
| | | DRIVESTRENGTH = 1, 3x Gain connection | — | 113 | — | kHz |
| | | DRIVESTRENGTH = 0, 3x Gain connection | — | 28 | — | kHz |
| Phase margin | PM | DRIVESTRENGTH = 3, Buffer connection | — | 67 | — | ° |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 69 | — | ° |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 63 | — | ° |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 68 | — | ° |
| Output voltage noise | N _{OUT} | DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz | — | 146 | — | μVrms |
| | | DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz | — | 163 | — | μVrms |
| | | DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz | — | 170 | — | μVrms |
| | | DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz | — | 176 | — | μVrms |
| | | DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz | — | 313 | — | μVrms |
| | | DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz | — | 271 | — | μVrms |
| | | DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz | — | 247 | — | μVrms |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz | — | 245 | — | μVrms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|--|-----|-------|-----|------------|
| Slew rate ⁶ | SR | DRIVESTRENGTH = 3, INCBW=1 ⁷ | — | 4.7 | — | V/ μ s |
| | | DRIVESTRENGTH = 3, INCBW=0 | — | 1.5 | — | V/ μ s |
| | | DRIVESTRENGTH = 2, INCBW=1 ⁷ | — | 1.27 | — | V/ μ s |
| | | DRIVESTRENGTH = 2, INCBW=0 | — | 0.42 | — | V/ μ s |
| | | DRIVESTRENGTH = 1, INCBW=1 ⁷ | — | 0.17 | — | V/ μ s |
| | | DRIVESTRENGTH = 1, INCBW=0 | — | 0.058 | — | V/ μ s |
| | | DRIVESTRENGTH = 0, INCBW=1 ⁷ | — | 0.044 | — | V/ μ s |
| | | DRIVESTRENGTH = 0, INCBW=0 | — | 0.015 | — | V/ μ s |
| Startup time ⁸ | T _{START} | DRIVESTRENGTH = 2 | — | — | 12 | μ s |
| Input offset voltage | V _{OSI} | DRIVESTRENGTH = 2 or 3, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 1 or 0, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 2 or 3, across operating temperature range | -12 | — | 12 | mV |
| | | DRIVESTRENGTH = 1 or 0, across operating temperature range | -45 | — | 30 | mV |
| DC power supply rejection ratio ⁹ | PSRR _{DC} | Input referred | — | 70 | — | dB |
| DC common-mode rejection ratio ⁹ | CMRR _{DC} | Input referred | — | 70 | — | dB |
| Total harmonic distortion | THD _{OPA} | DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V | — | 90 | — | dB |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V | — | 90 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{INPUT} = 0.5\text{ V}$, $V_{OUTPUT} = 0.5\text{ V}$. | | | | | | |
| 2. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{INPUT} = 0.5\text{ V}$, $V_{OUTPUT} = 1.5\text{ V}$. Nominal voltage gain is 3. | | | | | | |
| 3. If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information. | | | | | | |
| 4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 μA current when the OPAMP drives 1.5 V between output and ground. | | | | | | |
| 5. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network. | | | | | | |
| 6. Step between 0.2V and $V_{OPA}-0.2\text{V}$, 10%-90% rising/falling range. | | | | | | |
| 7. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3 , or the OPAMP may not be stable. | | | | | | |
| 8. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV. | | | | | | |
| 9. When HCMDIS=1 and input common mode transitions the region from $V_{OPA}-1.4\text{V}$ to $V_{OPA}-1\text{V}$, input offset will change. PSRR and CMRR specifications do not apply to this transition region. | | | | | | |

4.1.19 Pulse Counter (PCNT)

Table 4.27. Pulse Counter (PCNT)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------|----------|--|-----|-----|-----|------|
| Input frequency | F_{IN} | Asynchronous Single and Quadrature Modes | — | — | 10 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |

4.1.20 Analog Port (APORT)

Table 4.28. Analog Port (APORT)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-------------|----------------------|-----|-----|-----|---------------|
| Supply current ^{1 2} | I_{APORT} | Operation in EM0/EM1 | — | 7 | — | μA |
| | | Operation in EM2/EM3 | — | 63 | — | nA |

Note:

- Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported peripheral currents. Additional peripherals requesting access to APORT do not incur further current.
- Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.

4.1.21 I2C

4.1.21.1 I2C Standard-mode (Sm)¹Table 4.29. I2C Standard-mode (Sm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|-----|-----|------|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 100 | kHz |
| SCL clock low time | t _{LOW} | | 4.7 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 4 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 250 | — | — | ns |
| SDA hold time ³ | t _{HD_DAT} | | 100 | — | 3450 | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 4.7 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 4 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 4 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 4.7 | — | — | μs |

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.21.2 I2C Fast-mode (Fm)¹Table 4.30. I2C Fast-mode (Fm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------|----------------|-----|-----|-----|---------|
| SCL clock frequency ² | f_{SCL} | | 0 | — | 400 | kHz |
| SCL clock low time | t_{LOW} | | 1.3 | — | — | μ s |
| SCL clock high time | t_{HIGH} | | 0.6 | — | — | μ s |
| SDA set-up time | t_{SU_DAT} | | 100 | — | — | ns |
| SDA hold time ³ | t_{HD_DAT} | | 100 | — | 900 | ns |
| Repeated START condition set-up time | t_{SU_STA} | | 0.6 | — | — | μ s |
| (Repeated) START condition hold time | t_{HD_STA} | | 0.6 | — | — | μ s |
| STOP condition set-up time | t_{SU_STO} | | 0.6 | — | — | μ s |
| Bus free time between a STOP and START condition | t_{BUF} | | 1.3 | — | — | μ s |

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.21.3 I2C Fast-mode Plus (Fm+)¹Table 4.31. I2C Fast-mode Plus (Fm+)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|------|-----|------|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 1000 | kHz |
| SCL clock low time | t _{LOW} | | 0.5 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.26 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 50 | — | — | ns |
| SDA hold time | t _{HD_DAT} | | 100 | — | — | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 0.26 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 0.26 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 0.26 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 0.5 | — | — | μs |

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.22 USART SPI Master Timing

Table 4.32. SPI Master Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------|----------------|------------------------------|-----|------|------|
| SCLK period ^{1 2 3} | t_{SCLK} | | 2 * $t_{H\text{FPERCLK}}$ | — | — | ns |
| CS to MOSI ^{1 2} | t_{CS_MO} | | -12.5 | — | 14 | ns |
| SCLK to MOSI ^{1 2} | t_{SCLK_MO} | | -8.5 | — | 10.5 | ns |
| MISO setup time ^{1 2} | t_{SU_MI} | IOVDD = 1.62 V | 90 | — | — | ns |
| | | IOVDD = 3.0 V | 42 | — | — | ns |
| MISO hold time ^{1 2} | t_{H_MI} | | -9 | — | — | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{H\text{FPERCLK}}$ is one period of the selected H FPERCLK .

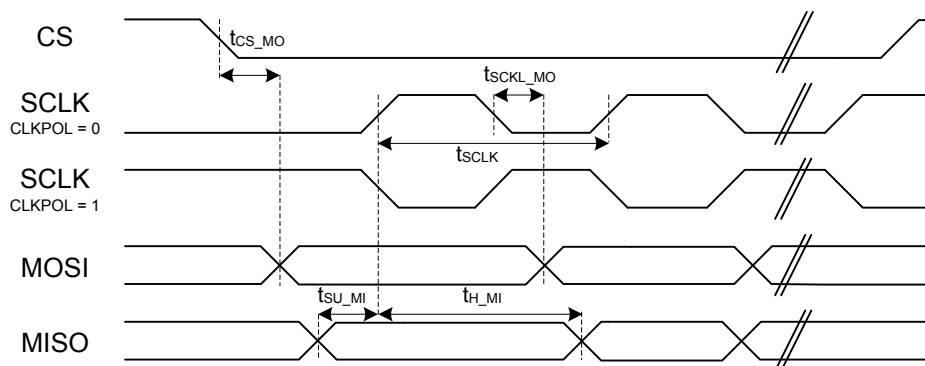


Figure 4.1. SPI Master Timing Diagram

4.1.23 USART SPI Slave Timing

Table 4.33. SPI Slave Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|-------------------|----------------|-----------------------------|-----|------------------------------|------|
| SCLK period ^{1 2 3} | t_{SCLK} | | 6 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK high time ^{1 2 3} | t_{SCLK_HI} | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK low time ^{1 2 3} | t_{SCLK_LO} | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| CS active to MISO ^{1 2} | $t_{CS_ACT_MI}$ | | 4 | — | 70 | ns |
| CS disable to MISO ^{1 2} | $t_{CS_DIS_MI}$ | | 4 | — | 50 | ns |
| MOSI setup time ^{1 2} | t_{SU_MO} | | 12.5 | — | — | ns |
| MOSI hold time ^{1 2 3} | t_{H_MO} | | 13 | — | — | ns |
| SCLK to MISO ^{1 2 3} | t_{SCLK_MI} | | 6 + 1.5 * $t_{HFPERCLK}$ | — | 45 + 2.5 * $t_{HFPERCLK}$ | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

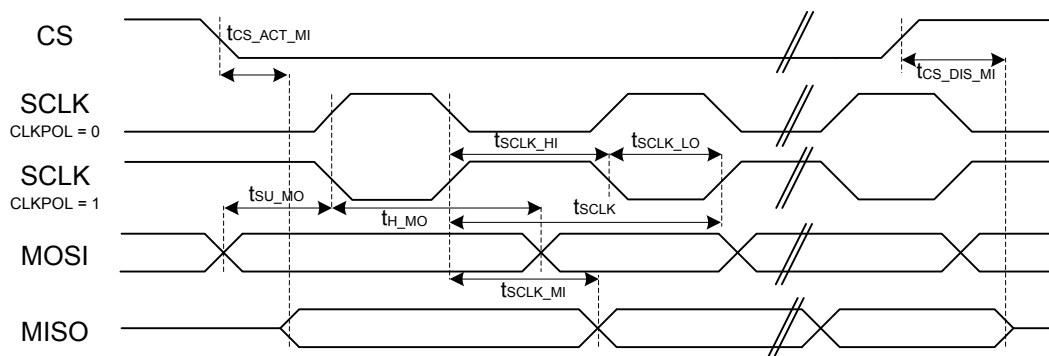


Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Zwave Radio

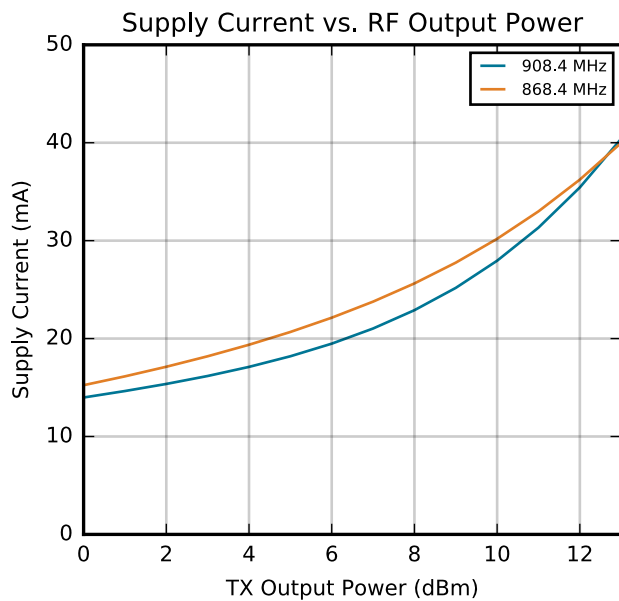


Figure 4.3. RF Transmitter Output Power

RF transmitter output power measured based on reference design BRD4200 at the output of the ZGM130S device.

5. Typical Connection Diagrams

5.1 Typical ZGM130S Connections

Typical connections for the ZGM130S module are shown in [Figure 5.1 Typical Power Connections for ZGM130S on page 61](#) and [Figure 5.2 Typical RF Connections for ZGM130S on page 61](#).

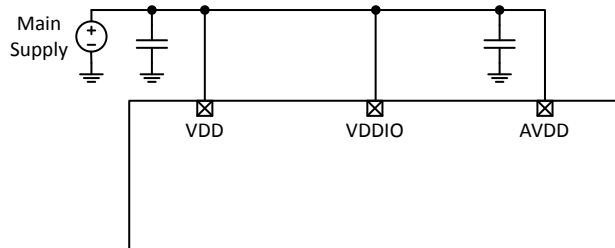


Figure 5.1. Typical Power Connections for ZGM130S

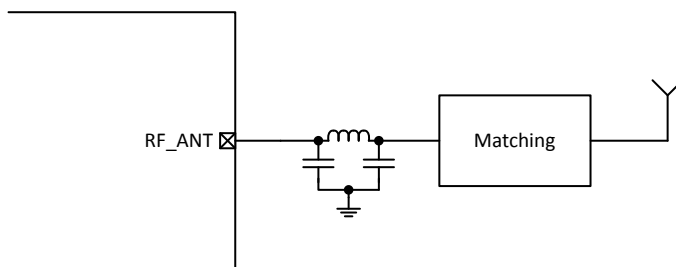


Figure 5.2. Typical RF Connections for ZGM130S

6. Pin Definitions

6.1 ZGM130S Device Pinout

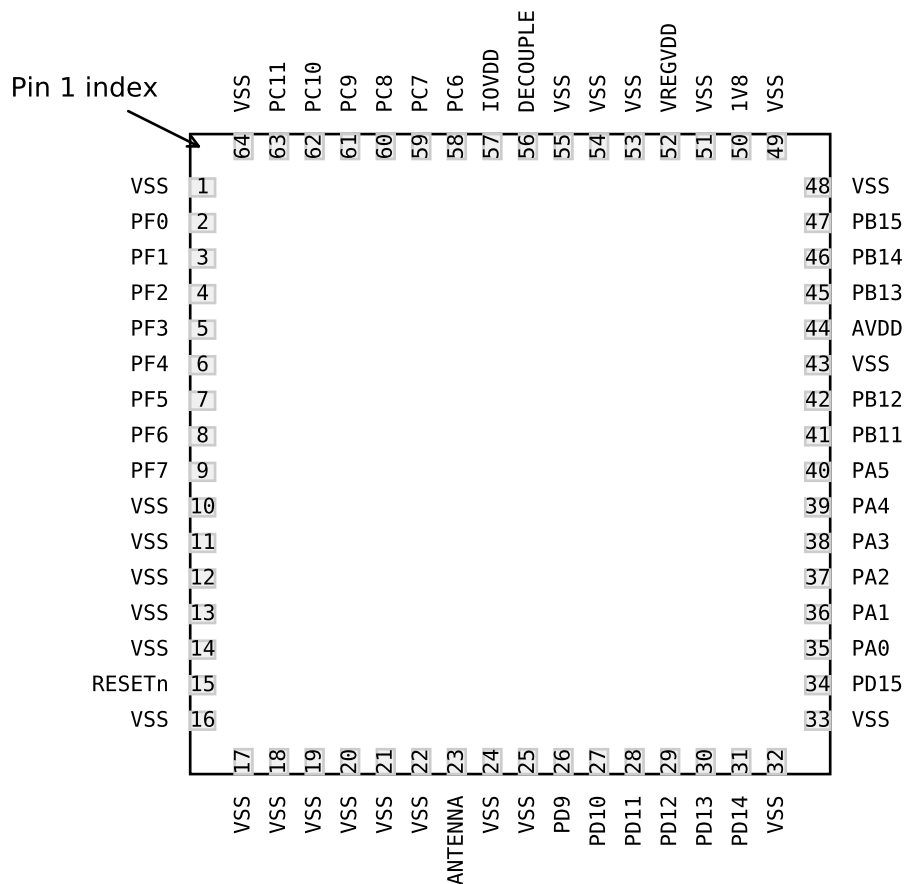


Figure 6.1. ZGM130S Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.2 GPIO Functionality Table](#) or [6.3 Alternate Functionality Overview](#).

Table 6.1. ZGM130S Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---|---|----------|--------|---|
| VSS | 1 10 11 12 13 14 16 17 18 19 20 21 22 24 25 32 33 43 48 49 51 53 54 55 64 | Ground | PF0 | 2 | GPIO (5V) |
| PF1 | 3 | GPIO (5V) | PF2 | 4 | GPIO (5V) |
| PF3 | 5 | GPIO (5V) | PF4 | 6 | GPIO (5V) |
| PF5 | 7 | GPIO (5V) | PF6 | 8 | GPIO (5V) |
| PF7 | 9 | GPIO (5V) | RESETn | 15 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| ANTENNA | 23 | 50 Ohm RF IO. | PD9 | 26 | GPIO (5V) |
| PD10 | 27 | GPIO (5V) | PD11 | 28 | GPIO (5V) |
| PD12 | 29 | GPIO (5V) | PD13 | 30 | GPIO |
| PD14 | 31 | GPIO | PD15 | 34 | GPIO |
| PA0 | 35 | GPIO | PA1 | 36 | GPIO |
| PA2 | 37 | GPIO | PA3 | 38 | GPIO |
| PA4 | 39 | GPIO | PA5 | 40 | GPIO (5V) |
| PB11 | 41 | GPIO | PB12 | 42 | GPIO |
| AVDD | 44 | Analog power supply. | PB13 | 45 | GPIO |
| PB14 | 46 | GPIO | PB15 | 47 | GPIO |
| 1V8 | 50 | 1.8V output of the internal DC-DC converter. Internally decoupled - do not add external decoupling. | VREGVDD | 52 | Voltage regulator VDD input |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|--------|--------------------------|
| DECOUPLE | 56 | N.C. This pin is the decouple output for an on-chip voltage regulator. This pin is internally decoupled, and should be left unconnected on the PCB. | IOVDD | 57 | Digital IO power supply. |
| PC6 | 58 | GPIO (5V) | PC7 | 59 | GPIO (5V) |
| PC8 | 60 | GPIO (5V) | PC9 | 61 | GPIO (5V) |
| PC10 | 62 | GPIO (5V) | PC11 | 63 | GPIO (5V) |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.2 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [6.3 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 6.2. GPIO Functionality Table

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PA0 | | TIM0_CC0 #0 | US0_TX #0 | | |
| | | TIM0_CC1 #31 | US0_RX #31 | | |
| | | TIM0_CC2 #30 | US0_CLK #30 | | |
| | | TIM0_CDTI0 #29 | US0_CS #29 | | |
| | | TIM0_CDTI1 #28 | US0_CTS #28 | | CMU_CLK1 #0 |
| | | TIM0_CDTI2 #27 | US0_RTS #27 | FRC_DCLK #0 | PRS_CH6 #0 |
| | BUSDY | TIM1_CC0 #0 | US1_TX #0 | FRC_DOUT #31 | PRS_CH7 #10 |
| | BUSCX | TIM1_CC1 #31 | US1_RX #31 | FRC_DFRAME #30 | PRS_CH8 #9 |
| | ADC0_EXTN | TIM1_CC2 #30 | US1_CLK #30 | MODEM_DCLK #0 | PRS_CH9 #8 |
| | | TIM1_CC3 #29 | US1_CS #29 | MODEM_DIN #31 | ACMP0_O #0 |
| | | WTIM0_CC0 #0 | US1_CTS #28 | MODEM_DOUT #30 | ACMP1_O #0 |
| | | LETIM0_OUT0 #0 | US1_RTS #27 | | LES_CH8 |
| | | LETIM0_OUT1 #31 | LEU0_TX #0 | | |
| | | PCNT0_S0IN #0 | LEU0_RX #31 | | |
| | | PCNT0_S1IN #31 | I2C0_SDA #0 | | |
| | | | I2C0_SCL #31 | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|--|----------------|---------------|-------|----------------|
| | Analog | Timers | Communication | Radio | Other |
| PA1 | BUSCY BUSDX ADC0_EXTP VDACC0_EXT | TIM0_CC0 #1 | US0_TX #1 | | |
| | | TIM0_CC1 #0 | US0_RX #0 | | |
| | | TIM0_CC2 #31 | US0_CLK #31 | | |
| | | TIM0_CDTI0 #30 | US0_CS #30 | | |
| | | TIM0_CDTI1 #29 | US0_CTS #29 | | CMU_CLK0 #0 |
| | | TIM0_CDTI2 #28 | US0_RTS #28 | | FRC_DCLK #1 |
| | | TIM1_CC0 #1 | US1_TX #1 | | FRC_DOUT #0 |
| | | TIM1_CC1 #0 | US1_RX #0 | | FRC_DFRAME #31 |
| | | TIM1_CC2 #31 | US1_CLK #31 | | MODEM_DCLK #1 |
| | | TIM1_CC3 #30 | US1_CS #30 | | MODEM_DIN #0 |
| | | WTIM0_CC0 #1 | US1_CTS #29 | | MODEM_DOUT #31 |
| | | LETIM0_OUT0 #1 | US1_RTS #28 | | |
| | | LETIM0_OUT1 #0 | LEU0_TX #1 | | |
| | | PCNT0_S0IN #1 | LEU0_RX #0 | | |
| | | PCNT0_S1IN #0 | I2C0_SDA #1 | | |
| | | | I2C0_SCL #0 | | |
| PA2 | VDACC0_OUT1ALT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P | TIM0_CC0 #2 | US0_TX #2 | | |
| | | TIM0_CC1 #1 | US0_RX #1 | | |
| | | TIM0_CC2 #0 | US0_CLK #0 | | |
| | | TIM0_CDTI0 #31 | US0_CS #31 | | |
| | | TIM0_CDTI1 #30 | US0_CTS #30 | | |
| | | TIM0_CDTI2 #29 | US0_RTS #29 | | FRC_DCLK #2 |
| | | TIM1_CC0 #2 | US1_TX #2 | | FRC_DOUT #1 |
| | | TIM1_CC1 #1 | US1_RX #1 | | FRC_DFRAME #0 |
| | | TIM1_CC2 #0 | US1_CLK #0 | | MODEM_DCLK #2 |
| | | TIM1_CC3 #31 | US1_CS #31 | | MODEM_DIN #1 |
| | | WTIM0_CC0 #2 | US1_CTS #30 | | MODEM_DOUT #0 |
| | | WTIM0_CC1 #0 | US1_RTS #29 | | |
| | | LETIM0_OUT0 #2 | LEU0_TX #2 | | |
| | | LETIM0_OUT1 #1 | LEU0_RX #1 | | |
| | | PCNT0_S0IN #2 | I2C0_SDA #2 | | |
| | | PCNT0_S1IN #1 | I2C0_SCL #1 | | |
| | | | PRS_CH6 #2 | | |
| | | | PRS_CH7 #1 | | |
| | | | PRS_CH8 #0 | | |
| | | | PRS_CH9 #10 | | |
| | | | ACMP0_O #2 | | |
| | | | ACMP1_O #2 | | |
| | | | LES_CH10 | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---------------|---|----------------|---------------|---------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PA3 | BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT | TIM0_CC0 #3 | US0_TX #3 | | |
| | | TIM0_CC1 #2 | US0_RX #2 | | |
| | | TIM0_CC2 #1 | US0_CLK #1 | | |
| | | TIM0_CDTI0 #0 | US0_CS #0 | | |
| | | TIM0_CDTI1 #31 | US0_CTS #31 | | PRS_CH6 #3 |
| | | TIM0_CDTI2 #30 | US0_RTS #30 | FRC_DCLK #3 | PRS_CH7 #2 |
| | | TIM1_CC0 #3 | US1_TX #3 | FRC_DOUT #2 | PRS_CH8 #1 |
| | | TIM1_CC1 #2 | US1_RX #2 | FRC_DFRAME #1 | PRS_CH9 #0 |
| | | TIM1_CC2 #1 | US1_CLK #1 | MODEM_DCLK #3 | ACMP0_O #3 |
| | | TIM1_CC3 #0 | US1_CS #0 | MODEM_DIN #2 | ACMP1_O #3 |
| | | WTIM0_CC0 #3 | US1_CTS #31 | MODEM_DOUT #1 | LES_CH11 |
| | | WTIM0_CC1 #1 | US1_RTS #30 | | GPIO_EM4WU8 |
| | | LETIM0_OUT0 #3 | LEU0_TX #3 | | |
| | | LETIM0_OUT1 #2 | LEU0_RX #2 | | |
| PCNT0_S0IN #3 | I2C0_SDA #3 | | | | |
| PCNT0_S1IN #2 | I2C0_SCL #2 | | | | |
| PA4 | VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N | TIM0_CC0 #4 | US0_TX #4 | | |
| | | TIM0_CC1 #3 | US0_RX #3 | | |
| | | TIM0_CC2 #2 | US0_CLK #2 | | |
| | | TIM0_CDTI0 #1 | US0_CS #1 | | |
| | | TIM0_CDTI1 #0 | US0_CTS #0 | | |
| | | TIM0_CDTI2 #31 | US0_RTS #31 | FRC_DCLK #4 | PRS_CH6 #4 |
| | | TIM1_CC0 #4 | US1_TX #4 | FRC_DOUT #3 | PRS_CH7 #3 |
| | | TIM1_CC1 #3 | US1_RX #3 | FRC_DFRAME #2 | PRS_CH8 #2 |
| | | TIM1_CC2 #2 | US1_CLK #2 | MODEM_DCLK #4 | PRS_CH9 #1 |
| | | TIM1_CC3 #1 | US1_CS #1 | MODEM_DIN #3 | ACMP0_O #4 |
| | | WTIM0_CC0 #4 | US1_CTS #0 | MODEM_DOUT #2 | ACMP1_O #4 |
| | | WTIM0_CC1 #2 | US1_RTS #31 | | LES_CH12 |
| | | WTIM0_CC2 #0 | LEU0_TX #4 | | |
| | | LETIM0_OUT0 #4 | LEU0_RX #3 | | |
| | | LETIM0_OUT1 #3 | I2C0_SDA #4 | | |
| | | PCNT0_S0IN #4 | I2C0_SCL #3 | | |
| PCNT0_S1IN #3 | | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------|----------------|-------------|---------------|--------------|
| | Analog | Timers | Communication | Radio | Other | |
| PA5 | VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSCY BUSDX | | US0_TX #5 | | | |
| | | | | US0_RX #4 | | |
| | | | | US0_CLK #3 | | |
| | | | TIM0_CC0 #5 | US0_CS #2 | | |
| | | | TIM0_CC1 #4 | US0_CTS #1 | | |
| | | | TIM0_CC2 #3 | US0_RTS #0 | | |
| | | | TIM0_CDT10 #2 | US1_TX #5 | | |
| | | | TIM0_CDT11 #1 | US1_RX #4 | | CMU_CLKI0 #4 |
| | | | TIM0_CDT12 #0 | US1_CLK #3 | FRC_DCLK #5 | PRS_CH6 #5 |
| | | | TIM1_CC0 #5 | US1_CS #2 | FRC_DOUT #4 | PRS_CH7 #4 |
| | | | TIM1_CC1 #4 | US1_CTS #1 | FRC_DFRAME #3 | PRS_CH8 #3 |
| | | | TIM1_CC2 #3 | US1_RTS #0 | MODEM_DCLK #5 | PRS_CH9 #2 |
| | | | TIM1_CC3 #2 | US2_TX #0 | MODEM_DIN #4 | ACMP0_O #5 |
| | | | WTIM0_CC0 #5 | US2_RX #31 | MODEM_DOUT #3 | ACMP1_O #5 |
| | | | WTIM0_CC1 #3 | US2_CLK #30 | | LES_CH13 |
| | | | WTIM0_CC2 #1 | US2_CS #29 | | ETM_TCLK #1 |
| | | | LETIM0_OUT0 #5 | US2_CTS #28 | | |
| | | | LETIM0_OUT1 #4 | US2_RTS #27 | | |
| | | | PCNT0_S0IN #5 | LEU0_TX #5 | | |
| | | | PCNT0_S1IN #4 | LEU0_RX #4 | | |
| | | | | I2C0_SDA #5 | | |
| | | | | I2C0_SCL #4 | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|----------------|---------------|---------------|------------|
| | Analog | Timers | Communication | Radio | Other |
| PB11 | | TIM0_CC0 #6 | | | |
| | | TIM0_CC1 #5 | | | |
| | | TIM0_CC2 #4 | US0_TX #6 | | |
| | | TIM0_CDTI0 #3 | US0_RX #5 | | |
| | | TIM0_CDTI1 #2 | US0_CLK #4 | | |
| | | TIM0_CDTI2 #1 | US0_CS #3 | | |
| | | TIM1_CC0 #6 | US0_CTS #2 | | |
| | | TIM1_CC1 #5 | US0_RTS #1 | FRC_DCLK #6 | PRS_CH6 #6 |
| | BUSCY | TIM1_CC2 #4 | US1_TX #6 | FRC_DOUT #5 | PRS_CH7 #5 |
| | BUSDX | TIM1_CC3 #3 | US1_RX #5 | FRC_DFRAME #4 | PRS_CH8 #4 |
| | OPA2_P | WTIM0_CC0 #15 | US1_CLK #4 | MODEM_DCLK #6 | PRS_CH9 #3 |
| | | WTIM0_CC1 #13 | US1_CS #3 | MODEM_DIN #5 | ACMP0_O #6 |
| | | WTIM0_CC2 #11 | US1_CTS #2 | MODEM_DOUT #4 | ACMP1_O #6 |
| | | WTIM0_CDTI0 #7 | US1_RTS #1 | | |
| | | WTIM0_CDTI1 #5 | LEU0_TX #6 | | |
| | | WTIM0_CDTI2 #3 | LEU0_RX #5 | | |
| | | LETIM0_OUT0 #6 | I2C0_SDA #6 | | |
| | | LETIM0_OUT1 #5 | I2C0_SCL #5 | | |
| | | PCNT0_S0IN #6 | | | |
| | | PCNT0_S1IN #5 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|----------------|---------------|---------------|------------|
| | Analog | Timers | Communication | Radio | Other |
| PB12 | | TIM0_CC0 #7 | | | |
| | | TIM0_CC1 #6 | | | |
| | | TIM0_CC2 #5 | US0_TX #7 | | |
| | | TIM0_CDTI0 #4 | US0_RX #6 | | |
| | | TIM0_CDTI1 #3 | US0_CLK #5 | | |
| | | TIM0_CDTI2 #2 | US0_CS #4 | | |
| | | TIM1_CC0 #7 | US0_CTS #3 | | |
| | | TIM1_CC1 #6 | US0_RTS #2 | FRC_DCLK #7 | PRS_CH6 #7 |
| | BUSDY | TIM1_CC2 #5 | US1_TX #7 | FRC_DOUT #6 | PRS_CH7 #6 |
| | BUSCX | TIM1_CC3 #4 | US1_RX #6 | FRC_DFRAME #5 | PRS_CH8 #5 |
| | OPA2_OUT | WTIM0_CC0 #16 | US1_CLK #5 | MODEM_DCLK #7 | PRS_CH9 #4 |
| | | WTIM0_CC1 #14 | US1_CS #4 | MODEM_DIN #6 | ACMP0_O #7 |
| | | WTIM0_CC2 #12 | US1_CTS #3 | MODEM_DOUT #5 | ACMP1_O #7 |
| | | WTIM0_CDTI0 #8 | US1_RTS #2 | | |
| | | WTIM0_CDTI1 #6 | LEU0_TX #7 | | |
| | | WTIM0_CDTI2 #4 | LEU0_RX #6 | | |
| | | LETIM0_OUT0 #7 | I2C0_SDA #7 | | |
| | | LETIM0_OUT1 #6 | I2C0_SCL #6 | | |
| | | PCNT0_S0IN #7 | | | |
| | | PCNT0_S1IN #6 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|----------------|---------------|---------------|-------|
| | Analog | Timers | Communication | Radio | Other |
| PB13 | BUSCY BUSDX OPA2_N | TIM0_CC0 #8 | | | |
| | | TIM0_CC1 #7 | | | |
| | | TIM0_CC2 #6 | US0_TX #8 | | |
| | | TIM0_CDTI0 #5 | US0_RX #7 | | |
| | | TIM0_CDTI1 #4 | US0_CLK #6 | | |
| | | TIM0_CDTI2 #3 | US0_CS #5 | | |
| | | TIM1_CC0 #8 | US0_CTS #4 | | |
| | | TIM1_CC1 #7 | US0_RTS #3 | FRC_DCLK #8 | |
| | | TIM1_CC2 #6 | US1_TX #8 | FRC_DOUT #7 | |
| | | TIM1_CC3 #5 | US1_RX #7 | FRC_DFRAME #6 | |
| | | WTIM0_CC0 #17 | US1_CLK #6 | MODEM_DCLK #8 | |
| | | WTIM0_CC1 #15 | US1_CS #5 | MODEM_DIN #7 | |
| | | WTIM0_CC2 #13 | US1_CTS #4 | MODEM_DOUT #6 | |
| | | WTIM0_CDTI0 #9 | US1_RTS #3 | | |
| | | WTIM0_CDTI1 #7 | LEU0_TX #8 | | |
| | | WTIM0_CDTI2 #5 | LEU0_RX #7 | | |
| | | LETIM0_OUT0 #8 | I2C0_SDA #8 | | |
| | | LETIM0_OUT1 #7 | I2C0_SCL #7 | | |
| | | PCNT0_S0IN #8 | | | |
| | | PCNT0_S1IN #7 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|---------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PB14 | BUSDY BUSCX | TIM0_CC0 #9 | | | |
| | | TIM0_CC1 #8 | | | |
| | | TIM0_CC2 #7 | US0_TX #9 | | |
| | | TIM0_CDT10 #6 | US0_RX #8 | | |
| | | TIM0_CDT11 #5 | US0_CLK #7 | | |
| | | TIM0_CDT12 #4 | US0_CS #6 | | |
| | | TIM1_CC0 #9 | US0_CTS #5 | | |
| | | TIM1_CC1 #8 | US0_RTS #4 | FRC_DCLK #9 | CMU_CLK1 #1 |
| | | TIM1_CC2 #7 | US1_TX #9 | FRC_DOUT #8 | PRS_CH6 #9 |
| | | TIM1_CC3 #6 | US1_RX #8 | FRC_DFRAME #7 | PRS_CH7 #8 |
| | | WTIM0_CC0 #18 | US1_CLK #7 | MODEM_DCLK #9 | PRS_CH8 #7 |
| | | WTIM0_CC1 #16 | US1_CS #6 | MODEM_DIN #8 | PRS_CH9 #6 |
| | | WTIM0_CC2 #14 | US1_CTS #5 | MODEM_DOUT #7 | ACMP0_O #9 |
| | | WTIM0_CDT10 #10 | US1_RTS #4 | | ACMP1_O #9 |
| | | WTIM0_CDT11 #8 | LEU0_TX #9 | | |
| | | WTIM0_CDT12 #6 | LEU0_RX #8 | | |
| | | LETIM0_OUT0 #9 | I2C0_SDA #9 | | |
| | | LETIM0_OUT1 #8 | I2C0_SCL #8 | | |
| | | PCNT0_S0IN #9 | | | |
| | | PCNT0_S1IN #8 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PB15 | | TIM0_CC0 #10 | | | |
| | | TIM0_CC1 #9 | | | |
| | | TIM0_CC2 #8 | US0_TX #10 | | |
| | | TIM0_CDT10 #7 | US0_RX #9 | | |
| | | TIM0_CDT11 #6 | US0_CLK #8 | | |
| | | TIM0_CDT12 #5 | US0_CS #7 | | |
| | | TIM1_CC0 #10 | US0_CTS #6 | | CMU_CLK0 #1 |
| | | TIM1_CC1 #9 | US0_RTS #5 | FRC_DCLK #10 | PRS_CH6 #10 |
| | | TIM1_CC2 #8 | US1_TX #10 | FRC_DOUT #9 | PRS_CH7 #9 |
| | BUSCY | TIM1_CC3 #7 | US1_RX #9 | FRC_DFRAME #8 | PRS_CH8 #8 |
| | BUSDY | WTIM0_CC0 #19 | US1_CLK #8 | MODEM_DCLK #10 | PRS_CH9 #7 |
| | | WTIM0_CC1 #17 | US1_CS #7 | MODEM_DIN #9 | ACMP0_O #10 |
| | | WTIM0_CC2 #15 | US1_CTS #6 | MODEM_DOUT #8 | ACMP1_O #10 |
| | | WTIM0_CDT10 #11 | US1_RTS #5 | | |
| | | WTIM0_CDT11 #9 | LEU0_TX #10 | | |
| | | WTIM0_CDT12 #7 | LEU0_RX #9 | | |
| | | LETIM0_OUT0 #10 | I2C0_SDA #10 | | |
| | | LETIM0_OUT1 #9 | I2C0_SCL #9 | | |
| | | PCNT0_S0IN #10 | | | |
| | | PCNT0_S1IN #9 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|--------------|
| | Analog | Timers | Communication | Radio | Other |
| PC6 | BUSBY BUSAX | TIM0_CC0 #11 | | | |
| | | TIM0_CC1 #10 | | | |
| | | TIM0_CC2 #9 | US0_TX #11 | | |
| | | TIM0_CDTI0 #8 | US0_RX #10 | | |
| | | TIM0_CDTI1 #7 | US0_CLK #9 | | |
| | | TIM0_CDTI2 #6 | US0_CS #8 | | |
| | | TIM1_CC0 #11 | US0_CTS #7 | | |
| | | TIM1_CC1 #10 | US0_RTS #6 | FRC_DCLK #11 | CMU_CLK0 #2 |
| | | TIM1_CC2 #9 | US1_TX #11 | FRC_DOUT #10 | CMU_CLKI0 #2 |
| | | TIM1_CC3 #8 | US1_RX #10 | FRC_DFRAME #9 | PRS_CH0 #8 |
| | | WTIM0_CC0 #26 | US1_CLK #9 | MODEM_DCLK #11 | PRS_CH9 #11 |
| | | WTIM0_CC1 #24 | US1_CS #8 | MODEM_DIN #10 | PRS_CH10 #0 |
| | | WTIM0_CC2 #22 | US1_CTS #7 | MODEM_DOUT #9 | PRS_CH11 #5 |
| | | WTIM0_CDTI0 #18 | US1_RTS #6 | | ACMP0_O #11 |
| | | WTIM0_CDTI1 #16 | LEU0_TX #11 | | ACMP1_O #11 |
| | | WTIM0_CDTI2 #14 | LEU0_RX #10 | | ETM_TCLK #3 |
| | | LETIM0_OUT0 #11 | I2C0_SDA #11 | | |
| | | LETIM0_OUT1 #10 | I2C0_SCL #10 | | |
| | | PCNT0_S0IN #11 | | | |
| | | PCNT0_S1IN #10 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PC7 | BUSAY BUSBX | TIM0_CC0 #12 | | | |
| | | TIM0_CC1 #11 | | | |
| | | TIM0_CC2 #10 | US0_TX #12 | | |
| | | TIM0_CDTI0 #9 | US0_RX #11 | | |
| | | TIM0_CDTI1 #8 | US0_CLK #10 | | |
| | | TIM0_CDTI2 #7 | US0_CS #9 | | |
| | | TIM1_CC0 #12 | US0_CTS #8 | | CMU_CLK1 #2 |
| | | TIM1_CC1 #11 | US0_RTS #7 | FRC_DCLK #12 | PRS_CH0 #9 |
| | | TIM1_CC2 #10 | US1_TX #12 | FRC_DOUT #11 | PRS_CH9 #12 |
| | | TIM1_CC3 #9 | US1_RX #11 | FRC_DFRAME #10 | PRS_CH10 #1 |
| | | WTIM0_CC0 #27 | US1_CLK #10 | MODEM_DCLK #12 | PRS_CH11 #0 |
| | | WTIM0_CC1 #25 | US1_CS #9 | MODEM_DIN #11 | ACMP0_O #12 |
| | | WTIM0_CC2 #23 | US1_CTS #8 | MODEM_DOUT #10 | ACMP1_O #12 |
| | | WTIM0_CDTI0 #19 | US1_RTS #7 | | ETM_TD0 |
| | | WTIM0_CDTI1 #17 | LEU0_TX #12 | | |
| | | WTIM0_CDTI2 #15 | LEU0_RX #11 | | |
| | | LETIM0_OUT0 #12 | I2C0_SDA #12 | | |
| | | LETIM0_OUT1 #11 | I2C0_SCL #11 | | |
| | | PCNT0_S0IN #12 | | | |
| | | PCNT0_S1IN #11 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PC8 | BUSBY BUSAX | TIM0_CC0 #13 | | | |
| | | TIM0_CC1 #12 | | | |
| | | TIM0_CC2 #11 | US0_TX #13 | | |
| | | TIM0_CDTI0 #10 | US0_RX #12 | | |
| | | TIM0_CDTI1 #9 | US0_CLK #11 | | |
| | | TIM0_CDTI2 #8 | US0_CS #10 | | |
| | | TIM1_CC0 #13 | US0_CTS #9 | | |
| | | TIM1_CC1 #12 | US0_RTS #8 | FRC_DCLK #13 | PRS_CH0 #10 |
| | | TIM1_CC2 #11 | US1_TX #13 | FRC_DOUT #12 | PRS_CH9 #13 |
| | | TIM1_CC3 #10 | US1_RX #12 | FRC_DFRAME #11 | PRS_CH10 #2 |
| | | WTIM0_CC0 #28 | US1_CLK #11 | MODEM_DCLK #13 | PRS_CH11 #1 |
| | | WTIM0_CC1 #26 | US1_CS #10 | MODEM_DIN #12 | ACMP0_O #13 |
| | | WTIM0_CC2 #24 | US1_CTS #9 | MODEM_DOUT #11 | ACMP1_O #13 |
| | | WTIM0_CDTI0 #20 | US1_RTS #8 | | ETM_TD1 |
| | | WTIM0_CDTI1 #18 | LEU0_TX #13 | | |
| | | WTIM0_CDTI2 #16 | LEU0_RX #12 | | |
| | | LETIM0_OUT0 #13 | I2C0_SDA #13 | | |
| | | LETIM0_OUT1 #12 | I2C0_SCL #12 | | |
| | | PCNT0_S0IN #13 | | | |
| | | PCNT0_S1IN #12 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PC9 | BUSAY BUSBX | TIM0_CC0 #14 | | | |
| | | TIM0_CC1 #13 | | | |
| | | TIM0_CC2 #12 | US0_TX #14 | | |
| | | TIM0_CDTI0 #11 | US0_RX #13 | | |
| | | TIM0_CDTI1 #10 | US0_CLK #12 | | |
| | | TIM0_CDTI2 #9 | US0_CS #11 | | |
| | | TIM1_CC0 #14 | US0_CTS #10 | | |
| | | TIM1_CC1 #13 | US0_RTS #9 | FRC_DCLK #14 | PRS_CH0 #11 |
| | | TIM1_CC2 #12 | US1_TX #14 | FRC_DOUT #13 | PRS_CH9 #14 |
| | | TIM1_CC3 #11 | US1_RX #13 | FRC_DFRAME #12 | PRS_CH10 #3 |
| | | WTIM0_CC0 #29 | US1_CLK #12 | MODEM_DCLK #14 | PRS_CH11 #2 |
| | | WTIM0_CC1 #27 | US1_CS #11 | MODEM_DIN #13 | ACMP0_O #14 |
| | | WTIM0_CC2 #25 | US1_CTS #10 | MODEM_DOUT #12 | ACMP1_O #14 |
| | | WTIM0_CDTI0 #21 | US1_RTS #9 | | ETM_TD2 |
| | | WTIM0_CDTI1 #19 | LEU0_TX #14 | | |
| | | WTIM0_CDTI2 #17 | LEU0_RX #13 | | |
| | | LETIM0_OUT0 #14 | I2C0_SDA #14 | | |
| | | LETIM0_OUT1 #13 | I2C0_SCL #13 | | |
| | | PCNT0_S0IN #14 | | | |
| | | PCNT0_S1IN #13 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------|
| | Analog | Timers | Communication | Radio | Other |
| PC10 | BUSBY BUSAX | TIM0_CC0 #15 | | | |
| | | TIM0_CC1 #14 | US0_TX #15 | | |
| | | TIM0_CC2 #13 | US0_RX #14 | | |
| | | TIM0_CDTI0 #12 | US0_CLK #13 | | |
| | | TIM0_CDTI1 #11 | US0_CS #12 | | |
| | | TIM0_CDTI2 #10 | US0_CTS #11 | | |
| | | TIM1_CC0 #15 | US0_RTS #10 | | |
| | | TIM1_CC1 #14 | US1_TX #15 | FRC_DCLK #15 | |
| | | TIM1_CC2 #13 | US1_RX #14 | FRC_DOUT #14 | |
| | | TIM1_CC3 #12 | US1_CLK #13 | FRC_DFRAME #13 | |
| | | WTIM0_CC0 #30 | US1_CS #12 | MODEM_DCLK #15 | |
| | | WTIM0_CC1 #28 | US1_CTS #11 | MODEM_DIN #14 | |
| | | WTIM0_CC2 #26 | US1_RTS #10 | MODEM_DOUT #13 | |
| | | WTIM0_CDTI0 #22 | LEU0_TX #15 | | |
| | | WTIM0_CDTI1 #20 | LEU0_RX #14 | | |
| | | WTIM0_CDTI2 #18 | I2C0_SDA #15 | | |
| | | LETIM0_OUT0 #15 | I2C0_SCL #14 | | |
| | | LETIM0_OUT1 #14 | I2C1_SDA #19 | | |
| | | PCNT0_S0IN #15 | I2C1_SCL #18 | | |
| | | PCNT0_S1IN #14 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PC11 | | TIM0_CC0 #16 | | | |
| | | TIM0_CC1 #15 | US0_TX #16 | | |
| | | TIM0_CC2 #14 | US0_RX #15 | | |
| | | TIM0_CDTI0 #13 | US0_CLK #14 | | |
| | | TIM0_CDTI1 #12 | US0_CS #13 | | |
| | | TIM0_CDTI2 #11 | US0_CTS #12 | | |
| | | TIM1_CC0 #16 | US0_RTS #11 | | CMU_CLK0 #3 |
| | | TIM1_CC1 #15 | US1_TX #16 | FRC_DCLK #16 | PRS_CH0 #13 |
| | | TIM1_CC2 #14 | US1_RX #15 | FRC_DOUT #15 | PRS_CH9 #16 |
| | BUSAY | TIM1_CC3 #13 | US1_CLK #14 | FRC_DFRAME #14 | PRS_CH10 #5 |
| | BUSBX | WTIM0_CC0 #31 | US1_CS #13 | MODEM_DCLK #16 | PRS_CH11 #4 |
| | | WTIM0_CC1 #29 | US1_CTS #12 | MODEM_DIN #15 | ACMP0_O #16 |
| | | WTIM0_CC2 #27 | US1_RTS #11 | MODEM_DOUT #14 | ACMP1_O #16 |
| | | WTIM0_CDTI0 #23 | LEU0_TX #16 | | DBG_SWO #3 |
| | | WTIM0_CDTI1 #21 | LEU0_RX #15 | | |
| | | WTIM0_CDTI2 #19 | I2C0_SDA #16 | | |
| | | LETIM0_OUT0 #16 | I2C0_SCL #15 | | |
| | | LETIM0_OUT1 #15 | I2C1_SDA #20 | | |
| | | PCNT0_S0IN #16 | I2C1_SCL #19 | | |
| | | PCNT0_S1IN #15 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|-----------------|---------------|--------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other | |
| PD9 | BUSCY BUSDX | TIM0_CC0 #17 | | | | |
| | | TIM0_CC1 #16 | | | | |
| | | TIM0_CC2 #15 | | US0_TX #17 | | |
| | | TIM0_CDTI0 #14 | | US0_RX #16 | | |
| | | TIM0_CDTI1 #13 | | US0_CLK #15 | | |
| | | TIM0_CDTI2 #12 | | US0_CS #14 | | |
| | | TIM1_CC0 #17 | | US0_CTS #13 | | CMU_CLK0 #4 |
| | | TIM1_CC1 #16 | | US0_RTS #12 | FRC_DCLK #17 | PRS_CH3 #8 |
| | | TIM1_CC2 #15 | | US1_TX #17 | FRC_DOUT #16 | PRS_CH4 #0 |
| | | TIM1_CC3 #14 | | US1_RX #16 | FRC_DFRAME #15 | PRS_CH5 #6 |
| | | WTIM0_CC1 #31 | | US1_CLK #15 | MODEM_DCLK #17 | PRS_CH6 #11 |
| | | WTIM0_CC2 #29 | | US1_CS #14 | MODEM_DIN #16 | ACMP0_O #17 |
| | | WTIM0_CDTI0 #25 | | US1_CTS #13 | MODEM_DOUT #15 | ACMP1_O #17 |
| | | WTIM0_CDTI1 #23 | | US1_RTS #12 | | LES_CH1 |
| | | WTIM0_CDTI2 #21 | | LEU0_TX #17 | | |
| | | LETIM0_OUT0 #17 | | LEU0_RX #16 | | |
| | | LETIM0_OUT1 #16 | | I2C0_SDA #17 | | |
| | | PCNT0_S0IN #17 | | I2C0_SCL #16 | | |
| | | PCNT0_S1IN #16 | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PD10 | | TIM0_CC0 #18 | | | |
| | | TIM0_CC1 #17 | US0_TX #18 | | |
| | | TIM0_CC2 #16 | US0_RX #17 | | |
| | | TIM0_CDTI0 #15 | US0_CLK #16 | | |
| | | TIM0_CDTI1 #14 | US0_CS #15 | | |
| | | TIM0_CDTI2 #13 | US0_CTS #14 | | CMU_CLK1 #4 |
| | | TIM1_CC0 #18 | US0_RTS #13 | FRC_DCLK #18 | PRS_CH3 #9 |
| | | TIM1_CC1 #17 | US1_TX #18 | FRC_DOUT #17 | PRS_CH4 #1 |
| | BUSDY | TIM1_CC2 #16 | US1_RX #17 | FRC_DFRAME #16 | PRS_CH5 #0 |
| | BUSCX | TIM1_CC3 #15 | US1_CLK #16 | MODEM_DCLK #18 | PRS_CH6 #12 |
| | | WTIM0_CC2 #30 | US1_CS #15 | MODEM_DIN #17 | ACMP0_O #18 |
| | | WTIM0_CDTI0 #26 | US1_CTS #14 | MODEM_DOUT #16 | ACMP1_O #18 |
| | | WTIM0_CDTI1 #24 | US1_RTS #13 | | LES_CH2 |
| | | WTIM0_CDTI2 #22 | LEU0_TX #18 | | |
| | | LETIM0_OUT0 #18 | LEU0_RX #17 | | |
| | | LETIM0_OUT1 #17 | I2C0_SDA #18 | | |
| | | PCNT0_S0IN #18 | I2C0_SCL #17 | | |
| | | PCNT0_S1IN #17 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|----------------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PD11 | BUSCY BUSDX | TIM0_CC0 #19 | | | |
| | | TIM0_CC1 #18 | US0_TX #19 | | |
| | | TIM0_CC2 #17 | US0_RX #18 | | |
| | | TIM0_CDTI0 #16 | US0_CLK #17 | | |
| | | TIM0_CDTI1 #15 | US0_CS #16 | | |
| | | TIM0_CDTI2 #14 | US0_CTS #15 | | |
| | | TIM1_CC0 #19 | US0_RTS #14 | FRC_DCLK #19 | PRS_CH3 #10 |
| | | TIM1_CC1 #18 | US1_TX #19 | FRC_DOUT #18 | PRS_CH4 #2 |
| | | TIM1_CC2 #17 | US1_RX #18 | FRC_DFRAME #17 | PRS_CH5 #1 |
| | | TIM1_CC3 #16 | US1_CLK #17 | MODEM_DCLK #19 | PRS_CH6 #13 |
| | | WTIM0_CC2 #31 | US1_CS #16 | MODEM_DIN #18 | ACMP0_O #19 |
| | | WTIM0_CDTI0 #27 | US1_CTS #15 | MODEM_DOUT #17 | ACMP1_O #19 |
| | | WTIM0_CDTI1 #25 | US1_RTS #14 | | LES_CH3 |
| | | WTIM0_CDTI2 #23 | LEU0_TX #19 | | |
| | | LETIM0_OUT0 #19 | LEU0_RX #18 | | |
| | | LETIM0_OUT1 #18 | I2C0_SDA #19 | | |
| | | PCNT0_S0IN #19 | I2C0_SCL #18 | | |
| PCNT0_S1IN #18 | | | | | |
| PD12 | VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSDY BUSCX | TIM0_CC0 #20 | US0_TX #20 | | |
| | | TIM0_CC1 #19 | US0_RX #19 | | |
| | | TIM0_CC2 #18 | US0_CLK #18 | | |
| | | TIM0_CDTI0 #17 | US0_CS #17 | | |
| | | TIM0_CDTI1 #16 | US0_CTS #16 | | |
| | | TIM0_CDTI2 #15 | US0_RTS #15 | FRC_DCLK #20 | PRS_CH3 #11 |
| | | TIM1_CC0 #20 | US1_TX #20 | FRC_DOUT #19 | PRS_CH4 #3 |
| | | TIM1_CC1 #19 | US1_RX #19 | FRC_DFRAME #18 | PRS_CH5 #2 |
| | | TIM1_CC2 #18 | US1_CLK #18 | MODEM_DCLK #20 | PRS_CH6 #14 |
| | | TIM1_CC3 #17 | US1_CS #17 | MODEM_DIN #19 | ACMP0_O #20 |
| | | WTIM0_CDTI0 #28 | US1_CTS #16 | MODEM_DOUT #18 | ACMP1_O #20 |
| | | WTIM0_CDTI1 #26 | US1_RTS #15 | | LES_CH4 |
| | | WTIM0_CDTI2 #24 | LEU0_TX #20 | | |
| | | LETIM0_OUT0 #20 | LEU0_RX #19 | | |
| | | LETIM0_OUT1 #19 | I2C0_SDA #20 | | |
| | | PCNT0_S0IN #20 | I2C0_SCL #19 | | |
| | | PCNT0_S1IN #19 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PD13 | VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P | TIM0_CC0 #21 | US0_TX #21 | | |
| | | TIM0_CC1 #20 | US0_RX #20 | | |
| | | TIM0_CC2 #19 | US0_CLK #19 | | |
| | | TIM0_CDTI0 #18 | US0_CS #18 | | |
| | | TIM0_CDTI1 #17 | US0_CTS #17 | | |
| | | TIM0_CDTI2 #16 | US0_RTS #16 | FRC_DCLK #21 | PRS_CH3 #12 |
| | | TIM1_CC0 #21 | US1_TX #21 | FRC_DOUT #20 | PRS_CH4 #4 |
| | | TIM1_CC1 #20 | US1_RX #20 | FRC_DFRAME #19 | PRS_CH5 #3 |
| | | TIM1_CC2 #19 | US1_CLK #19 | MODEM_DCLK #21 | PRS_CH6 #15 |
| | | TIM1_CC3 #18 | US1_CS #18 | MODEM_DIN #20 | ACMP0_O #21 |
| | | WTIM0_CDTI0 #29 | US1_CTS #17 | MODEM_DOUT #19 | ACMP1_O #21 |
| | | WTIM0_CDTI1 #27 | US1_RTS #16 | | LES_CH5 |
| | | WTIM0_CDTI2 #25 | LEU0_TX #21 | | |
| | | LETIM0_OUT0 #21 | LEU0_RX #20 | | |
| | | LETIM0_OUT1 #20 | I2C0_SDA #21 | | |
| | | PCNT0_S0IN #21 | I2C0_SCL #20 | | |
| | | PCNT0_S1IN #20 | | | |
| PD14 | BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT | TIM0_CC0 #22 | US0_TX #22 | | |
| | | TIM0_CC1 #21 | US0_RX #21 | | |
| | | TIM0_CC2 #20 | US0_CLK #20 | | |
| | | TIM0_CDTI0 #19 | US0_CS #19 | | |
| | | TIM0_CDTI1 #18 | US0_CTS #18 | | CMU_CLK0 #5 |
| | | TIM0_CDTI2 #17 | US0_RTS #17 | FRC_DCLK #22 | PRS_CH3 #13 |
| | | TIM1_CC0 #22 | US1_TX #22 | FRC_DOUT #21 | PRS_CH4 #5 |
| | | TIM1_CC1 #21 | US1_RX #21 | FRC_DFRAME #20 | PRS_CH5 #4 |
| | | TIM1_CC2 #20 | US1_CLK #20 | MODEM_DCLK #22 | PRS_CH6 #16 |
| | | TIM1_CC3 #19 | US1_CS #19 | MODEM_DIN #21 | ACMP0_O #22 |
| | | WTIM0_CDTI0 #30 | US1_CTS #18 | MODEM_DOUT #20 | ACMP1_O #22 |
| | | WTIM0_CDTI1 #28 | US1_RTS #17 | | LES_CH6 |
| | | WTIM0_CDTI2 #26 | LEU0_TX #22 | | GPIO_EM4WU4 |
| | | LETIM0_OUT0 #22 | LEU0_RX #21 | | |
| | | LETIM0_OUT1 #21 | I2C0_SDA #22 | | |
| | | PCNT0_S0IN #22 | I2C0_SCL #21 | | |
| | | PCNT0_S1IN #21 | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|-----------------|---------------|-------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other | |
| PD15 | VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N | TIM0_CC0 #23 | US0_TX #23 | | | |
| | | TIM0_CC1 #22 | US0_RX #22 | | | |
| | | TIM0_CC2 #21 | US0_CLK #21 | | | |
| | | TIM0_CDTI0 #20 | US0_CS #20 | | | |
| | | TIM0_CDTI1 #19 | US0_CTS #19 | | FRC_DCLK #23 | CMU_CLK1 #5 |
| | | TIM0_CDTI2 #18 | US0_RTS #18 | | FRC_DOUT #22 | PRS_CH3 #14 |
| | | TIM1_CC0 #23 | US1_TX #23 | | FRC_DFRAME #21 | PRS_CH4 #6 |
| | | TIM1_CC1 #22 | US1_RX #22 | | MODEM_DCLK #23 | PRS_CH5 #5 |
| | | TIM1_CC2 #21 | US1_CLK #21 | | MODEM_DIN #22 | PRS_CH6 #17 |
| | | TIM1_CC3 #20 | US1_CS #20 | | MODEM_DOUT #21 | ACMP0_O #23 |
| | | WTIM0_CDTI0 #31 | US1_CTS #19 | | | ACMP1_O #23 |
| | | WTIM0_CDTI1 #29 | US1_RTS #18 | | | LES_CH7 |
| | | WTIM0_CDTI2 #27 | LEU0_TX #23 | | | DBG_SWO #2 |
| | | LETIM0_OUT0 #23 | LEU0_RX #22 | | | |
| | | LETIM0_OUT1 #22 | I2C0_SDA #23 | | | |
| | | PCNT0_S0IN #23 | I2C0_SCL #22 | | | |
| | | PCNT0_S1IN #22 | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------------|-----------------|-------------|----------------|--------------|
| | Analog | Timers | Communication | Radio | Other | |
| PF0 | BUSBY BUSAX | | US0_TX #24 | | | |
| | | | US0_RX #23 | | | |
| | | | US0_CLK #22 | | | |
| | | | TIM0_CC0 #24 | US0_CS #21 | | |
| | | | TIM0_CC1 #23 | US0_CTS #20 | | |
| | | | TIM0_CC2 #22 | US0_RTS #19 | | |
| | | | TIM0_CDTI0 #21 | US1_TX #24 | | |
| | | | TIM0_CDTI1 #20 | US1_RX #23 | | PRS_CH0 #0 |
| | | | TIM0_CDTI2 #19 | US1_CLK #22 | FRC_DCLK #24 | PRS_CH1 #7 |
| | | | TIM1_CC0 #24 | US1_CS #21 | FRC_DOUT #23 | PRS_CH2 #6 |
| | | | TIM1_CC1 #23 | US1_CTS #20 | FRC_DFRAME #22 | PRS_CH3 #5 |
| | | | TIM1_CC2 #22 | US1_RTS #19 | MODEM_DCLK #24 | ACMP0_O #24 |
| | | | TIM1_CC3 #21 | US2_TX #14 | MODEM_DIN #23 | ACMP1_O #24 |
| | | | WTIM0_CDTI1 #30 | US2_RX #13 | MODEM_DOUT #22 | DBG_SWCLKTCK |
| | | | WTIM0_CDTI2 #28 | US2_CLK #12 | | BOOT_TX |
| | | | LETIM0_OUT0 #24 | US2_CS #11 | | |
| | | | LETIM0_OUT1 #23 | US2_CTS #10 | | |
| | | | PCNT0_S0IN #24 | US2_RTS #9 | | |
| | | | PCNT0_S1IN #23 | LEU0_TX #24 | | |
| | | | | LEU0_RX #23 | | |
| | | I2C0_SDA #24 | | | | |
| | | I2C0_SCL #23 | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------------|-----------------|-------------|----------------|--------------|
| | Analog | Timers | Communication | Radio | Other | |
| PF1 | BUSAY BUSBX | | US0_TX #25 | | | |
| | | | US0_RX #24 | | | |
| | | | US0_CLK #23 | | | |
| | | | TIM0_CC0 #25 | US0_CS #22 | | |
| | | | TIM0_CC1 #24 | US0_CTS #21 | | |
| | | | TIM0_CC2 #23 | US0_RTS #20 | | |
| | | | TIM0_CDTI0 #22 | US1_TX #25 | | |
| | | | TIM0_CDTI1 #21 | US1_RX #24 | | PRS_CH0 #1 |
| | | | TIM0_CDTI2 #20 | US1_CLK #23 | FRC_DCLK #25 | PRS_CH1 #0 |
| | | | TIM1_CC0 #25 | US1_CS #22 | FRC_DOUT #24 | PRS_CH2 #7 |
| | | | TIM1_CC1 #24 | US1_CTS #21 | FRC_DFRAME #23 | PRS_CH3 #6 |
| | | | TIM1_CC2 #23 | US1_RTS #20 | MODEM_DCLK #25 | ACMP0_O #25 |
| | | | TIM1_CC3 #22 | US2_TX #15 | MODEM_DIN #24 | ACMP1_O #25 |
| | | | WTIM0_CDTI1 #31 | US2_RX #14 | MODEM_DOUT #23 | DBG_SWDIOTMS |
| | | | WTIM0_CDTI2 #29 | US2_CLK #13 | | BOOT_RX |
| | | | LETIM0_OUT0 #25 | US2_CS #12 | | |
| | | | LETIM0_OUT1 #24 | US2_CTS #11 | | |
| | | | PCNT0_S0IN #25 | US2_RTS #10 | | |
| | | | PCNT0_S1IN #24 | LEU0_TX #25 | | |
| | | | | LEU0_RX #24 | | |
| | | I2C0_SDA #25 | | | | |
| | | I2C0_SCL #24 | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------|---------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other |
| PF2 | BUSBY BUSAX | TIM0_CC0 #26 | US0_TX #26 | | |
| | | TIM0_CC1 #25 | US0_RX #25 | | |
| | | TIM0_CC2 #24 | US0_CLK #24 | | |
| | | TIM0_CDTI0 #23 | US0_CS #23 | | CMU_CLK0 #6 |
| | | TIM0_CDTI1 #22 | US0_CTS #22 | | PRS_CH0 #2 |
| | | TIM0_CDTI2 #21 | US0_RTS #21 | FRC_DCLK #26 | PRS_CH1 #1 |
| | | TIM1_CC0 #26 | US1_TX #26 | FRC_DOUT #25 | PRS_CH2 #0 |
| | | TIM1_CC1 #25 | US1_RX #25 | FRC_DFRAME #24 | PRS_CH3 #7 |
| | | TIM1_CC2 #24 | US1_CLK #24 | MODEM_DCLK #26 | ACMP0_O #26 |
| | | TIM1_CC3 #23 | US1_CS #23 | MODEM_DIN #25 | ACMP1_O #26 |
| | | WTIM0_CDTI2 #30 | US1_CTS #22 | MODEM_DOUT #24 | DBG_TDO |
| | | LETIM0_OUT0 #26 | US1_RTS #21 | | DBG_SWO #0 |
| | | LETIM0_OUT1 #25 | LEU0_TX #26 | | GPIO_EM4WU0 |
| | | PCNT0_S0IN #26 | LEU0_RX #25 | | |
| | | PCNT0_S1IN #25 | I2C0_SDA #26 | | |
| | | | I2C0_SCL #25 | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------|-----------------|--------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other | |
| PF3 | BUSAY BUSBX | | US0_TX #27 | | | |
| | | | US0_RX #26 | | | |
| | | | US0_CLK #25 | | | |
| | | | US0_CS #24 | | | |
| | | | TIM0_CC0 #27 | US0_CTS #23 | | |
| | | | TIM0_CC1 #26 | US0_RTS #22 | | |
| | | | TIM0_CC2 #25 | US1_TX #27 | | |
| | | | TIM0_CDTI0 #24 | US1_RX #26 | | CMU_CLK1 #6 |
| | | | TIM0_CDTI1 #23 | US1_CLK #25 | FRC_DCLK #27 | PRS_CH0 #3 |
| | | | TIM0_CDTI2 #22 | US1_CS #24 | FRC_DOUT #26 | PRS_CH1 #2 |
| | | | TIM1_CC0 #27 | US1_CTS #23 | FRC_DFRAME #25 | PRS_CH2 #1 |
| | | | TIM1_CC1 #26 | US1_RTS #22 | MODEM_DCLK #27 | PRS_CH3 #0 |
| | | | TIM1_CC2 #25 | US2_TX #16 | MODEM_DIN #26 | ACMP0_O #27 |
| | | | TIM1_CC3 #24 | US2_RX #15 | MODEM_DOUT #25 | ACMP1_O #27 |
| | | | WTIM0_CDTI2 #31 | US2_CLK #14 | | DBG_TDI |
| | | | LETIM0_OUT0 #27 | US2_CS #13 | | |
| | | | LETIM0_OUT1 #26 | US2_CTS #12 | | |
| | | | PCNT0_S0IN #27 | US2_RTS #11 | | |
| | | | PCNT0_S1IN #26 | LEU0_TX #27 | | |
| | | | | LEU0_RX #26 | | |
| | | | | I2C0_SDA #27 | | |
| | | | | I2C0_SCL #26 | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------------|-----------------|-------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other | |
| PF4 | BUSBY BUSAX | | US0_TX #28 | | | |
| | | | US0_RX #27 | | | |
| | | | US0_CLK #26 | | | |
| | | | US0_CS #25 | | | |
| | | | TIM0_CC0 #28 | US0_CTS #24 | | |
| | | | TIM0_CC1 #27 | US0_RTS #23 | | |
| | | | TIM0_CC2 #26 | US1_TX #28 | | |
| | | | TIM0_CDTI0 #25 | US1_RX #27 | | |
| | | | TIM0_CDTI1 #24 | US1_CLK #26 | FRC_DCLK #28 | PRS_CH0 #4 |
| | | | TIM0_CDTI2 #23 | US1_CS #25 | FRC_DOUT #27 | PRS_CH1 #3 |
| | | | TIM1_CC0 #28 | US1_CTS #24 | FRC_DFRAME #26 | PRS_CH2 #2 |
| | | | TIM1_CC1 #27 | US1_RTS #23 | MODEM_DCLK #28 | PRS_CH3 #1 |
| | | | TIM1_CC2 #26 | US2_TX #17 | MODEM_DIN #27 | ACMP0_O #28 |
| | | | TIM1_CC3 #25 | US2_RX #16 | MODEM_DOUT #26 | ACMP1_O #28 |
| | | | LETIM0_OUT0 #28 | US2_CLK #15 | | |
| | | | LETIM0_OUT1 #27 | US2_CS #14 | | |
| | | | PCNT0_S0IN #28 | US2_CTS #13 | | |
| | | | PCNT0_S1IN #27 | US2_RTS #12 | | |
| | | | | LEU0_TX #28 | | |
| | | | | LEU0_RX #27 | | |
| | | I2C0_SDA #28 | | | | |
| | | I2C0_SCL #27 | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------------|-----------------|-------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other | |
| PF5 | BUSAY BUSBX | | US0_TX #29 | | | |
| | | | US0_RX #28 | | | |
| | | | US0_CLK #27 | | | |
| | | | US0_CS #26 | | | |
| | | | TIM0_CC0 #29 | US0_CTS #25 | | |
| | | | TIM0_CC1 #28 | US0_RTS #24 | | |
| | | | TIM0_CC2 #27 | US1_TX #29 | | |
| | | | TIM0_CDTI0 #26 | US1_RX #28 | | |
| | | | TIM0_CDTI1 #25 | US1_CLK #27 | FRC_DCLK #29 | PRS_CH0 #5 |
| | | | TIM0_CDTI2 #24 | US1_CS #26 | FRC_DOUT #28 | PRS_CH1 #4 |
| | | | TIM1_CC0 #29 | US1_CTS #25 | FRC_DFRAME #27 | PRS_CH2 #3 |
| | | | TIM1_CC1 #28 | US1_RTS #24 | MODEM_DCLK #29 | PRS_CH3 #2 |
| | | | TIM1_CC2 #27 | US2_TX #18 | MODEM_DIN #28 | ACMP0_O #29 |
| | | | TIM1_CC3 #26 | US2_RX #17 | MODEM_DOUT #27 | ACMP1_O #29 |
| | | | LETIM0_OUT0 #29 | US2_CLK #16 | | |
| | | | LETIM0_OUT1 #28 | US2_CS #15 | | |
| | | | PCNT0_S0IN #29 | US2_CTS #14 | | |
| | | | PCNT0_S1IN #28 | US2_RTS #13 | | |
| | | | | LEU0_TX #29 | | |
| | | | | LEU0_RX #28 | | |
| | | I2C0_SDA #29 | | | | |
| | | I2C0_SCL #28 | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------------|-----------------|-------------|----------------|-------------|
| | Analog | Timers | Communication | Radio | Other | |
| PF6 | BUSBY BUSAX | | US0_TX #30 | | | |
| | | | US0_RX #29 | | | |
| | | | US0_CLK #28 | | | |
| | | | US0_CS #27 | | | |
| | | | TIM0_CC0 #30 | US0_CTS #26 | | |
| | | | TIM0_CC1 #29 | US0_RTS #25 | | |
| | | | TIM0_CC2 #28 | US1_TX #30 | | |
| | | | TIM0_CDTI0 #27 | US1_RX #29 | | |
| | | | TIM0_CDTI1 #26 | US1_CLK #28 | FRC_DCLK #30 | CMU_CLK1 #7 |
| | | | TIM0_CDTI2 #25 | US1_CS #27 | FRC_DOUT #29 | PRS_CH0 #6 |
| | | | TIM1_CC0 #30 | US1_CTS #26 | FRC_DFRAME #28 | PRS_CH1 #5 |
| | | | TIM1_CC1 #29 | US1_RTS #25 | MODEM_DCLK #30 | PRS_CH2 #4 |
| | | | TIM1_CC2 #28 | US2_TX #19 | MODEM_DIN #29 | PRS_CH3 #3 |
| | | | TIM1_CC3 #27 | US2_RX #18 | MODEM_DOUT #28 | ACMP0_O #30 |
| | | | LETIM0_OUT0 #30 | US2_CLK #17 | | ACMP1_O #30 |
| | | | LETIM0_OUT1 #29 | US2_CS #16 | | |
| | | | PCNT0_S0IN #30 | US2_CTS #15 | | |
| | | | PCNT0_S1IN #29 | US2_RTS #14 | | |
| | | | | LEU0_TX #30 | | |
| | | | | LEU0_RX #29 | | |
| | | I2C0_SDA #30 | | | | |
| | | I2C0_SCL #29 | | | | |

| GPIO Name | Pin Alternate Functionality / Description | | | | | |
|-----------|---|--------------|-----------------|-------------|----------------|--------------|
| | Analog | Timers | Communication | Radio | Other | |
| PF7 | BUSAY BUSBX | | US0_TX #31 | | | |
| | | | US0_RX #30 | | | |
| | | | US0_CLK #29 | | | |
| | | | US0_CS #28 | | | |
| | | | TIM0_CC0 #31 | US0_CTS #27 | | |
| | | | TIM0_CC1 #30 | US0_RTS #26 | | |
| | | | TIM0_CC2 #29 | US1_TX #31 | | CMU_CLKI0 #1 |
| | | | TIM0_CDTI0 #28 | US1_RX #30 | | CMU_CLK0 #7 |
| | | | TIM0_CDTI1 #27 | US1_CLK #29 | FRC_DCLK #31 | PRS_CH0 #7 |
| | | | TIM0_CDTI2 #26 | US1_CS #28 | FRC_DOUT #30 | PRS_CH1 #6 |
| | | | TIM1_CC0 #31 | US1_CTS #27 | FRC_DFRAME #29 | PRS_CH2 #5 |
| | | | TIM1_CC1 #30 | US1_RTS #26 | MODEM_DCLK #31 | PRS_CH3 #4 |
| | | | TIM1_CC2 #29 | US2_TX #20 | MODEM_DIN #30 | ACMP0_O #31 |
| | | | TIM1_CC3 #28 | US2_RX #19 | MODEM_DOUT #29 | ACMP1_O #31 |
| | | | LETIM0_OUT0 #31 | US2_CLK #18 | | GPIO_EM4WU1 |
| | | | LETIM0_OUT1 #30 | US2_CS #17 | | |
| | | | PCNT0_S0IN #31 | US2_CTS #16 | | |
| | | | PCNT0_S1IN #30 | US2_RTS #15 | | |
| | | | | LEU0_TX #31 | | |
| | | | | LEU0_RX #30 | | |
| | | I2C0_SDA #31 | | | | |
| | | I2C0_SCL #30 | | | | |

6.3 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to [6.2 GPIO Functionality Table](#) for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.3. Alternate Functionality Overview

| Alternate Functionality | LOCATION | | | | | | | | Description |
|----------------------------|--|--|---|---|---|--|--|--|---|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| ACMP0_O | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Analog comparator ACMP0, digital output. |
| ACMP1_O | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Analog comparator ACMP1, digital output. |
| ADC0_EXTN | 0: PA0 | | | | | | | | Analog to digital converter ADC0 external reference input negative pin. |
| ADC0_EXTP | 0: PA1 | | | | | | | | Analog to digital converter ADC0 external reference input positive pin. |
| BOOT_RX | 0: PF1 | | | | | | | | Bootloader RX. |
| BOOT_TX | 0: PF0 | | | | | | | | Bootloader TX. |
| CMU_CLK0 | 0: PA1 1: PB15 2: PC6 3: PC11 | 4: PD9 5: PD14 6: PF2 7: PF7 | | | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | 0: PA0 1: PB14 2: PC7 3: PC10 | 4: PD10 5: PD15 6: PF3 7: PF6 | | | | | | | Clock Management Unit, clock output number 1. |
| CMU_CLKI0 | 0: PB13 1: PF7 2: PC6 | 4: PA5 | | | | | | | Clock Management Unit, clock input number 0. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|-------|--------|---------|---------|---------|---------|---------|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| DBG_SWCLKTCK | 0: PF0 | | | | | | | | <p>Debug-interface Serial Wire clock input and JTAG Test Clock.</p> <p>Note that this function is enabled to the pin out of reset, and has a built-in pull down.</p> |
| DBG_SWDIOTMS | 0: PF1 | | | | | | | | <p>Debug-interface Serial Wire data input / output and JTAG Test Mode Select.</p> <p>Note that this function is enabled to the pin out of reset, and has a built-in pull up.</p> |
| DBG_SWO | 0: PF2 1: PB13 2: PD15 3: PC11 | | | | | | | | <p>Debug-interface Serial Wire viewer Output.</p> <p>Note that this function is not enabled after reset, and must be enabled by software to be used.</p> |
| DBG_TDI | 0: PF3 | | | | | | | | <p>Debug-interface JTAG Test Data In.</p> <p>Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.</p> |
| DBG_TDO | 0: PF2 | | | | | | | | <p>Debug-interface JTAG Test Data Out.</p> <p>Note that this function becomes available after the first valid JTAG command is received.</p> |
| ETM_TCLK | 1: PA5 3: PC6 | | | | | | | | Embedded Trace Module ETM clock . |
| ETM_TDO | 3: PC7 | | | | | | | | Embedded Trace Module ETM data 0. |

| Alternate | LOCATION | | | | | | | | Description |
|--------------|--------------------------------------|--|---|--|--|--|--|--|--|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| ETM_TD1 | 3: PC8 | | | | | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | 3: PC9 | | | | | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | 3: PC10 | | | | | | | | Embedded Trace Module ETM data 3. |
| FRC_DCLK | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Frame Controller, Data Sniffer Clock. |
| FRC_DFRAME | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | Frame Controller, Data Sniffer Frame active |
| FRC_DOUT | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Frame Controller, Data Sniffer Output. |
| GPIO_EM4WU0 | 0: PF2 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | 0: PF7 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | 0: PD14 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU8 | 0: PA3 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU9 | 0: PB13 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU12 | 0: PC10 | | | | | | | | Pin can be used to wake the system up from EM4 |
| I2C0_SCL | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | I2C0 Serial Clock Line input / output. |

| Alternate | LOCATION | | | | | | | | |
|---------------|--------------------------------------|---|--|--|---|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| I2C0_SDA | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | I2C0 Serial Data input / output. |
| I2C1_SCL | | | | | 18: PC10 19: PC11 | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | | | | | 19: PC10 | 20: PC11 | | | I2C1 Serial Data input / output. |
| LES_CH1 | 0: PD9 | | | | | | | | LESENSE channel 1. |
| LES_CH2 | 0: PD10 | | | | | | | | LESENSE channel 2. |
| LES_CH3 | 0: PD11 | | | | | | | | LESENSE channel 3. |
| LES_CH4 | 0: PD12 | | | | | | | | LESENSE channel 4. |
| LES_CH5 | 0: PD13 | | | | | | | | LESENSE channel 5. |
| LES_CH6 | 0: PD14 | | | | | | | | LESENSE channel 6. |
| LES_CH7 | 0: PD15 | | | | | | | | LESENSE channel 7. |
| LES_CH8 | 0: PA0 | | | | | | | | LESENSE channel 8. |
| LES_CH9 | 0: PA1 | | | | | | | | LESENSE channel 9. |
| LES_CH10 | 0: PA2 | | | | | | | | LESENSE channel 10. |
| LES_CH11 | 0: PA3 | | | | | | | | LESENSE channel 11. |
| LES_CH12 | 0: PA4 | | | | | | | | LESENSE channel 12. |
| LES_CH13 | 0: PA5 | | | | | | | | LESENSE channel 13. |
| LETIM0_OUT0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Low Energy Timer LETIM0, output channel 1. |

| Alternate | LOCATION | | | | | | | | |
|---------------|--------------------------------------|--|---|--|--|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| LEU0_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | LEUART0 Receive input. |
| LEU0_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| MODEM_DCLK | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | MODEM data clock out. |
| MODEM_DIN | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | MODEM data in. |
| MODEM_DOUT | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | MODEM data out. |
| OPA0_N | 0: PA4 | | | | | | | | Operational Amplifier 0 external negative input. |
| OPA0_P | 0: PA2 | | | | | | | | Operational Amplifier 0 external positive input. |
| OPA1_N | 0: PD15 | | | | | | | | Operational Amplifier 1 external negative input. |
| OPA1_P | 0: PD13 | | | | | | | | Operational Amplifier 1 external positive input. |
| OPA2_N | 0: PB13 | | | | | | | | Operational Amplifier 2 external negative input. |
| OPA2_OUT | 0: PB12 | | | | | | | | Operational Amplifier 2 output. |
| OPA2_P | 0: PB11 | | | | | | | | Operational Amplifier 2 external positive input. |

| Alternate | LOCATION | | | | | | | | |
|---------------|--|---|---|--|---|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PCNT0_S0IN | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | 0: PF0 1: PF1 2: PF2 3: PF3 | 4: PF4 5: PF5 6: PF6 7: PF7 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | 0: PF1 1: PF2 2: PF3 3: PF4 | 4: PF5 5: PF6 6: PF7 7: PF0 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | 0: PF2 1: PF3 2: PF4 3: PF5 | 4: PF6 5: PF7 6: PF0 7: PF1 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | 0: PF3 1: PF4 2: PF5 3: PF6 | 4: PF7 5: PF0 6: PF1 7: PF2 | 8: PD9 9: PD10 10: PD11 11: PD12 | 12: PD13 13: PD14 14: PD15 | | | | | Peripheral Reflex System PRS, channel 3. |
| PRS_CH4 | 0: PD9 1: PD10 2: PD11 3: PD12 | 4: PD13 5: PD14 6: PD15 | | | | | | | Peripheral Reflex System PRS, channel 4. |
| PRS_CH5 | 0: PD10 1: PD11 2: PD12 3: PD13 | 4: PD14 5: PD15 6: PD9 | | | | | | | Peripheral Reflex System PRS, channel 5. |
| PRS_CH6 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PD9 | 12: PD10 13: PD11 14: PD12 15: PD13 | 16: PD14 17: PD15 | | | | Peripheral Reflex System PRS, channel 6. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---------------------------------------|--|---|---|--|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PRS_CH7 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PA0 | | | | | | Peripheral Reflex System PRS, channel 7. |
| PRS_CH8 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PA0 10: PA1 | | | | | | Peripheral Reflex System PRS, channel 8. |
| PRS_CH9 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PA0 9: PA1 10: PA2 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 | | | | Peripheral Reflex System PRS, channel 9. |
| PRS_CH10 | 0: PC6 1: PC7 2: PC8 3: PC9 | 4: PC10 5: PC11 | | | | | | | Peripheral Reflex System PRS, channel 10. |
| PRS_CH11 | 0: PC7 1: PC8 2: PC9 3: PC10 | 4: PC11 5: PC6 | | | | | | | Peripheral Reflex System PRS, channel 11. |
| TIM0_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDT10 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | Timer 0 Complimentary Dead Time Insertion channel 0. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|--|---|---|--|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| TIM0_CDT11 | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDT12 | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | Timer 1 Capture Compare input / output channel 2. |
| TIM1_CC3 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | Timer 1 Capture Compare input / output channel 3. |
| US0_CLK | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | USART0 clock input / output. |
| US0_CS | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | USART0 chip select input / output. |
| US0_CTS | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | USART0 Clear To Send hardware flow control input. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|--|---|---|--|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US0_RTS | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | USART0 Request To Send hardware flow control output. |
| US0_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | USART1 clock input / output. |
| US1_CS | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | USART1 chip select input / output. |
| US1_CTS | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | USART1 Clear To Send hardware flow control input. |
| US1_RTS | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | USART1 Request To Send hardware flow control output. |
| US1_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | | |
|---------------|--------------------------------------|--|---|---|---|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US1_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | | | | 12: PF0 13: PF1 14: PF3 15: PF4 | 16: PF5 17: PF6 18: PF7 | | | 30: PA5 | USART2 clock input / output. |
| US2_CS | | | 11: PF0 | 12: PF1 13: PF3 14: PF4 15: PF5 | 16: PF6 17: PF7 | | | 29: PA5 | USART2 chip select input / output. |
| US2_CTS | | | 10: PF0 11: PF1 | 12: PF3 13: PF4 14: PF5 15: PF6 | 16: PF7 | | | 28: PA5 | USART2 Clear To Send hardware flow control input. |
| US2_RTS | | | 9: PF0 10: PF1 11: PF3 | 12: PF4 13: PF5 14: PF6 15: PF7 | | | 27: PA5 | | USART2 Request To Send hardware flow control output. |
| US2_RX | | | | 13: PF0 14: PF1 15: PF3 | 16: PF4 17: PF5 18: PF6 19: PF7 | | | 31: PA5 | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | 0: PA5 | | | 14: PF0 15: PF1 | 16: PF3 17: PF4 18: PF5 19: PF6 | 20: PF7 | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| VDAC0_EXT | 0: PA1 | | | | | | | | Digital to analog converter VDACC0 external reference input pin. |

| Alternate | LOCATION | | | | | | | | |
|------------------------------|--------------------------------------|--|--|--|--|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| VDAC0_OUT0 / OPA0_OUT | 0: PA3 | | | | | | | | Digital to Analog Converter DAC0 output channel number 0. |
| VDAC0_OUT0ALT / OPA0_OUT-ALT | 0: PA5 1: PD13 2: PD15 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 0. |
| VDAC0_OUT1 / OPA1_OUT | 0: PD14 | | | | | | | | Digital to Analog Converter DAC0 output channel number 1. |
| VDAC0_OUT1ALT / OPA1_OUT-ALT | 0: PD12 1: PA2 2: PA4 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 1. |
| WTIM0_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 | | 15: PB11 | 16: PB12 17: PB13 18: PB14 19: PB15 | | 26: PC6 27: PC7 | 28: PC8 29: PC9 30: PC10 31: PC11 | Wide timer 0 Capture Compare input / output channel 0. |
| WTIM0_CC1 | 0: PA2 1: PA3 2: PA4 3: PA5 | | | 13: PB11 14: PB12 15: PB13 | 16: PB14 17: PB15 | | 24: PC6 25: PC7 26: PC8 27: PC9 | 28: PC10 29: PC11 31: PD9 | Wide timer 0 Capture Compare input / output channel 1. |
| WTIM0_CC2 | 0: PA4 1: PA5 | | 11: PB11 | 12: PB12 13: PB13 14: PB14 15: PB15 | | 22: PC6 23: PC7 | 24: PC8 25: PC9 26: PC10 27: PC11 | 29: PD9 30: PD10 31: PD11 | Wide timer 0 Capture Compare input / output channel 2. |
| WTIM0_CDTI0 | | 7: PB11 | 8: PB12 9: PB13 10: PB14 11: PB15 | | 18: PC6 19: PC7 | 20: PC8 21: PC9 22: PC10 23: PC11 | 25: PD9 26: PD10 27: PD11 | 28: PD12 29: PD13 30: PD14 31: PD15 | Wide timer 0 Complimentary Dead Time Insertion channel 0. |
| WTIM0_CDTI1 | | 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 | | 16: PC6 17: PC7 18: PC8 19: PC9 | 20: PC10 21: PC11 23: PD9 | 24: PD10 25: PD11 26: PD12 27: PD13 | 28: PD14 29: PD15 30: PF0 31: PF1 | Wide timer 0 Complimentary Dead Time Insertion channel 1. |
| WTIM0_CDTI2 | 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | | 14: PC6 15: PC7 | 16: PC8 17: PC9 18: PC10 19: PC11 | 21: PD9 22: PD10 23: PD11 | 24: PD12 25: PD13 26: PD14 27: PD15 | 28: PF0 29: PF1 30: PF2 31: PF3 | Wide timer 0 Complimentary Dead Time Insertion channel 2. |

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 6.4. Alternate Functionality Priority

| Alternate Functionality | Location | Priority |
|-------------------------|----------|------------|
| CMU_CLKI0 | 1: PF7 | High Speed |

6.4 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. [Figure 6.2 APORT Connection Diagram on page 105](#) shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

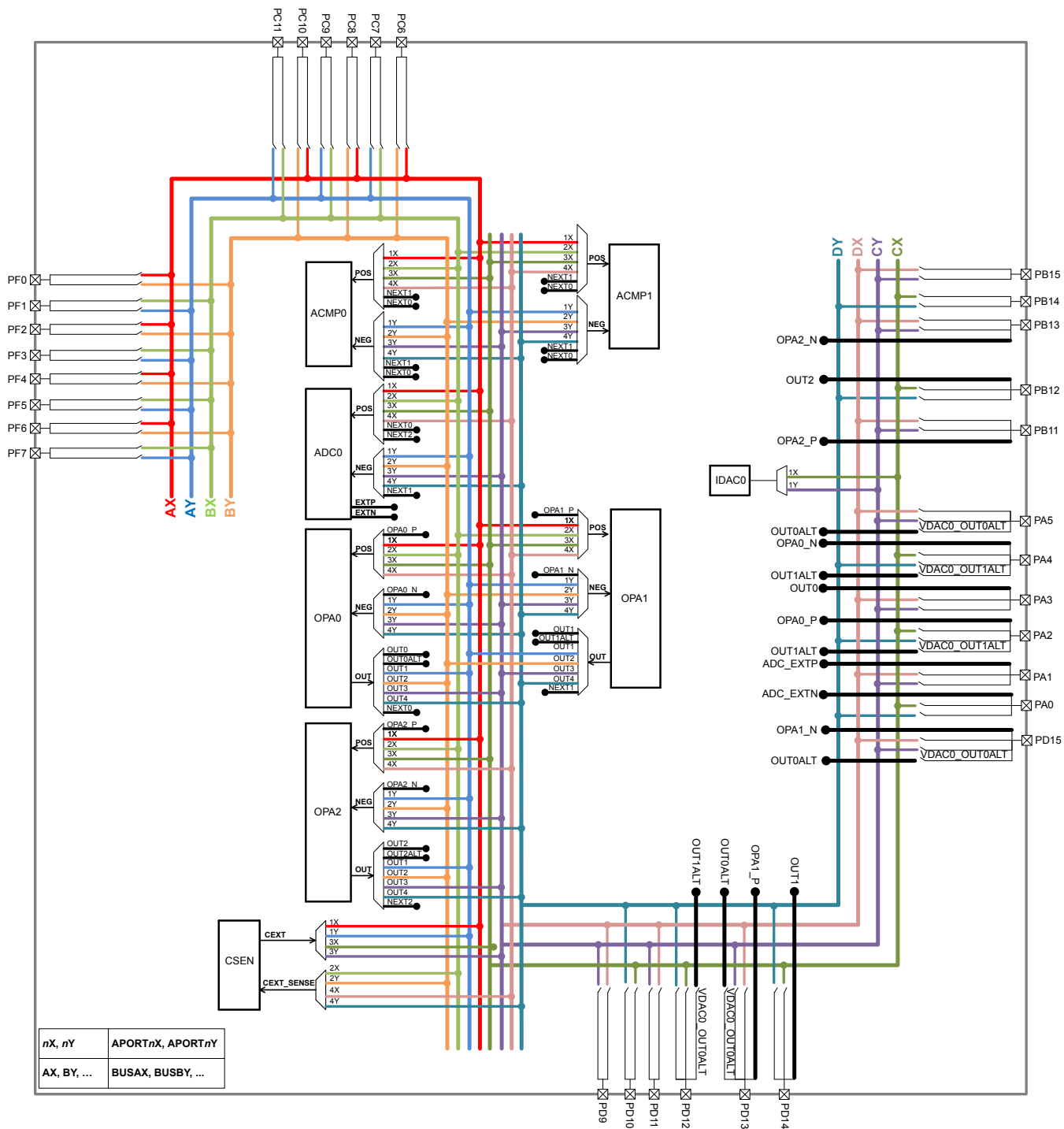


Figure 6.2. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.5. ACMP0 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | Port Bus |
|---------|---------|---------|---------|---------|---------|---------|---------|----------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | CH31 |
| PB14 | PB15 | PB15 | PB14 | | | | | CH30 |
| | PB13 | PB13 | | | | | | CH29 |
| PB12 | | | PB12 | | | | | CH28 |
| | PB11 | PB11 | | | | | | CH27 |
| | | | | | | | | CH26 |
| | | | | | | | | CH25 |
| | | | | | | | | CH24 |
| | | | | | PF7 | PF7 | | CH23 |
| | | | | PF6 | | | PF6 | CH22 |
| | | | | | PF5 | PF5 | | CH21 |
| | | | | PF4 | | | PF4 | CH20 |
| | | | | | PF3 | PF3 | | CH19 |
| | | | | PF2 | | | PF2 | CH18 |
| | | | | | PF1 | PF1 | | CH17 |
| | | | | PF0 | | | PF0 | CH16 |
| | | | | | | | | CH15 |
| | | | | | | | | CH14 |
| | PA5 | PA5 | | | | | | CH13 |
| PA4 | | | PA4 | | | | | CH12 |
| | PA3 | PA3 | | | PC11 | PC11 | | CH11 |
| PA2 | | | PA2 | PC10 | | | PC10 | CH10 |
| | PA1 | PA1 | | | PC9 | PC9 | | CH9 |
| PA0 | | | PA0 | PC8 | | | PC8 | CH8 |
| | PD15 | PD15 | | | PC7 | PC7 | | CH7 |
| PD14 | | | PD14 | PC6 | | | PC6 | CH6 |
| | PD13 | PD13 | | | | | | CH5 |
| PD12 | | | PD12 | | | | | CH4 |
| | PD11 | PD11 | | | | | | CH3 |
| PD10 | | | PD10 | | | | | CH2 |
| | PD9 | PD9 | | | | | | CH1 |
| | | | | | | | | CH0 |

Table 6.6. ACMP1 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | Bus |
| | PB15 | PB15 | | | | | | CH31 |
| | | | PB14 | | | | | CH30 |
| | PB13 | PB13 | | | | | | CH29 |
| | | | PB12 | | | | | CH28 |
| | PB11 | PB11 | | | | | | CH27 |
| | | | | | | | | CH26 |
| | | | | | | | | CH25 |
| | | | | | | | | CH24 |
| | | | | | PF7 | PF7 | | CH23 |
| | | | | PF6 | | | PF6 | CH22 |
| | | | | | PF5 | PF5 | | CH21 |
| | | | | | | | | CH20 |
| | | | | PF4 | | | PF4 | CH19 |
| | | | | | PF3 | PF3 | | CH18 |
| | | | | PF2 | | | PF2 | CH17 |
| | | | | | PF1 | PF1 | | CH16 |
| | | | | PF0 | | | PF0 | CH15 |
| | | | | | | | | CH14 |
| | | | | | | | | CH13 |
| | PA5 | PA5 | | | | | | CH12 |
| PA4 | | | PA4 | | | | | CH11 |
| | PA3 | PA3 | | | PC11 | PC11 | | CH10 |
| PA2 | | | PA2 | PC10 | | | PC10 | CH9 |
| | PA1 | PA1 | | | PC9 | PC9 | | CH8 |
| PA0 | | | PA0 | PC8 | | | PC8 | CH7 |
| | PD15 | PD15 | | | PC7 | PC7 | | CH6 |
| PD14 | | | PD14 | PC6 | | | PC6 | CH5 |
| | PD13 | PD13 | | | | | | CH4 |
| PD12 | | | PD12 | | | | | CH3 |
| | PD11 | PD11 | | | | | | CH2 |
| PD10 | | | PD10 | | | | | CH1 |
| | PD9 | PD9 | | | | | | CH0 |

Table 6.7. ADC0 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | Bus |
| | PB15 | PB15 | | | | | | CH31 |
| PB14 | | | PB14 | | | | | CH30 |
| | PB13 | PB13 | | | | | | CH29 |
| PB12 | | | PB12 | | | | | CH28 |
| | PB11 | PB11 | | | | | | CH27 |
| | | | | | | | | CH26 |
| | | | | | | | | CH25 |
| | | | | | | | | CH24 |
| | | | | | PF7 | PF7 | | CH23 |
| | | | | PF6 | | | PF6 | CH22 |
| | | | | | PF5 | PF5 | | CH21 |
| | | | | PF4 | | | PF4 | CH20 |
| | | | | | PF3 | PF3 | | CH19 |
| | | | | PF2 | | | PF2 | CH18 |
| | | | | | PF1 | PF1 | | CH17 |
| | | | | PF0 | | | PF0 | CH16 |
| | | | | | | | | CH15 |
| | | | | | | | | CH14 |
| | PA5 | PA5 | | | | | | CH13 |
| PA4 | | | PA4 | | | | | CH12 |
| | PA3 | PA3 | | | PC11 | PC11 | | CH11 |
| PA2 | | | PA2 | PC10 | | | PC10 | CH10 |
| | PA1 | PA1 | | | PC9 | PC9 | | CH9 |
| PA0 | | | PA0 | PC8 | | | PC8 | CH8 |
| | PD15 | PD15 | | | PC7 | PC7 | | CH7 |
| PD14 | | | PD14 | PC6 | | | PC6 | CH6 |
| | PD13 | PD13 | | | | | | CH5 |
| PD12 | | | PD12 | | | | | CH4 |
| | PD11 | PD11 | | | | | | CH3 |
| PD10 | | | PD10 | | | | | CH2 |
| | PD9 | PD9 | | | | | | CH1 |
| | | | | | | | | CH0 |

Table 6.10. VDAC0 / OPA Bus and Pin Mapping

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | |
|---------------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|-----|-----|--|
| OPA0_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | | PC9 | | PC7 | | | | | | | |
| APORT2Y | BUSBY | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | | PC8 | | PC6 | | | | | | |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | | |
| OPA0_P | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | | PC8 | | PC6 | | | | | | |
| APORT2X | BUSBX | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC6 | | | | | | |
| APORT3X | BUSCX | | PB14 | | PB12 | | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | | |

7. LGA64 Package Specifications

Refer to AN1223 for LGA Manufacturing Guidance.

7.1 LGA64 Package Dimensions

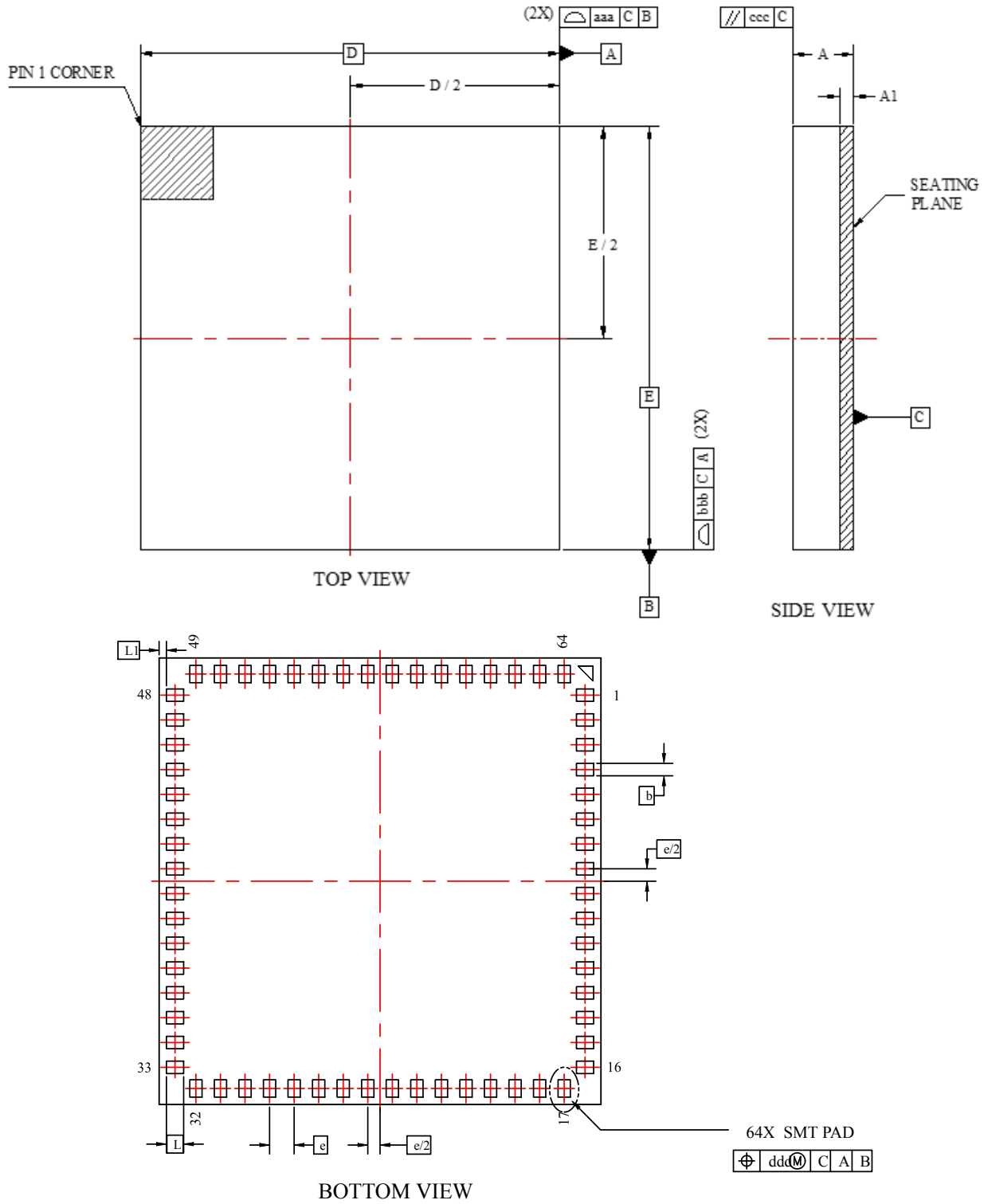


Figure 7.1. LGA64 Package Drawing

Table 7.1. LGA64 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 1.12 | 1.21 | 1.30 |
| A1 | 0.17 | 0.21 | 0.25 |
| b | 0.20 | 0.25 | 0.30 |
| D | 9.00 BSC | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| L | 0.30 | 0.35 | 0.40 |
| L1 | 0.10 | 0.15 | 0.20 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 LGA64 PCB Land Pattern

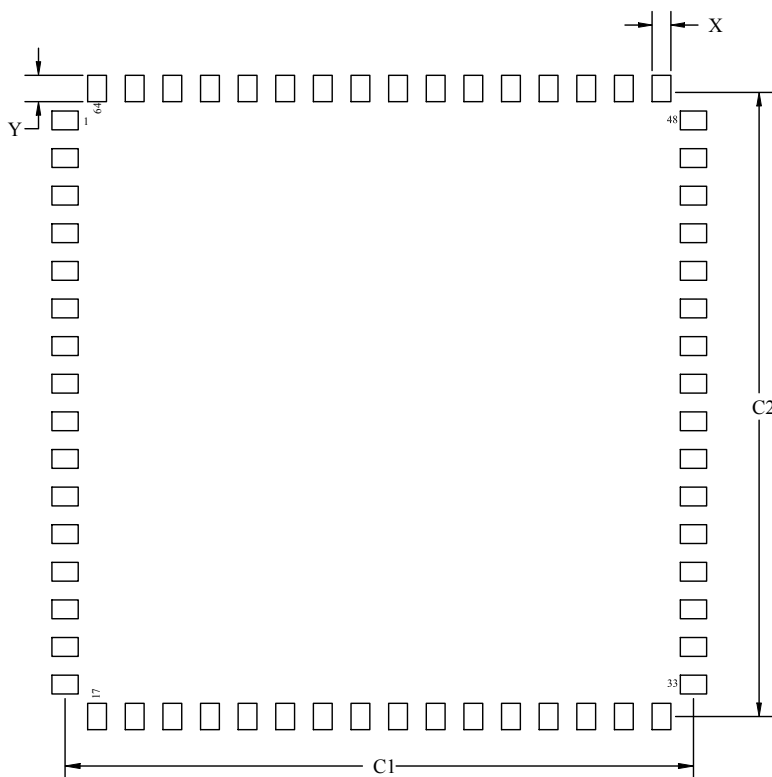


Figure 7.2. LGA64 PCB Land Pattern Drawing

Table 7.2. LGA64 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| C1 | 8.50 |
| C2 | 8.50 |
| X | 0.30 |
| Y | 0.35 |

Note:

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 LGA64 Package Marking

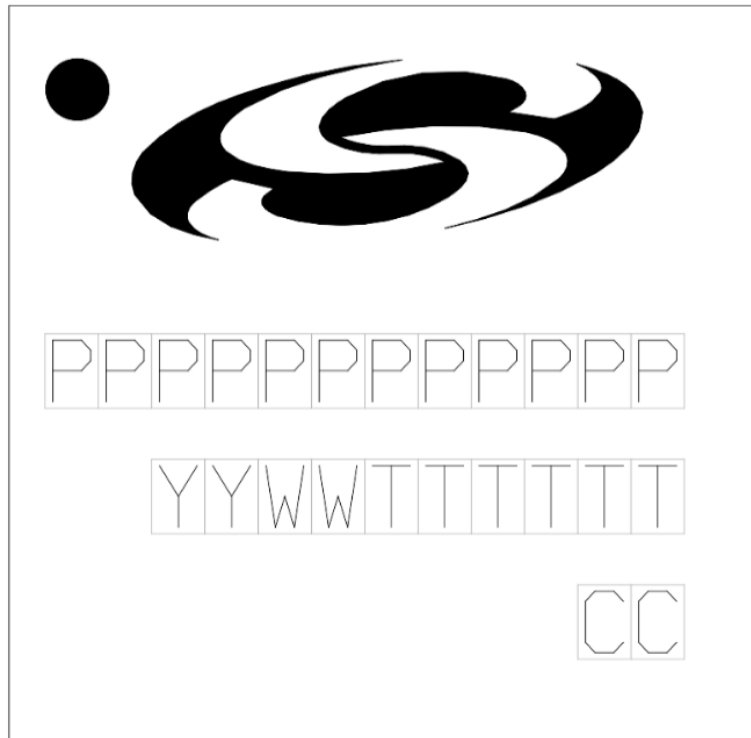


Figure 7.3. LGA64 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- C C – Country of Origin

8. Certifications

ZGM130S modules are not pre-certified and the end product containing this module should be certified for the respective regulatory body. Refer to AN1048 for detailed information related to Regulatory Certifications.

9. Revision History

Revision 1.2

December 2020

- Updated maximum TX power to 14 dBm.
- In [4.1.4.2 Current Consumption Using Radio 3.3 V with DC-DC](#) updated current consumptions for 912 MHz O-QPSK
- In [4.1.8.1 Sub-GHz RF Transmitter characteristics for 915 MHz Band](#)
 - Corrected FCC reference for non-restricted bands in :
 - SPURHARM_FCC_14
 - SPUROOB_FCC_14
 - Corrected FCC reference for PSD
- Added [4.1.8.2 Sub-GHz RF Transmitter characteristics for 915 MHz Band, +14 dBm](#) and other 912 MHz radio specs
- In [4.1.8.3 Sub-GHz RF Receiver Characteristics for 915 MHz Band](#), added sensitivity, image rejection, and blocking sensitivity for 912 MHz OQPSK PHY.
- Added reference to AN1223 in [7. LGA64 Package Specifications](#) section.
- In [7.3 LGA64 Package Marking](#) added package marking figure.
- Added [8. Certifications](#) section.

Revision 1.1

October 2019

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated [3.6.4 Low Energy Timer \(LETIMER\)](#) lowest energy mode.
- In [2. Ordering Information](#), updated ordering part numbers.

Revision 1.0

May 2019

- Added bullet about optional SAW filter to front page and feature lists.
- [Table 4.12 Sub-GHz RF Transmitter characteristics for 868 MHz Band on page 30](#) : Updated $POUT_{MAX}$ footnote with details about SAW insertion loss.
- [Table 4.9 Sub-GHz RF Transmitter characteristics for 915 MHz Band on page 25](#) : Updated $POUT_{MAX}$ footnote with details about SAW insertion loss.

Revision 0.5

January 2019

- Updated electrical characteristics with latest characterization results.

Revision 0.2

December 2018

- Crystal frequency changed to 39 MHz.
- Updated electrical characteristics with latest characterization estimates.
- [Table 4.9 Sub-GHz RF Transmitter characteristics for 915 MHz Band on page 25](#): PSD conditions updated to specify PSD at each data rate.
- [Table 6.3 Alternate Functionality Overview on page 93](#): Table formatting update.

Revision 0.1

August 2018

- Initial Release.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!



IoT Portfolio

www.silabs.com/IoT



SW/HW

www.silabs.com/simplicity



Quality

www.silabs.com/quality



Support & Community

www.silabs.com/community

Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required, or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, ClockBuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, ISOModem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>