ISL78227

2-Phase Boost Controller with Integrated Drivers

FN8808
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The ISL78227 is an automotive grade (AEC-Q100 Grade 1), 2-phase, 55V synchronous boost controller that simplifies the design of high power boost applications. It integrates strong half-bridge drivers, an analog/digital tracking input, and comprehensive protection functions.

The ISL78227 enables a simple, modular design for systems requiring power and thermal scalability. It offers peak-current mode control for fast line response and simple compensation. Its synchronous 2-phase architecture enables it to support higher current while reducing the size of input and output capacitors. The integrated drivers feature programmable adaptive dead time control offering flexibility in power stage design. The ISL78227 offers a 90° output clock and supports 1-, 2-, and 4-phases.

The ISL78227 offers a highly robust solution for the most demanding environments. Its unique soft-start control prevents large negative current even in extreme cases, such as a restart under high output pre-bias on high volume capacitances. It also offers two levels of cycle-by-cycle overcurrent protection, average current limiting, input OVP, output UVP/OVP, and internal OTP. In the event of a fault, the fault protection response can be selected to be latch-off or hiccup recovery.

Also integrated are several functions that ease system design. A unique tracking input controls the output voltage, allowing it to track either a digital duty cycle (PWM) signal or an analog reference. The ISL78227 provides input average current limiting so the system can deliver transient bursts of high load current while limiting the average current to avoid overheating.

Related Literature

For a full list of related documents, visit our website

- ISL78227 product page

Features

- Input/output voltage range: 5V to 55V, withstands 60V transients
- Supports synchronous or standard boost topology
- Peak current mode control with adjustable slope compensation
- Secondary average current control loop
- Integrated 5V 2A sourcing/3A sinking N-channel MOSFET drivers
- Switching frequency: 50kHz to 1.1MHz per phase
- External synchronization
- Programmable minimum duty cycle
- Programmable adaptive dead time control
- Optional diode emulation and phase dropping
- PWM and analog track function
- Forced PWM operation with negative current limiting and protection
- Comprehensive fault protections
- Selectable hiccup or latch-off fault response
- AEC-Q100 qualified, Grade 1: -40°C to +125°C
- 5mmx5mm 32 Ld Wettable Flank QFN (WFQFN) package

Applications

- Automotive power systems (12V to 24V, 12V to 48V, etc.)
  - Trunk audio amplifiers
  - Start-stop systems
  - Automotive boost applications
- Industrial and telecommunication power supplies

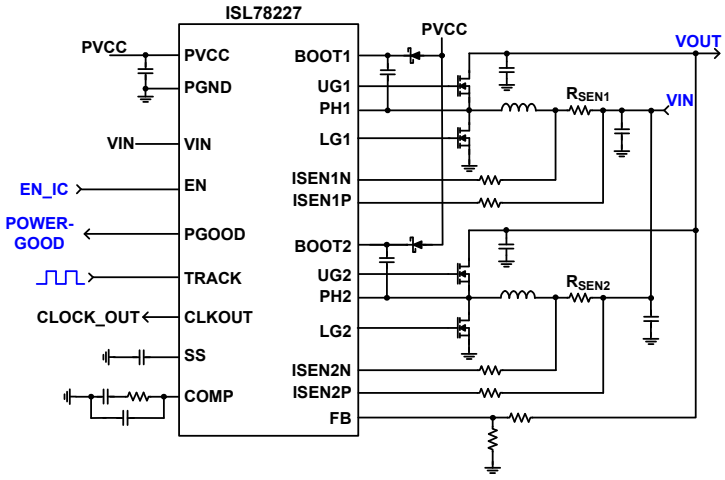
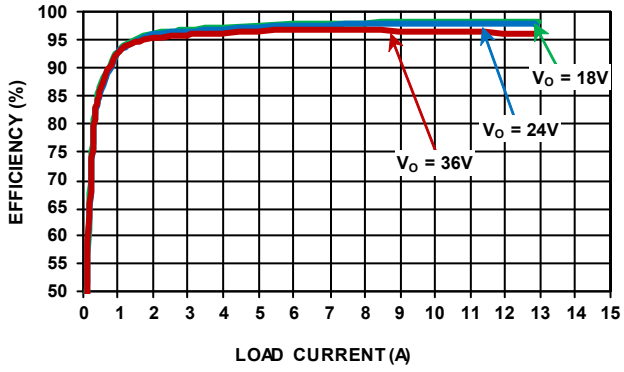


FIGURE 1. SIMPLIFIED APPLICATION SCHEMATIC, 2-PHASE SYNCHRONOUS BOOST



NOTE: (See Typical Application in Figure 4 on page 8.)

FIGURE 2. EFFICIENCY CURVES, V_{IN} = 12V, T_A = +25°C

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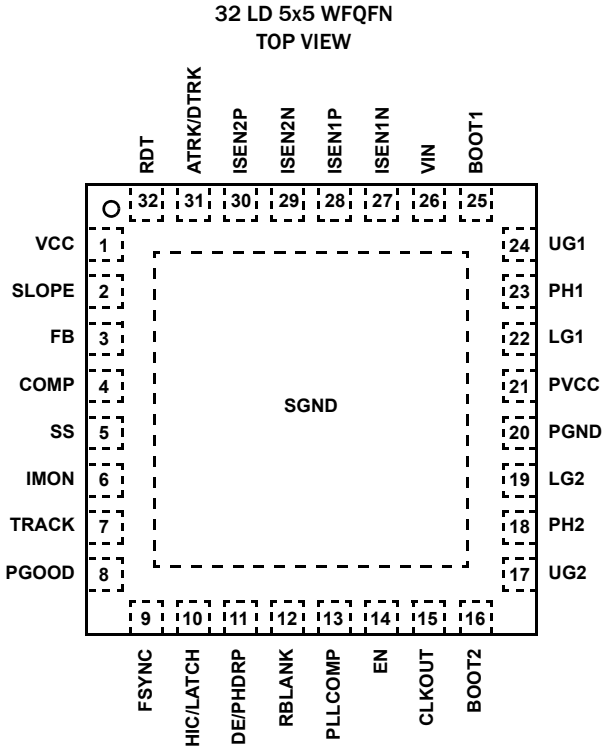
Pin Configuration



Functional Pin Description

PIN NAME	PIN #	DESCRIPTION
VCC	1	IC bias power input pin for the internal analog circuitry. Use a minimum 1µF ceramic capacitor between VCC and ground for noise decoupling purposes. VCC is typically biased by PVCC or an external bias supply with voltage ranging from 4.75V to 5.5V. Because PVCC provides pulsing drive current, a small resistor (10Ω or smaller) between PVCC and VCC can help filter out the noises from PVCC to VCC.
SLOPE	2	Programs the slope of the internal slope compensation. A resistor should be connected from the SLOPE pin to GND. Refer to "Adjustable Slope Compensation" on page 32 for information about how to select this resistor value.
FB	3	The inverting input of the error amplifier for the voltage regulation loop. A resistor network must be placed between the FB pin and the output rail to set the boost converter's output voltage. Refer to "Output Voltage Setting" on page 37 for more details. Output overvoltage and undervoltage comparators also monitor this pin. Refer to "Output Overvoltage Fault Protection" and "Output Undervoltage Indication" on page 34 for more details.
COMP	4	The output of the transconductance error amplifier (Gm1) for the output voltage regulation loop. Place the compensation network between the COMP pin and ground. Refer to "Output Voltage Regulation Loop" on page 25 for more details. The COMP pin voltage can also be controlled by the constant current control loop error amplifier (Gm2) output through a diode (D_{CC}) when the constant current control loop is used to control the input average current. Refer to "Constant Current Control (CC)" on page 35 for more details.
SS	5	A capacitor placed from SS to ground sets up the soft-start ramp rate and in turn, determines the soft-start time. Refer to "Soft-Start" on page 30 for more details.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
IMON	6	The average current monitor pin for the sum of the two phases' inductor currents. It is used for average current limiting and average current protection functions. The sourcing current from the IMON pin is the sum of the two CSA outputs plus a fixed 17µA offset current. With each CSA sensing individual phase's inductor current, the IMON signal represents the sum of the two phases' inductor currents and is the input current for the boost. Place a resistor in parallel with a capacitor from IMON to ground. The IMON pin output current signal builds up the average voltage signal representing the average current sense signals. A constant average current-limiting function and an average current protection are implemented based on the IMON signal. • Constant Current Control: A Constant Current (CC) control loop controls the IMON average current signal equal to a 1.6V reference (VREF_CC), which ultimately limits the total input average current to a constant level. • Average Current Protection: If the IMON pin voltage is higher than 2V, the part goes into either Hiccup or Latch-off fault protection depending on the HIC/LATCH pin configuration. Refer to "Average Current Sense for Two Phases - IMON" on page 31 for more details.
TRACK	7	External reference input pin for the IC output voltage regulation loop to follow. The input reference signal can be either a digital or analog signal selected by the ATRK/DTRK pin configuration. If the TRACK function is not used, connect the TRACK pin to VCC and the internal VREF_1.6V works as the reference. Refer to "Digital/Analog Track Function" on page 25 for more details.
PGOOD	8	Provides an open-drain, power-good signal. Pull up this pin with a resistor to this IC's VCC for proper function. When the output voltage is within OV/UV thresholds and soft-start is completed, the internal PGOOD open-drain transistor is open and PGOOD is pulled HIGH. It is pulled low when output UV/OV or input OV conditions are detected. Refer to "PGOOD Signal" on page 30 for more details.
FSYNC	9	Dual-function pin for switching frequency setting and synchronization is defined as follows:. • The PWM switching frequency can be programmed by a resistor R_{FSYNC} from this pin to ground. PWM frequency refers to a single-phase switching frequency in this datasheet. The typical programmable frequency range is 50kHz to 1.1MHz. • The PWM switching frequency can also be synchronized to an external clock applied on the FSYNC pin. The FSYNC pin detects the input clock signal's rising edge that it is to be synchronized with. The typical detectable minimum pulse width of the input clock is 20ns. The rising edge of LG1 is delayed by 35ns from the rising edge of the input clock signal at the FSYNC pin. When the internal clock is locked to the external clock, it latches to the external clock. If the external clock on the FSYNC pin is removed, the switching frequency oscillator shuts down. The part then detects PLL_LOCK fault and goes to either Hiccup mode or Latch-off mode, depending on the HIC/LATCHOFF pin configuration. If the part is set in Hiccup mode, it restarts with frequency set by R_{FSYNC}. The typical synchronization frequency range is 50kHz to 1.1MHz. The phase dropping mode is **not allowed** with external synchronization. Refer to "Oscillator and Synchronization" on page 27 for more details.
HIC/LATCH	10	Select either Hiccup or Latch-off response to faults including output overvoltage (monitoring the FB pin), output undervoltage (monitoring the FB pin, default inactive), V_{IN} overvoltage (monitoring the FB pin), peak overcurrent protection (OC2_PEAK), and average current protection (monitoring the IMON pin), etc. Set HIC/LATCH = HIGH to activate the Hiccup fault response. Set HIC/LATCH = LOW to activate the Latch-off fault response. Either toggling the EN pin or recycling VCC POR resets the IC from Latch-off status. Refer to "Selectable Hiccup or Latch-Off Fault Response" on page 33 for more details.
DE/PHDRP	11	Selects Diode Emulation mode (DE), Phase Dropping (PH_DROP) mode, or Continuous Conduction Mode (CCM). The three configurable modes are: DE mode, DE plus PH_DROP mode, and CCM mode. Refer to Table 2 on page 33 for the three configurable options. PD_DROP mode is **not allowed** with external synchronization.
RBLANK	12	A resistor from this pin to ground programs the blanking time for current sensing after the PWM is ON (LG is ON). This blanking time is also called t_{MINON} time, meaning the minimum ON-time when a PWM pulse is ON. Refer to "Minimum On-Time (Blank Time) Consideration" on page 28 for the selection of R_{BLANK}.
PLLCOMP	13	Compensation node for the switching frequency clock's PLL (Phase Lock Loop). A second order passive loop filter connected between this pin and ground compensates the PLL. Refer to "Oscillator and Synchronization" on page 27 for more details.
EN	14	Threshold-sensitive enable input for the controller. When the EN pin is driven above 1.21V (typical), the ISL78227 is enabled and the internal LDO is activated to power up PVCC followed by a start-up procedure. Driving the EN pin below 0.95V disables the IC and clears all fault states. Refer to "Enable" on page 30 for more details.
CLKOUT	15	Outputs a clock signal with same frequency to one phase's switching frequency. The rising edge signal on the CLKOUT pin is delayed by 90° from the rising edge of LG1 of the same IC. With CLKOUT connected to the FSYNC pin of the second ISL78227, a 4-phase interleaving operation can be achieved. Refer to "Oscillator and Synchronization" on page 27 for more details.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
BOOT2	16	Provides bias voltage to the Phase 2 high-side MOSFET driver. A bootstrap circuit creates a voltage suitable to drive the external N-channel MOSFET. A 0.47µF ceramic capacitor in series with a 1.5Ω resistor is recommended between the BOOT2 and PH2 pins. In the typical configuration, PVCC provides the bias to BOOT2 through a fast switching diode. In applications in which a high-side driver is not needed (for example, standard boost applications), BOOT2 is recommended to be connected to ground. The ISL78227 IC can detect BOOT2 being grounded during start-up and both the Phase 1 and Phase 2 high-side drivers are disabled. In addition, PH1 and PH2 should also be tied to ground.
UG2	17	Phase 2 high-side gate driver output. Disable this output by tying either BOOT1 and PH1 to ground or BOOT2 and PH2 to ground.
PH2	18	Represents the return path for the Phase 2 high-side gate drive. Connect this pin to the source of the Phase 2 high-side MOSFETs and the drain of the low-side MOSFETs.
LG2	19	Phase 2 low-side gate driver output. It should be connected to the Phase 2 low-side MOSFETs' gates.
PGND	20	Provides the return path for the low-side MOSFET drivers. This pin carries a noisy driving current, so traces connecting from this pin to the low-side MOSFET source and PVCC decoupling capacitor ground pad should be as short as possible. All sensitive analog signal traces should not share common traces with this driver return path. Connect this pin to the ground copper plane (wiring away from the IC instead of connecting through the IC bottom PAD) through several vias as close as possible to the IC.
PVCC	21	Output of the internal linear regulator that provides bias for the low-side driver, high-side driver (PVCC connected to BOOTx through diodes), and VCC bias (PVCC and VCC are typically connected through a small resistor like 10Ω or smaller, which helps to filter out the noises from PVCC to VCC). The PVCC operating range is 4.75V to 5.5V. A minimum 10µF decoupling ceramic capacitor should be used between PVCC and PGND. Refer to "Internal 5.2V LDO" on page 36 for more details.
LG1	22	Phase 1 low-side gate driver output. It should be connected to the Phase 1 low-side MOSFETs' gates.
PH1	23	Represents the return path for the Phase 1 high-side gate drive. Connect this pin to the source of the Phase 1 high-side MOSFETs and the drain of the low-side MOSFETs.
UG1	24	Phase 1 high-side MOSFET gate drive output. Disable this output by tying either BOOT1 and PH1 to ground or BOOT2 and PH2 to ground.
BOOT1	25	Provides bias voltage to the Phase 1 high-side MOSFET driver. A bootstrap circuit creates a voltage suitable to drive the external N-channel MOSFET. A 0.47µF ceramic capacitor in series with a 1.5Ω resistor are recommended between BOOT1 and PH1 pins. In a typical configuration, PVCC provides the bias to BOOT1 through a fast switching diode. In applications in which a high-side driver is not needed (for example, standard boost applications), BOOT1 is recommended to be connected to ground. The ISL78227 IC can detect BOOT1 being grounded during start-up and both the Phase 1 and Phase 2 high-side drivers are disabled. In addition, PH1 and PH2 should also be tied to ground.
VIN	26	Connect the supply rail to this pin. Typically, connect the boost input voltage to this pin. The VIN pin can also be supplied by a separate input source independent from the boost power stage input source. This pin is connected to the input of the internal linear regulator, generating the power necessary to operate the chip. The DC voltage applied to VIN should not exceed 55V during normal operation. VIN can withstand transients up to 60V, but in this case, the device's overvoltage protection stops it from switching to protect itself. Refer to "Input Overvoltage Fault Protection" on page 34 for more details.
ISEN1N	27	The ISEN1N pin is the negative potential input to the Phase 1 current sense amplifier. This amplifier continuously senses the Phase 1 inductor current through a power current sense resistor in series with the inductor. The sensed current signal is used for current mode control, peak current limiting, average current limiting, and diode emulation.
ISEN1P	28	Positive potential input to the Phase 1 current sense amplifier.
ISEN2N	29	Negative potential input to the Phase 2 current sense amplifier. This amplifier continuously senses the Phase 2 inductor current through a power current sense resistor in series with the inductor. The sensed current signal is used for current mode control, peak current limiting, average current limiting, and diode emulation.
ISEN2P	30	Positive phase input to the Phase 2 current sense amplifier.
ATRK/DTRK	31	Logic input pin to select the input signal format options for the TRACK pin. Pull this pin HIGH for the TRACK pin to accept analog input signals. Pull this pin LOW for the TRACK pin to accept digital input signals. Refer to "Digital/Analog Track Function" on page 25 for more details.
RDT	32	A resistor connected from this pin to ground programs the dead times between UGx OFF to LGx ON and LGx OFF to UGx ON to prevent shoot-through. Refer to "Driver Configuration" on page 24 for the selection of RDT.
SGND	-	Signal ground bottom pad to which to refer the internal sensitive analog circuits. Also serves as thermal pad. Connect this pad to a large ground plane. Put as many vias as possible in this pad connecting to the ground copper plane to help reduce the IC's θ_{JA}. In layout power flow planning, avoid noisy, high frequency pulse current flow through the SGND area.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (Units) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL78227ARZ	ISL78227ARZ	-40 to +125	-	32 Ld 5x5 WFQFN	L32.5x5H
ISL78227ARZ-T	ISL78227ARZ	-40 to +125	6k	32 Ld 5x5 WFQFN	L32.5x5H
ISL78227ARZ-T7A	ISL78227ARZ	-40 to +125	250	32 Ld 5x5 WFQFN	L32.5x5H
ISL78227EV1Z	Evaluation Board				

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL78227 product information page. For more information about MSL, refer to TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	TOPOLOGY	PMBus™	NTC	TRACK FUNCTION	PACKAGE
ISL78229	2-Phase Boost Controller	Yes	Yes	Yes	40 Ld 6x6 WFQFN
ISL78227	2-Phase Boost Controller	No	No	Yes	32 Ld 5x5 WFQFN

Block Diagram

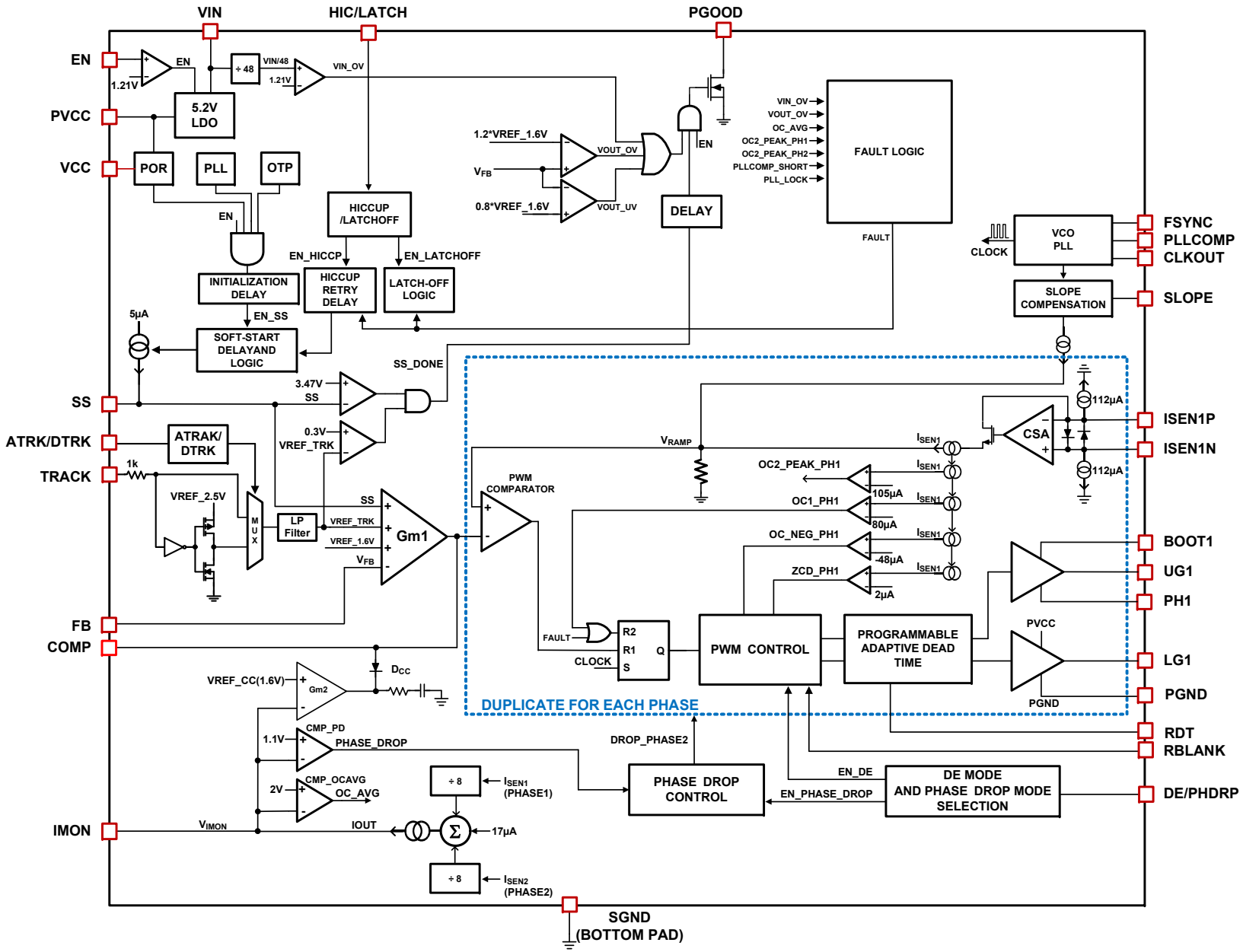
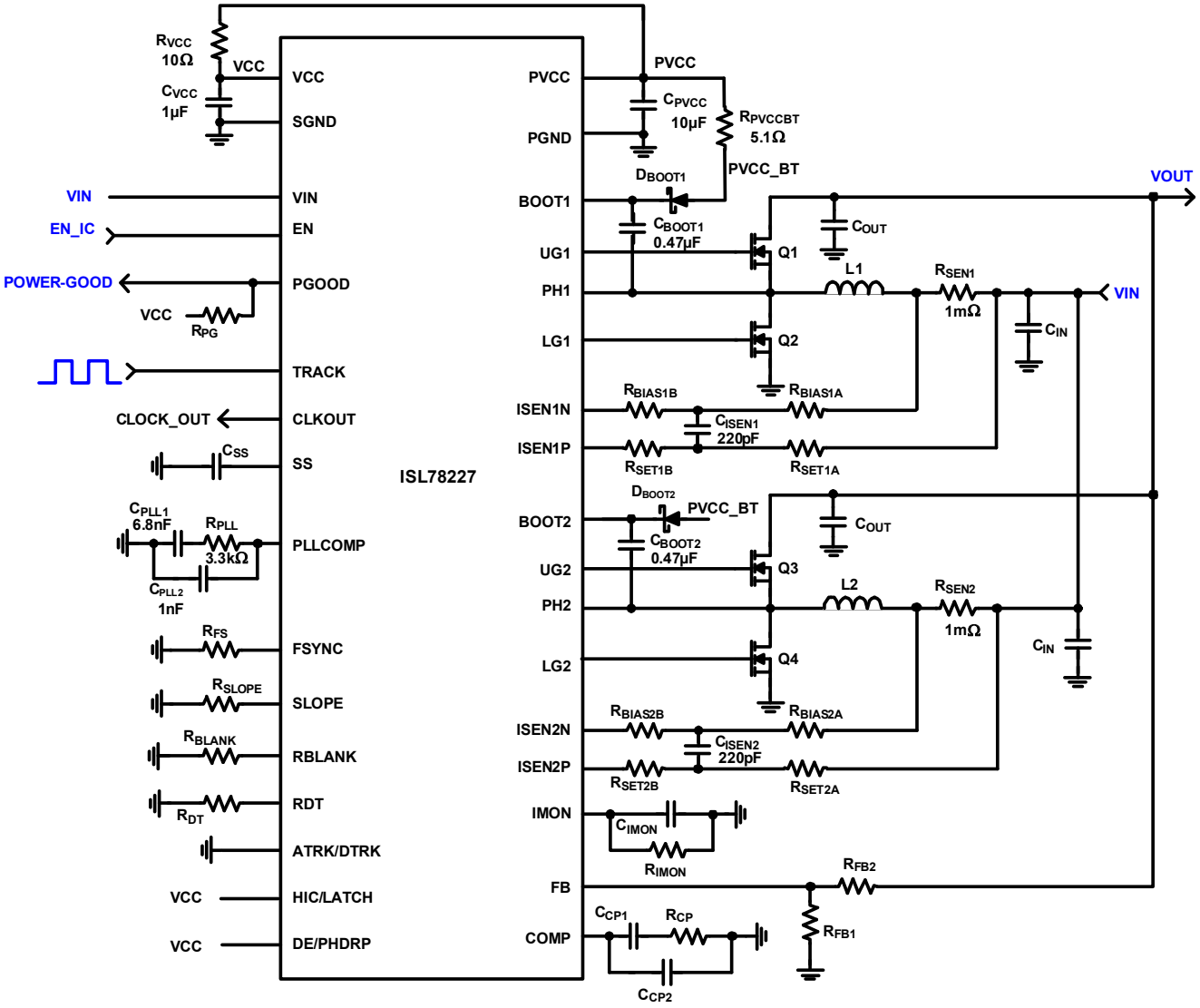


FIGURE 3. BLOCK DIAGRAM

Typical Application - 2-Phase Synchronous Boost



ATRK/DTRK:
= VCC to track analog signal
= GND to track digital signal

HIC/LATCH:
= VCC for HICCUP mode
= GND for LATCHOFF mode

DE/PHDRP:
= VCC for DE mode
= FLOAT for DE and Phase-Drop mode
= GND for CCM mode

Q1, Q2, Q3, Q4: 2 BUK9Y6R0-60E in parallel

FIGURE 4. TYPICAL APPLICATION 2-PHASE SYNCHRONOUS BOOST

Absolute Maximum Ratings

VIN . . . . . - 0.3V to +60V
PH1, PH2 . . . . . - 0.3V to +60V
. . . . . -10V(<20ns Pulse Width, 25µJ)
BOOT1, BOOT2, UG1, UG2 . . . . . - 0.3V to +65V
Upper Driver Supply Voltage, V_{BOOTx} - V_{PHx} . . . . . - 0.3V to +6.5V
. . . . . -0.3V to +0.9V (<10ns)
PVCC, VCC . . . . . - 0.3V to +6.5V
ISEN1P, ISEN1N, ISEN2P, ISEN2N . . . . . - 0.3V to +60V
V_{ISENxP} - V_{ISENxN} . . . . . ±0.6V
All Other Pins . . . . . - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model (Tested per AEC-Q100-002) 2kV
Charged Device Model (Tested per AEC-Q100-011) 750V
Latch-Up Rating (Tested per AEC-Q100-004) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld 5x5 WFQFN Package (Notes 4, 5)	30	1.2

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . refer to TB493

Recommended Operating Conditions

VIN . . . . . 5V to +55V
PVCC, VCC . . . . . 4.75V to 5.5V
PH1, PH2 . . . . . - 0.3V to +55V
Upper Driver Supply Voltage, V_{BOOTx} - V_{PHx} . . . . . 3.5V to 6V
ISEN1P to ISEN1N and ISEN2P to ISEN2N Differential Voltage . . . . ±0.3V
ISEN1P, ISEN1N, ISEN2P, ISEN2N Common-Mode Voltage . . . . 4V to 55V
Operational Junction Temperature Range (Automotive) . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 7). Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SUPPLY INPUT						
Input Voltage Range	V_{IN}	Switching, under the condition of internal LDO having dropout (V_{IN} - PVCC) less than 0.25V	**5**		**55**	V
Input Supply Current to the VIN Pin (IC Enabled)	I_{Q_SW}	EN = 5V, V_{IN} = 12V, PVCC = VCC, BOOT1 and BOOT2 supplied by PVCC, R_{FSYNC} = 40.2k (f_{SW} = 300kHz), LGx = OPEN, UGx = OPEN		8.0	**10.0**	mA
	I_{Q_NON-SW}	EN = 5V, V_{IN} = 12V, PVCC = VCC, BOOT1 and BOOT2 supplied by PVCC, non-switching, LGx = OPEN, UGx = OPEN		6.0	**8.5**	mA
Input Supply Current to the VIN Pin (IC Shutdown)	$I\_SD\_VIN\_55V$	EN = GND, V_{IN} = 55V		0.2	**1.0**	µA
Input Bias Current (IC Shutdown) to Each of ISEN1P/ISEN1N/ISEN2P/ISEN2N Pins	I_SD_ISENxP/N	EN = GND, V_{IN} = 55V ISEN1P (or ISEN1N/ISEN2P/ISEN2N) = 55V	**-1**	0	**1**	µA
INPUT OVERVOLTAGE PROTECTION						
V_{IN} OVP Rising Threshold (Switching Disable)		EN = 5V, V_{IN} rising	**56.5**	58.0	**59.5**	V
V_{IN} OVP Trip Delay		EN = 5V, V_{IN} rising		5		µs
INTERNAL LINEAR REGULATOR						
LDO Voltage (PVCC Pin)	V_{PVCC}	V_{IN} = 6V to 55V, C_{PVCC} = 4.7µF, I_{PVCC} = 10mA	**5.0**	5.2	**5.4**	V
LDO Saturation Dropout Voltage (PVCC Pin)	$V_{DROPOUT}$	V_{IN} = 4.9V, C_{PVCC} = 4.7µF, I_PVCC = 80mA		0.3		V
LDO Current Limit (PVCC Pin)	I_{OC_LDO}	V_{IN} = 6V, V_{PVCC} = 4.5V	**130**	195	**250**	mA
LDO Output Short Current Limit (PVCC Pin)	I_{OCFB_LDO}	V_{IN} = 6V, V_{PVCC} = 0V	**50**	100	**160**	mA

Electrical Specifications Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 7). Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER-ON RESET (For both PVCC and VCC)						
Rising V_{VCC} POR Threshold	V_{PORH_VCC}		**4.35**	4.50	**4.75**	V
Falling V_{VCC} POR Threshold	V_{PORL_VCC}		**4.05**	4.15	**4.25**	V
V_{VCC} POR Hysteresis	V_{PORHYS_VCC}			0.4		V
Rising V_{PVCC} POR Threshold	V_{PORH_PVCC}		**4.35**	4.50	**4.75**	V
Falling V_{PVCC} POR Threshold	V_{PORL_PVCC}		**3.0**	3.2	**3.4**	V
V_{PVCC} POR Hysteresis	V_{PORHYS_PVCC}			1.3		V
Soft-Start Delay	t_{SS_DLY}	From POR rising to initiation of soft-start. R_{FSYNC} = 61.9k, f_{SW} = 200kHz, PLLCOMP pin network of R_{PLL} = 3.24k, C_{PLL1} = 6.8nF, and C_{PLL2} = 1nF		0.85		ms
EN						
Enable Threshold	V_{ENH}	EN Rising	**1.13**	1.21	**1.33**	V
	V_{ENL}	EN Falling	**0.85**	0.95	**1.10**	V
	V_{EN_HYS}	Hysteresis		250		mV
Input Impedance		EN = 4V	**2**	6		MΩ
PWM SWITCHING FREQUENCY						
PWM Switching Frequency (Per Phase)	F_{OSC}	R_{FSYNC} = 249kΩ (0.1%)	**46.0**	50.2	**54.5**	kHz
		R_{FSYNC} = 82.5kΩ (0.1%)	**142**	150	**156**	kHz
		R_{FSYNC} = 40.2kΩ (0.1%)	**290**	300	**310**	kHz
		R_{FSYNC} = 10kΩ (0.1%)	**990**	1100	**1170**	kHz
Minimum Adjustable Switching Frequency				50		kHz
Maximum Adjustable Switching Frequency				1100		kHz
FSYNC Pin Voltage				0.5		V
Minimum ON-Time (Blanking Time) on LGx	t_{MINON_1}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 80kΩ (0.1%)	**315**	410	**525**	ns
	t_{MINON_2}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 50kΩ (0.1%)	**175**	260	**325**	ns
	t_{MINON_3}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 25kΩ (0.1%)	**100**	140	**180**	ns
	t_{MINON_4}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 10k	**75**	90	**105**	ns
Maximum Duty Cycle	D_{MAX}	D_{MAX} = T_LG_ ON/t_{SW}, V_{COMP} = 3.5V, f_{SW} = 300kHz, RDT = 18.2kΩ, C_{UG} = OPEN, C_{LG} = OPEN	**88.5**	89.0	**90.5**	%
SYNCHRONIZATION (FSYNC PIN)						
Minimum Synchronization Frequency at FSYNC Input				50		kHz
Maximum Synchronization Frequency at FSYNC Input				1100		kHz
Input High Threshold	V_{IH}		**3.5**			V
Input Low Threshold	V_{IL}				**1.5**	V

Electrical Specifications Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 7). Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Input Minimum Pulse Width - Rise-to-Fall			**20**			ns
Input Minimum Pulse Width - Fall-to-Rise			**20**			ns
Delay Time from Input Pulse Rising to LG1 Rising Edge Minus Dead Time t_{DT1}		C_{LG} = OPEN, RDT = 50kΩ		35		ns
Input Impedance		Input impedance before synchronization mode		1		kΩ
		Input impedance after synchronization mode		200		MΩ
CLKOUT						
$CLKOUT_H$		I_{CLKOUT} = 500µA	**V_{CC} - 0.5**	V_{CC} - 0.1		V
$CLKOUT_L$		I_{CLKOUT} = -500µA		0.1	**0.4**	V
Output Pulse Width		C_{CLKOUT} = 100pF, t_{SW} is each phase's switching period		1/12 * t_{SW}		
Phase Shift from LG1 Rising Edge to CLKOUT Pulse Rising Edge		C_{LG1} = OPEN, C_{CLKOUT} = OPEN, f_{SW} = 300kHz, t_{DT1} = 60ns (refer to Figure 56 on page 28 for the timing diagram)		87		°
SOFT-START						
Soft-Start Current	I_{SS}		**4.5**	5.0	**5.5**	µA
Minimum Soft-Start Pre-Bias Voltage				0		V
Maximum Soft-Start Pre-Bias Voltage				1.6		V
Soft-Start Pre-bias Voltage Accuracy		V_{FB} = 500mV	**-25**	0	**25**	mV
Soft-Start Clamp Voltage	$V_{SSCLAMP}$		**3.25**	3.47	**3.70**	V
HICCUP RETRY DELAY (Refer to "Selectable Hiccup or Latch-Off Fault Response" on page 33 for details)						
Hiccup Retry Delay		If Hiccup fault response selected		500		ms
REFERENCE VOLTAGE FOR OUTPUT VOLTAGE REGULATION						
System Reference Accuracy		Measured at the FB pin	**1.576**	1.600	**1.620**	V
FB Pin Input Bias Current		V_{FB} = 1.6V, TRACK = Open	**-0.05**	0.01	**0.05**	µA
ERROR AMPLIFIER FOR OUTPUT VOLTAGE REGULATION (Gm1)						
Transconductance Gain				2		mA/V
Output Impedance				7.5		MΩ
Unity Gain Bandwidth		C_{COMP} = 100pF from COMP pin to GND		3.3		MHz
Slew Rate		C_{COMP} = 100pF from COMP pin to GND		±3		V/µs
Output Current Capability				±300		µA
Maximum Output Voltage			**3.5**	3.7		V
Minimum Output Voltage				0.1	**0.3**	V
PWM CORE						
SLOPE Pin Voltage			**480**	500	**520**	mV
SLOPE Accuracy		R_{SLOPE} = 20k (0.1%)	**-20**	0	**20**	%
		R_{SLOPE} = 40.2k (0.1%)	**-20**	3	**20**	%

Electrical Specifications Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 7). Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Duty Cycle Matching		V_{RSENx} = 30mV, R_{SETx} = 665Ω (0.1%), R_{SLOPE} = 27k, f_{SW} = 150kHz, V_{COMP} = 2.52V, Measure $(T_{on\_lg2} - T_{on\_lg1})/(T_{on\_lg2} + T_{on\_lg1})$ *2		3		%
CURRENT SENSE AMPLIFIER						
Minimum ISENxN and ISENxP Common-Mode Voltage Range		Accuracy becomes worse when lower than 4V		4		V
Maximum ISENxN and ISENxP Common-Mode Voltage Range				55		V
Maximum Input Differential Voltage Range	V_{ISENxP} - V_{ISENxN}			±0.3		V
ISENxP/ISENxN Bias Current	I_{SENxP/N_BIAS}	Sourcing out of pin, EN = 5V, V_{ISENxN} = V_{ISENxP}, V_{CM} = 4V to 55V	**100**	123	**150**	µA
ZCD DETECTION - CSA						
Zero Crossing Detection (ZCD) Threshold	V_{ZCD_CSA}	Measures voltage threshold before R_{SEN} at CSA inputs (equivalent to the voltage across the current sense shunt resistor), R_{SET} = 665Ω (0.1%)	**-4.0**	1.3	**6.0**	mV
PHASE DROPPING						
V_{IMON} Phase-Drop Falling Threshold, to Drop Phase 2	$V_{PHDRP\_TH\_F}$	When V_{IMON} falls below $V_{PHDRP\_TH\_F}$, drop off Phase 2	**1.0**	1.1	**1.2**	V
V_{IMON} Phase-Add Rising Threshold, to Add Phase 2	$V_{PHADD\_TH\_R}$	When V_{IMON} rise above $V_{PHADD\_TH\_R}$, add back Phase 2	**1.05**	1.15	**1.25**	V
V_{IMON} Phase-Drop Threshold Hysteresis	V_{PHDRP_HYS}	When V_{IMON}<$V_{PHDRP\_TH\_F}$ - V_{PHDrop_HYS}, add back Phase 2	**45**	50	**55**	mV
PEAK OVERCURRENT CYCLE-BY-CYCLE LIMITNG (OC1)						
Peak Current Cycle-by-Cycle Limit Threshold for Individual Phase	V_{OC1}	Cycle-by-cycle current limit threshold (I_{OC1_TH} = 80µA, compared with I_{SENx}). Measures the voltage threshold before R_{SETx} at CSA Inputs (equivalent to the voltage across the current sense shunt resistor), R_{SETx} = 665Ω (0.1%)	**40**	53	**65**	mV
Peak Current Cycle-by-Cycle Limit Trip Delay		C_{LG} = OPEN, from the time V_{OC1} tripped to LG falling		50		ns
PEAK OVERCURRENT FAULT PROTECTION OC2_PEAK, (Refer to "Peak Overcurrent Fault (OC2_PEAK) Protection" on page 35 for details)						
Peak Current Fault Protection Threshold for Individual Phase	V_{OC2}	Peak current hiccup protection threshold (I_{OC2_TH} = 105µA, compared with I_{SENx}). Measures the voltage threshold before R_{SETx} at CSA Inputs (equivalent to the voltage across the current sense shunt resistor), R_{SETx} = 665Ω (0.1%)	**55**	70	**85**	mV
OC2_PEAK Trip Blanking Time				3		cycles

Electrical Specifications Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 7). Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
NEGATIVE CURRENT CYCLE-BY-CYCLE LIMITNG (OC_NEG)						
Negative Current Cycle-by-Cycle Limit Threshold for Individual Phase	V_{OC_NEG}	Negative Current Cycle-by-Cycle Limit ($I_{OC\_NEG\_TH}$ = -48µA, compared with I_{SENx}). Measures the voltage threshold before R_{SETx} at CSA Inputs (equivalent to the voltage across the current sense shunt resistor), R_{SET} = 665Ω (0.1%)		-32		mV
AVERAGE CONSTANT CURRENT CONTROL LOOP						
IMON Current Accuracy		V_{RSENx} = 30mV, R_{SETx} = 665Ω (0.1%), with ISENxP/N pins biased at 4V or 55V common-mode voltage	**27.0**	28.3	**29.5**	µA
IMON Offset Current		V_{RSENx} = 0V, R_{SET} = 665Ω (0.1%), with ISENxP/N pins biased at 4V or 55V common-mode voltage	**16**	17	**18**	µA
Constant Current Control Reference Accuracy	$VREF_{CC}$	Measure the IMON pin	**1.575**	1.600	**1.625**	V
AVERAGE OVERCURRENT FAULT PROTECTION OC_AVG, (Refer to "Average Overcurrent Fault (OC_AVG) Protection" on page 36 for details)						
OC_AVG Fault Threshold at the IMON Pin			**1.9**	2.0	**2.1**	V
OC_AVG Fault Trip Delay				1		µs
GATE DRIVERS						
UG Source Resistance	R_{UG_SOURCE}	100mA source current, V_{BOOT} - V_{PH} = 4.4V		1.2		Ω
UG Source Current	I_{UG_SOURCE}	V_{UG} - V_{PH} = 2.5V, V_{BOOT} - V_{PH} = 4.4V		2		A
UG Sink Resistance	R_{UG_SINK}	100mA sink current, V_{BOOT} - V_{PH} = 4.4V		0.6		Ω
UG Sink Current	I_{UG_SINK}	V_{UG} - V_{PH} = 2.5V, V_{BOOT} - V_{PH} = 4.4V		2.0		A
LG Source Resistance	R_{LG_SOURCE}	100mA source current, PVCC = 5.2V		1.2		Ω
LG Source Current	I_{LG_SOURCE}	V_{LG} - PGND = 2.5V, PVCC = 5.2V		2.0		A
LG Sink Resistance	R_{LG_SINK}	100mA sink current, PVCC = 5.2V		0.55		Ω
LG Sink Current	I_{LG_SINK}	V_{LG} - PGND = 2.5V, PVCC = 5.2V		3		A
UG to PH Internal Resistor				50		kΩ
LG to PGND Internal Resistor				50		kΩ
BOOT-PH UVLO Detection Threshold			**2.8**	3.0	**3.2**	V
BOOT-PH UVLO Detection Threshold Hysteresis			**0.09**	0.15	**0.22**	V
Dead Time Delay - UG Falling to LG Rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 10k (0.1%)	**55**	70	**85**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 10k (0.1%)	**65**	80	**95**	ns
Dead Time Delay - UG Falling to LG rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 18.2kΩ (0.1%)	**85**	100	**115**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 18.2kΩ (0.1%)	**95**	110	**125**	ns
Dead Time Delay - UG Falling to LG Rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 50kΩ (0.1%)	**185**	210	**240**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 50kΩ (0.1%)	**205**	230	**260**	ns
Dead Time Delay - UG Falling to LG Rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 64.9kΩ (0.1%)	**235**	265	**295**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 64.9kΩ (0.1%)	**260**	290	**320**	ns

Electrical Specifications Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 7). Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
OUTPUT OVERVOLTAGE DETECTION/PROTECTION MONITOR THE FB PIN, (Refer to "Output Overvoltage Fault Protection" on page 34 for details)						
FB Overvoltage Rising Trip Threshold	V_{FBOV_RISE}	Percentage of VREF_1.6V (Selectable Hiccup/Latch-off response)	**118**	120	**122**	%
FB Overvoltage Falling Recovery Threshold	V_{FBOV_FALL}	Percentage of VREF_1.6V (Selectable Hiccup/Latch-off response)	**114**	116	**118**	%
Overvoltage Threshold Hysteresis				4		%
FB Overvoltage Trip Delay				1		µs
OUTPUT UNDERVOLTAGE DETECTION (MONITOR THE FB PIN), (Refer to "Output Undervoltage Indication" on page 34 for details)						
Undervoltage Falling Trip Threshold	$V_{FBUVREF\_FALL}$	Percentage of VREF_1.6V	**78**	80	**82**	%
Undervoltage Rising Recovery Threshold	$V_{FBUVREF\_RISE}$	Percentage of VREF_1.6V	**82.5**	84.0	**86.5**	%
Undervoltage Threshold Hysteresis				4		%
POWER-GOOD MONITOR (PGOOD PIN)						
PGOOD Leakage Current		PGOOD HIGH, V_{PGOOD} = 5V			**1**	µA
PGOOD Low Voltage		PGOOD LOW, I_{PGOOD} = 0.5mA		0.06	**0.40**	V
PGOOD Rising Delay (DE Mode)		The PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥ 0.3V to PGOOD HIGH when DE mode is selected (DE/PHDRP = VCC or FLOAT)		0.5		ms
PGOOD Rising Delay (CCM Mode)		The PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥ 0.3V to PGOOD HIGH when CCM mode is selected (DE/PHDRP = GND)		100		ms
PGOOD Falling Blanking Time				10		µs
HIC/LATCH, ATRK/DTRK PIN DIGITAL LOGIC INPUT						
Input Leakage Current		EN <1V	**-1**		**1**	µA
Input Pull Down Current		EN >2V, pin voltage = 2.1V	**0.7**	1.0	**2.0**	µA
Logic Input Low					**0.8**	V
Logic Input High			**2.1**			V
DE/PHDRP PIN DIGITAL LOGIC INPUT (HIGH/LOW/FLOAT)						
Input Leakage Current			-1		1	µA
Float Impedance - Pin to VCC		Pin = GND	**100**	200	**300**	kΩ
Float Impedance - Pin to GND		Pin = VCC	**100**	200	**300**	kΩ
Output Voltage on DE/PHDRP Pin		Pin = Float	**2.1**	2.6	**2.7**	V
Tri-State Input Voltage MAX					3	V
Tri-State Input Voltage MIN			**1.8**			V
Logic Input Low		Pin voltage falling			**0.7**	V
Logic Input High		Pin voltage rising	**V_{CC} - 0.4**			V
TRACK PIN - DIGITAL INPUT LOGIC						
Input Leakage Current		EN <1V, pin voltage = 5V, V_{CC} = 0V	**-1**		**1**	µA
Input Pull-Up Current		EN >2V, pin voltage = 0V, V_{CC} = 5V	**0.8**	1.1	**1.5**	µA

Electrical Specifications Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 7). Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Input Pull-Up Current Compliance Voltage		EN >2V, pin open		2.5		V
Logic Input Low		PIN voltage falling			**0.8**	V
Logic Input High		PIN voltage rising	2			V
Duty Cycle Conversion (FB Accuracy)		0% duty cycle input, measure at the FB pin		0		V
		25% duty cycle input, frequency = 400kHz, measure at the FB pin	**0.600**	0.625	**0.650**	V
		50% duty cycle input, frequency = 400kHz, measure at the FB pin	**1.218**	1.253	**1.288**	V
		60% duty cycle input, measure at the FB pin	**1.45**	1.49	**1.53**	V
TRACK PIN - ANALOG INPUT						
Input Leakage Current		V_{TRACK} = 1.6V, leakage current into this pin to ground	**-1.0**	-0.6	**-0.3**	µA
TRACK Input Reference Voltage Range			0		**1.6**	V
TRACK Input Reference Voltage Accuracy		Measure at the FB pin, V_{TRACK} = 1.5V	**-4.0**	-0.5	**4.0**	%
		Measure at the FB pin, V_{TRACK} = 0.5V	**-6.0**	1.8	**6.0**	%
TRACK SS_DONE Detection Threshold			**0.29**	0.30	**0.31**	V
OVER-TEMPERATURE PROTECTION						
Over-Temperature Trip Point				160		°C
Over-Temperature Recovery Threshold				145		°C

NOTES:

6. Compliance to datasheet limits are assured by one or more methods: production test, characterization, and/or design.
7. The IC is tested in conditions with minimum power dissipations in the IC, meaning $T_A \approx T_J$.

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C.

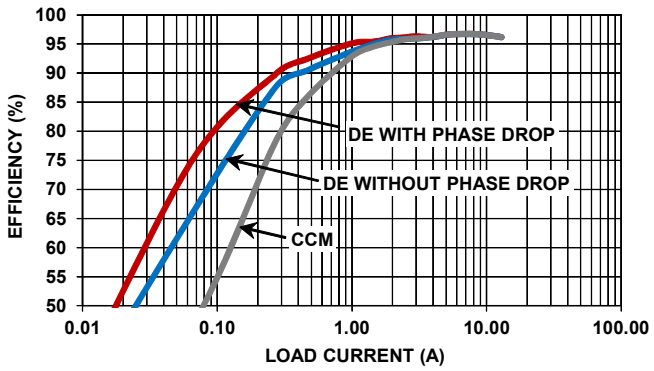


FIGURE 5. EFFICIENCY vs LOAD, 2-PHASE BOOST, 3 MODES OPERATION, f_{SW} = 200kHz, V_{IN} = 12V, V_{OUT} = 36V, T_A = +25°C

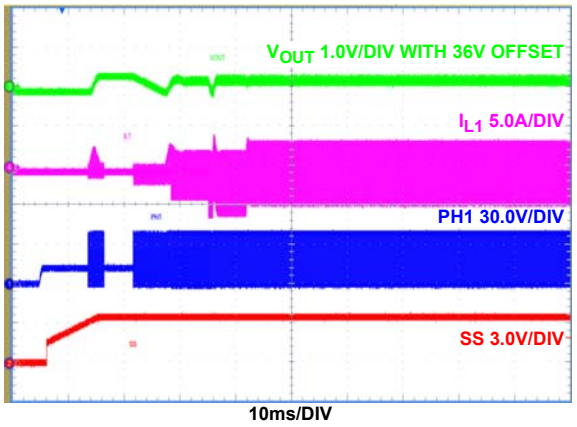


FIGURE 6. EN INTO PRE-BIASED OUTPUT, CCM MODE (DE/PHDRP = GND), I_{OUT} = 0A

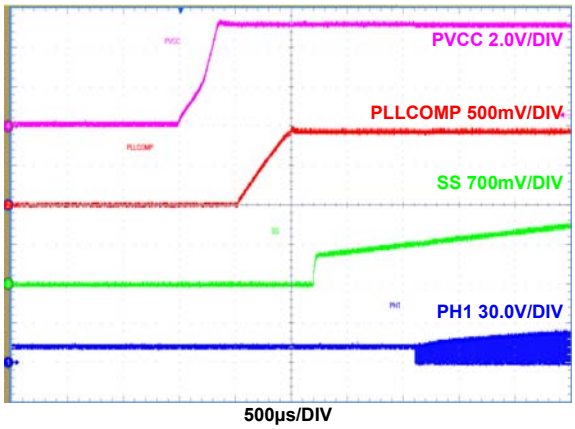


FIGURE 7. EN ON AND INITIALIZATION TO START-UP, I_{OUT} = 0A

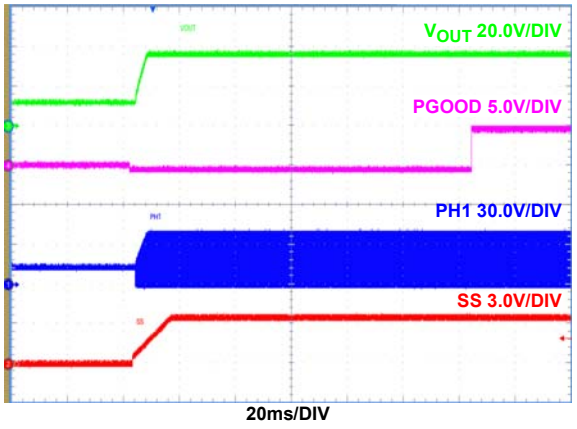


FIGURE 8. SOFT-START, CCM MODE (DE/PHDRP = GND), I_{OUT} = 8A

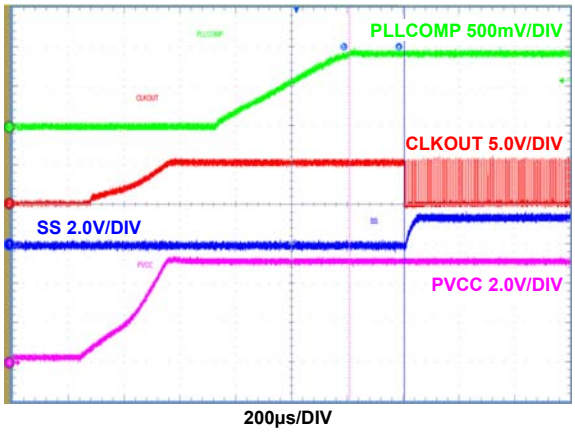


FIGURE 9. EN ON AND INITIALIZATION TO START-UP, I_{OUT} = 0A

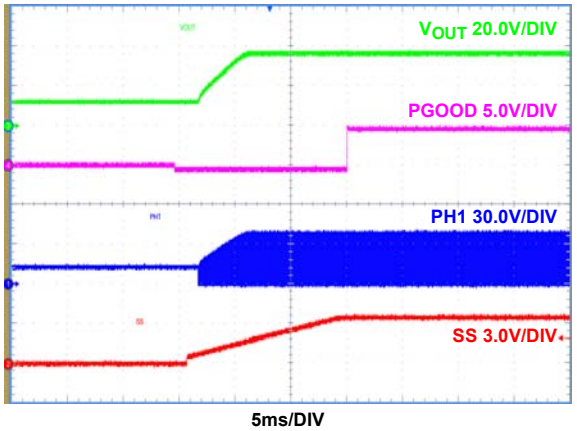


FIGURE 10. SOFT-START, DE+PHDROP MODE (DE/PHDRP = FLOAT), I_{OUT} = 8A

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C. **(Continued)**

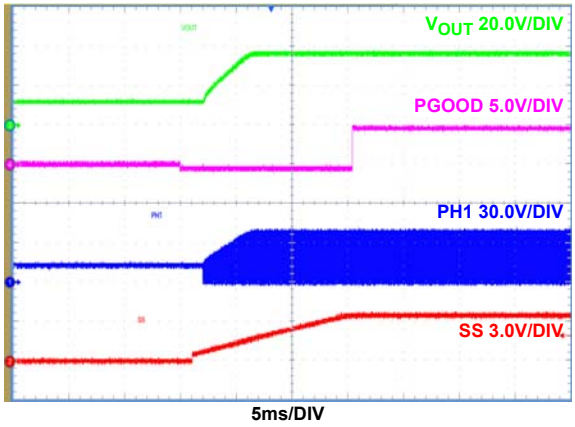


FIGURE 11. SOFT-START, DE MODE (DE/PHDRP = VCC), I_{OUT} = 8A

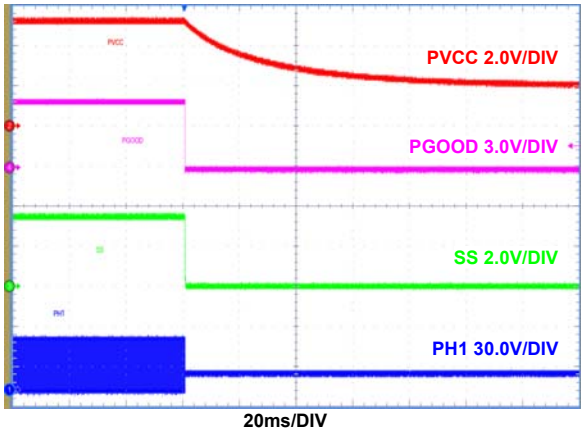


FIGURE 12. EN SHUTDOWN, PVCC/PGOOD/SS FALL, I_{OUT} = 0A

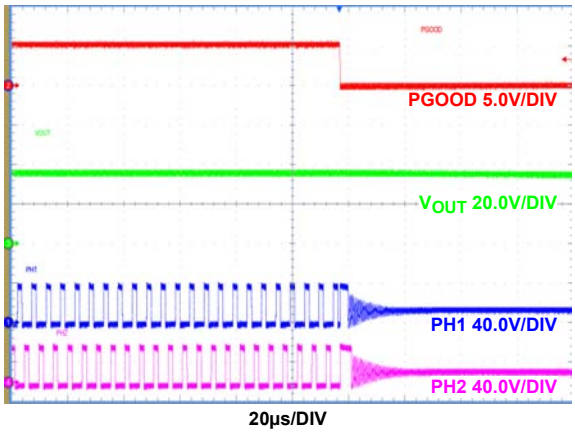


FIGURE 13. EN SHUTDOWN, I_{OUT} = 8A

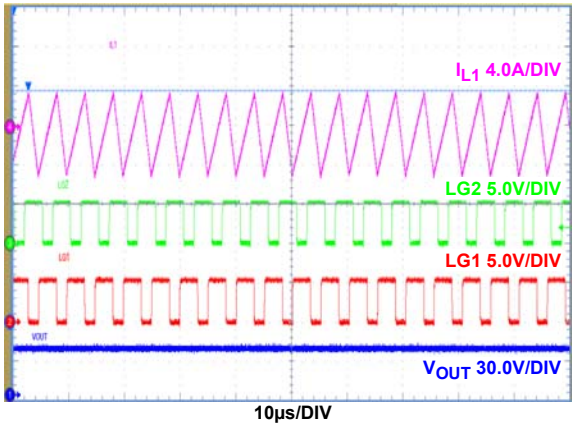


FIGURE 14. CCM MODE (DE/PHDRP = GND), PHASE 1 INDUCTOR RIPPLE CURRENT, I_{OUT} = 0A

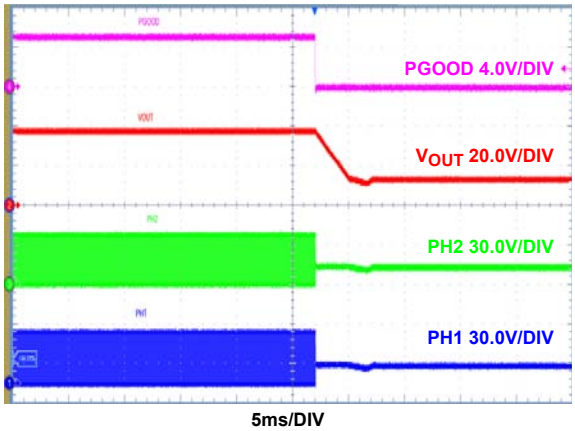


FIGURE 15. EN SHUTDOWN, I_{OUT} = 8A

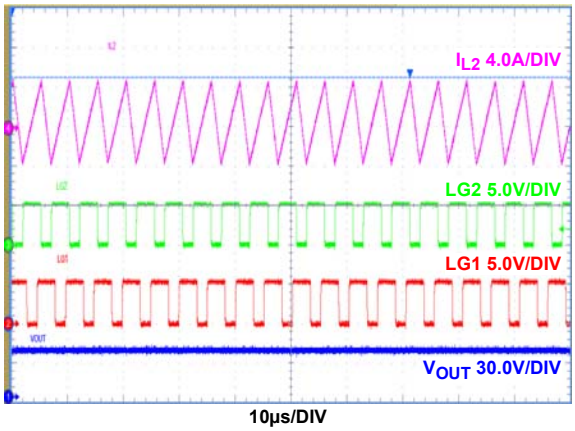


FIGURE 16. CCM MODE (DE/PHDRP = GND), PHASE 2 INDUCTOR RIPPLE CURRENT, I_{OUT} = 0A

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C. **(Continued)**

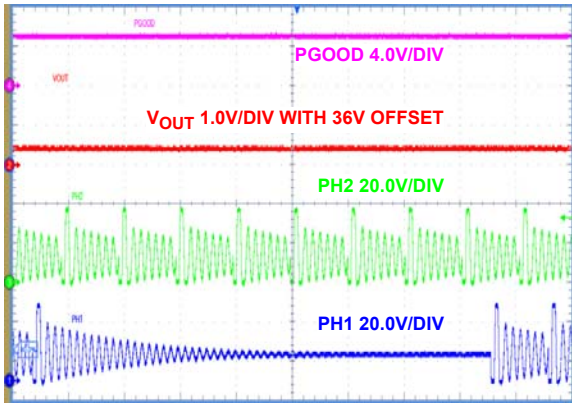


FIGURE 17. DE MODE (DE/PHDRP = V_{CC}), DIODE EMULATION OPERATION, PULSE SKIPPING, I_{OUT} = 0A

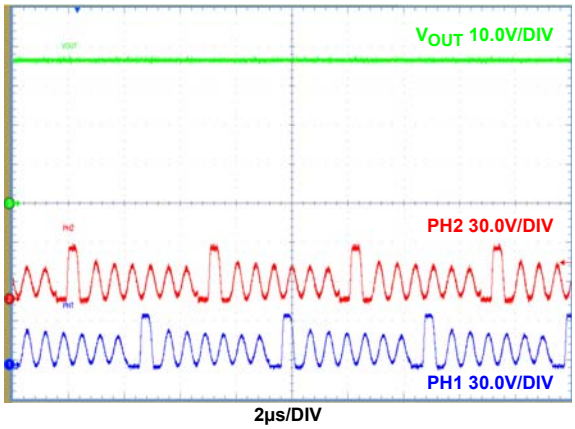


FIGURE 18. DE MODE (DE/PHDRP = V_{CC}), DIODE EMULATION OPERATION, I_{OUT} = 29mA

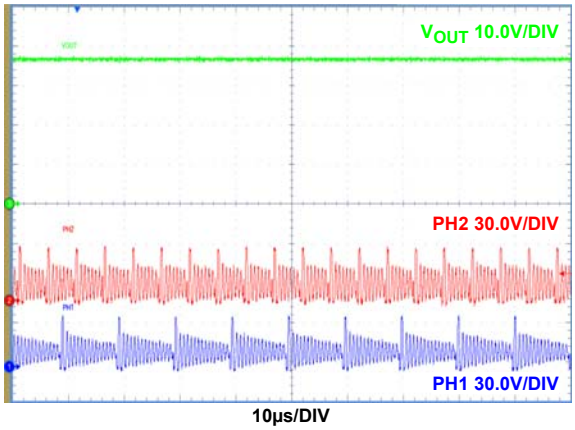


FIGURE 19. DE MODE (DE/PHDRP = V_{CC}), PH1 AND PH2 DIODE EMULATION OPERATION, PULSE SKIPPING, I_{OUT} = 7mA

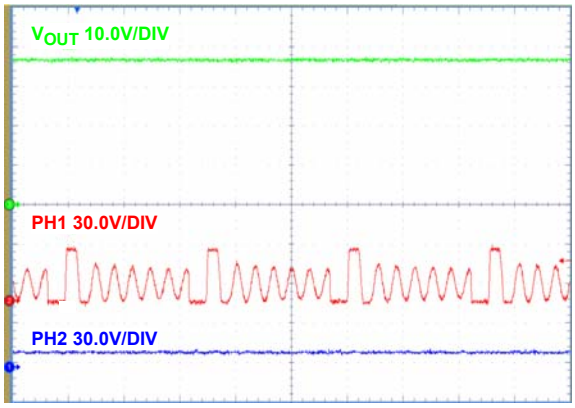


FIGURE 20. DE+PH_DROP MODE (DE/PHDRP = FLOAT), PH1 DIODE EMULATION WITH PH2 DROPPED, I_{OUT} = 29mA

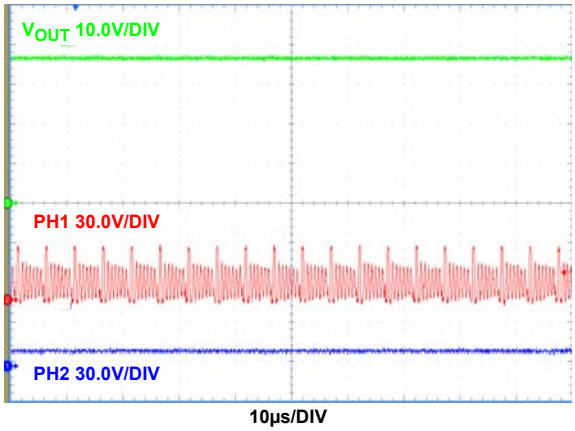


FIGURE 21. DE+PHDRP MODE (DE/PHDRP = FLOAT), PH1 DIODE EMULATION WITH PH2 DROPPED, I_{OUT} = 7mA

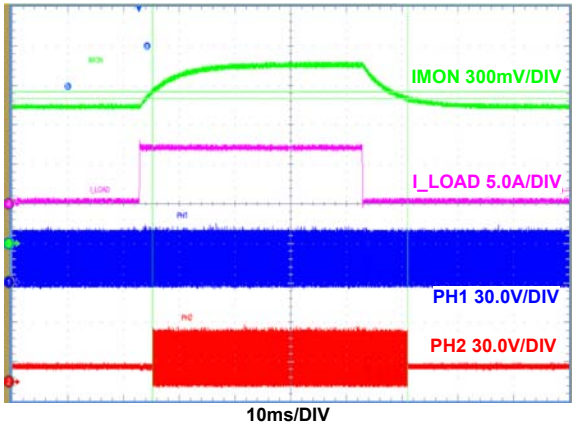


FIGURE 22. DE+PHDRP MODE (DE/PHDRP = FLOAT), PH2 ADDED AND DROPPED, UNDER TRANSIENT STEP LOAD OF 1A TO 8A

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C. **(Continued)**

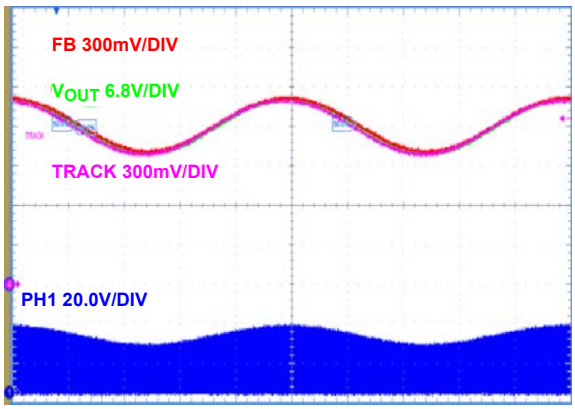


FIGURE 23. ANALOG TRACKING 100Hz SINUSOIDAL SIGNAL, CCM MODE (DE/PHDRP = GND), ATRK/DTRAK = VCC, I_{OUT} = 1A

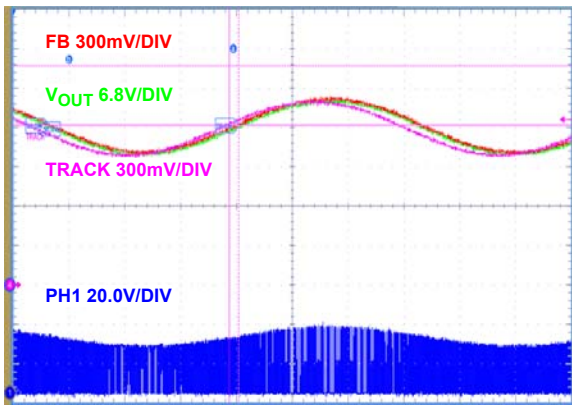


FIGURE 24. ANALOG TRACKING 300Hz SINUSOIDAL SIGNAL AT THE TRACK PIN, CCM MODE (DE/PHDRP = GND), ATRK/DTRAK = VCC, I_{OUT} = 1A

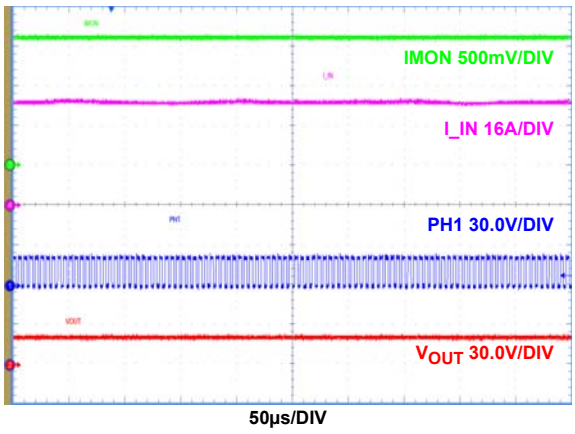


FIGURE 25. STEADY-STATE OPERATION OF INPUT CONSTANT CURRENT MODE, I_{IN} CONTROLLED AT 43A CONSTANT, V_{OUT} = 19.5V

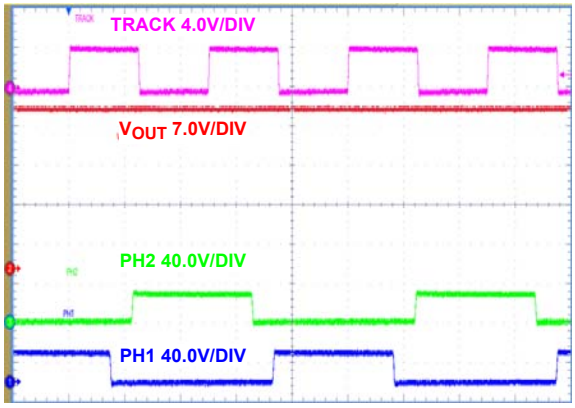


FIGURE 26. DIGITAL TRACKING (TRACKING SIGNAL, FREQUENCY = 400kHz, D_TRACK = 0.5), V_{OUT} = 28.3V

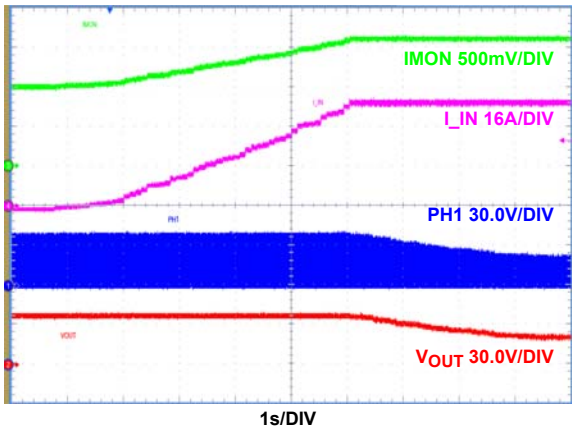


FIGURE 27. LOAD CURRENT KEEP INCREASING FROM NO LOAD TO OVERLOAD (25A), V_{OUT} STARTS TO DROP WHEN INPUT CONSTANT CURRENT MODE STARTS TO WORK, INPUT CURRENT IS FINALLY CONTROLLED TO BE CONSTANT

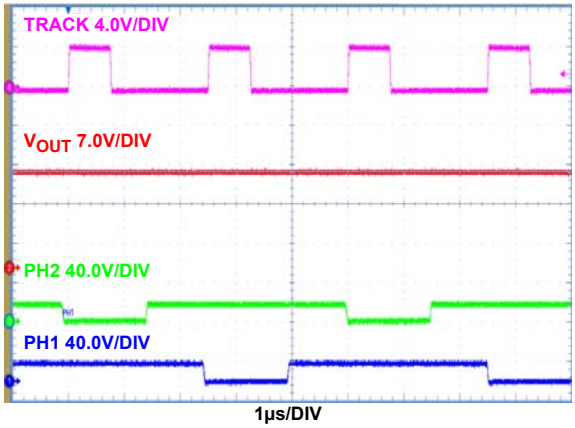


FIGURE 28. DIGITAL TRACKING (TRACKING SIGNAL, FREQUENCY = 400kHz, D_TRACK = 0.3), V_{OUT} = 17V

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C. **(Continued)**

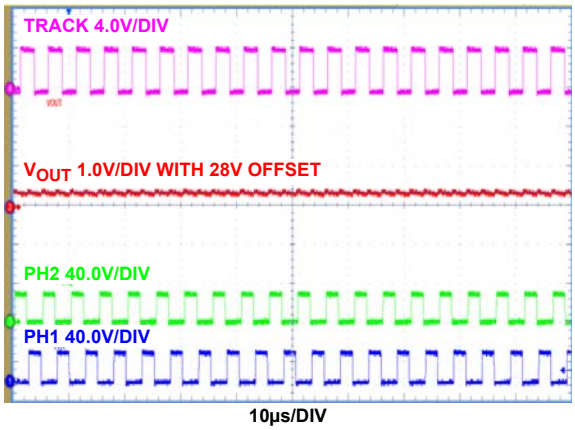


FIGURE 29. DIGITAL TRACKING, (TRACKING SIGNAL, FREQUENCY = 200kHz, D_TRACK = 0.5), V_{OUT} = 28.3V

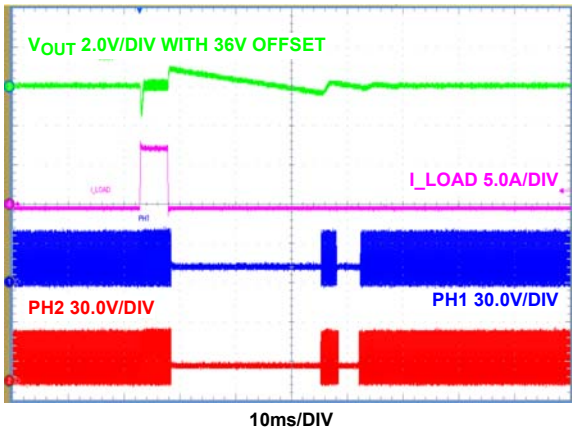


FIGURE 30. DE MODE (DE/PHDRP = VCC), TRANSIENT RESPONSE, I_{OUT} = 0.03A TO 8A STEP LOAD

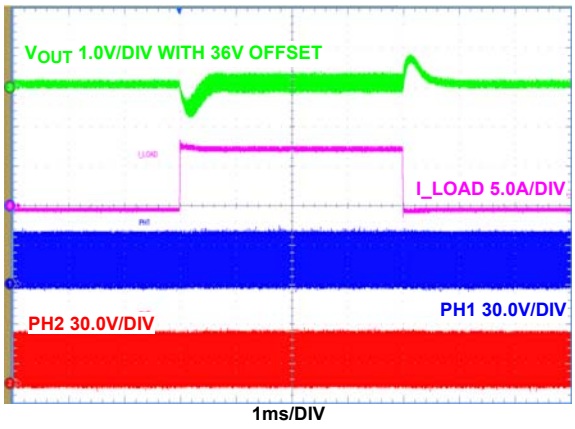


FIGURE 31. CCM MODE (DE/PHDRP = GND), TRANSIENT RESPONSE, I_{OUT} = 0A TO 8A STEP LOAD

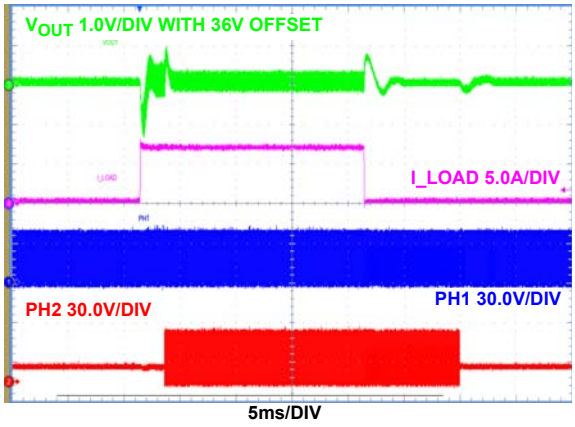


FIGURE 32. DE+PH_DROP MODE (DE/PHDRP = FLOAT), TRANSIENT RESPONSE, I_{OUT} = 1A TO 8A STEP LOAD

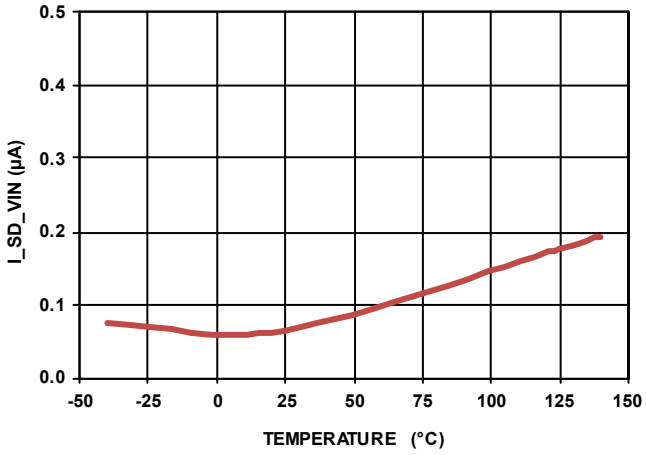


FIGURE 33. SHUTDOWN CURRENT AT THE VIN PIN I_SD vs TEMPERATURE, V_{IN} = 55V

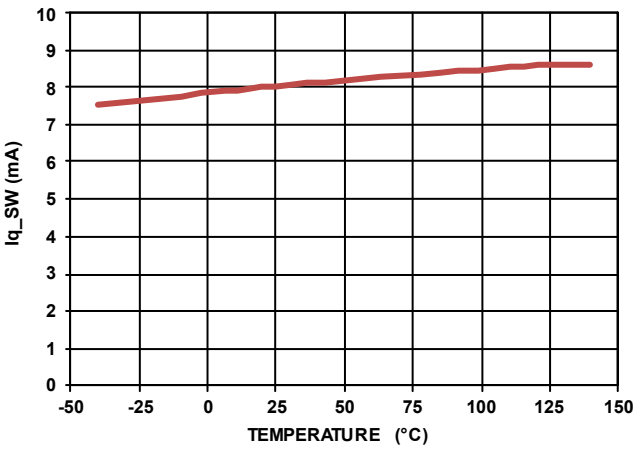


FIGURE 34. IC OPERATIONAL QUIESCENT CURRENT vs TEMPERATURE, IC SWITCHING, NO LOAD ON LGX AND UGX

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C. **(Continued)**

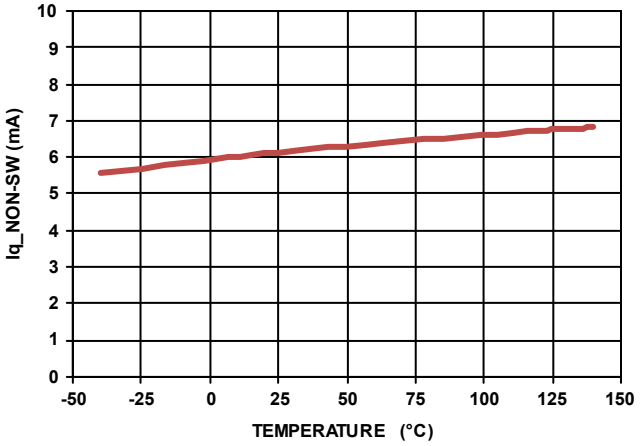


FIGURE 35. IC OPERATIONAL QUIESCENT CURRENT vs TEMPERATURE, IC NOT SWITCHING

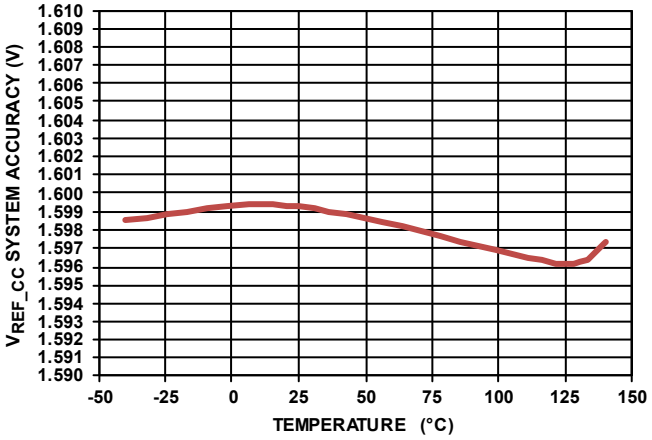


FIGURE 36. V_{REF_CC} SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE IMON PIN, VREF_CC = 1.6V

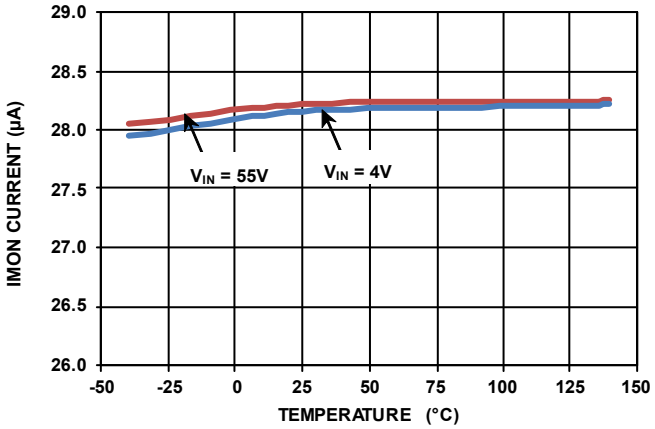


FIGURE 37. IMON OUTPUT CURRENT ACCURACY (CURRENT-SENSING SIGNAL OUTPUT) vs TEMPERATURE, V_{RSENx} = 30mV, R_{SETx} = 665Ω (0.1%)

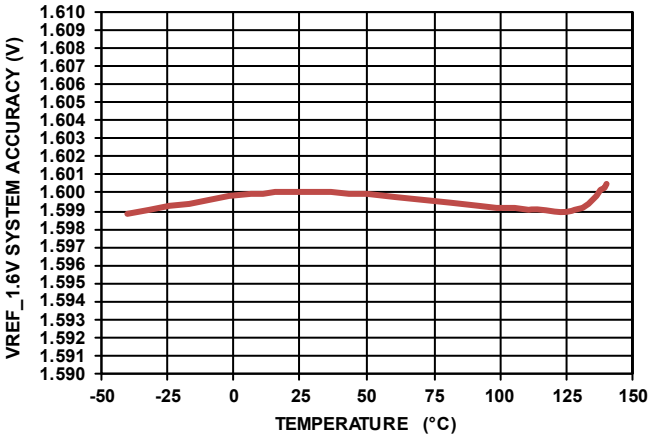


FIGURE 38. VREF_1.6V SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN

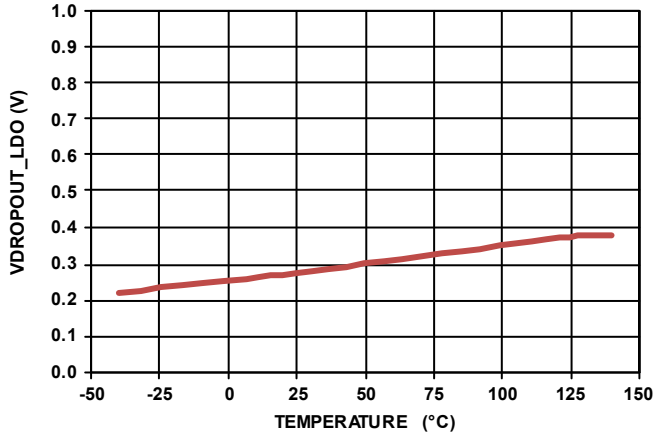


FIGURE 39. INTERNAL LDO DROPOUT VOLTAGE vs TEMPERATURE, 80mA LOAD CURRENT ON LDO OUTPUT (PVCC)

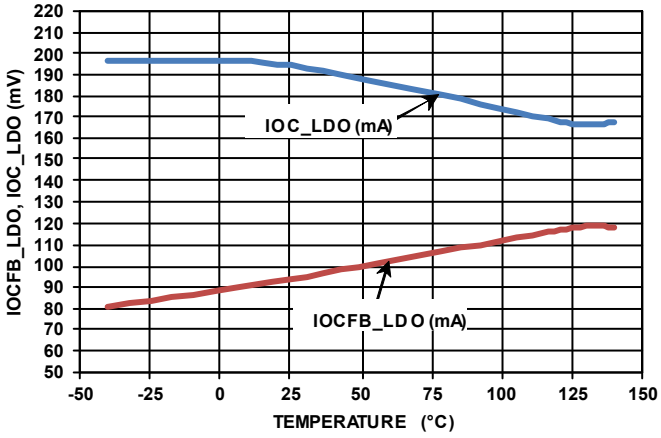


FIGURE 40. INTERNAL LDO OVERCURRENT THRESHOLD AND ITS FOLDBACK OVERCURRENT THRESHOLD vs TEMPERATURE

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C. **(Continued)**

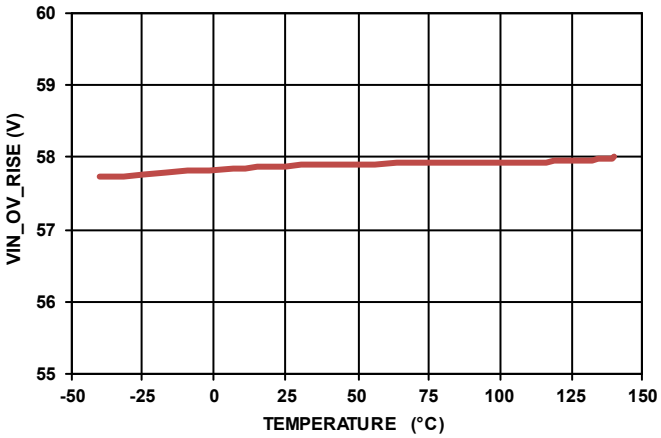


FIGURE 41. V_{IN} OV RISING THRESHOLD vs TEMPERATURE

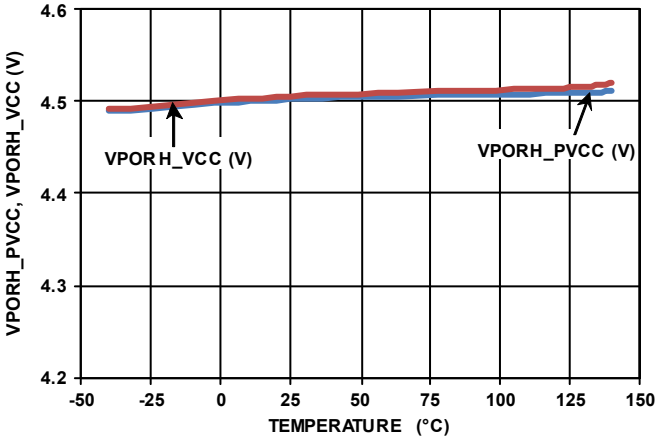


FIGURE 42. PVCC/VCC POR RISING THRESHOLD vs TEMPERATURE

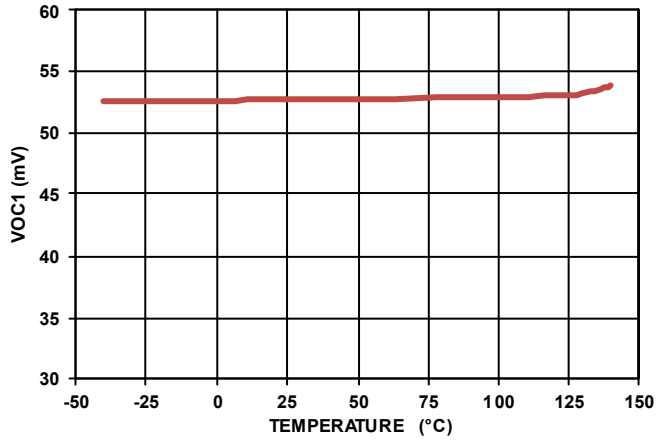


FIGURE 43. OC1 VOLTAGE THRESHOLD (ACROSS RSEN) vs TEMPERATURE

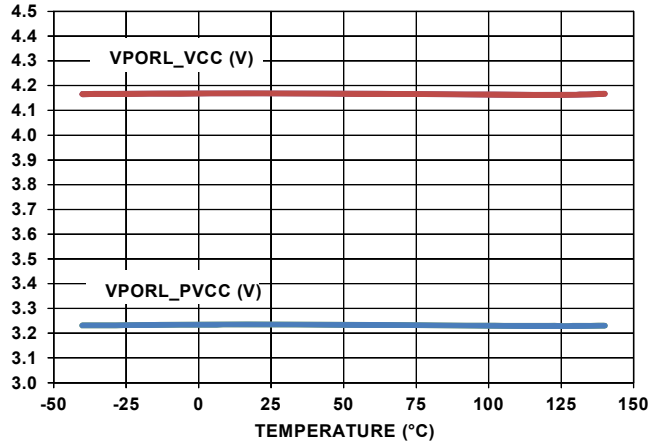


FIGURE 44. PVCC/VCC POR FALLING THRESHOLD vs TEMPERATURE

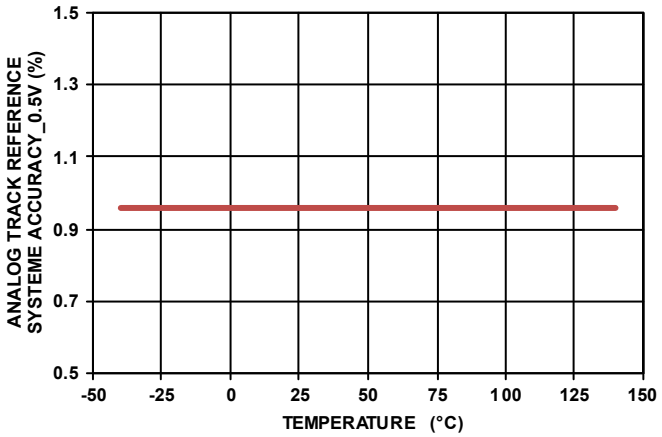


FIGURE 45. ANALOG TRACKING REFERENCE SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN, V_{TRACK} = 0.5V

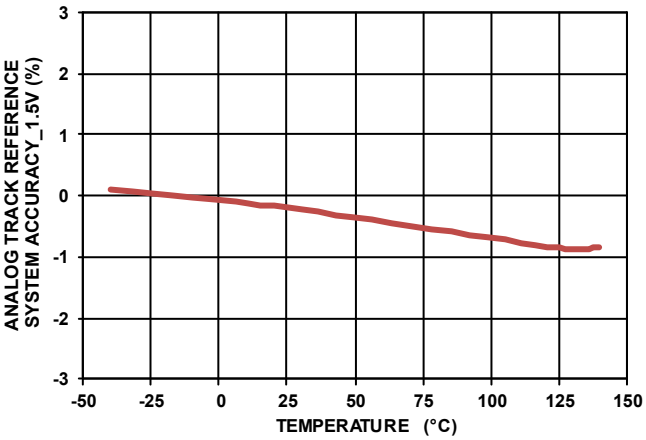


FIGURE 46. ANALOG TRACKING REFERENCE SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN, V_{TRACK} = 1.5V

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V, and T_A = +25°C. **(Continued)**

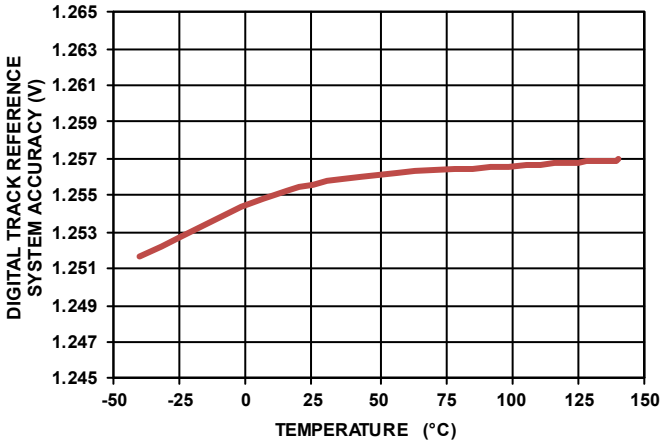


FIGURE 47. DIGITAL TRACKING REFERENCE SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN, DUTY CYCLE OF TRACK PIN SIGNAL IS 0.5

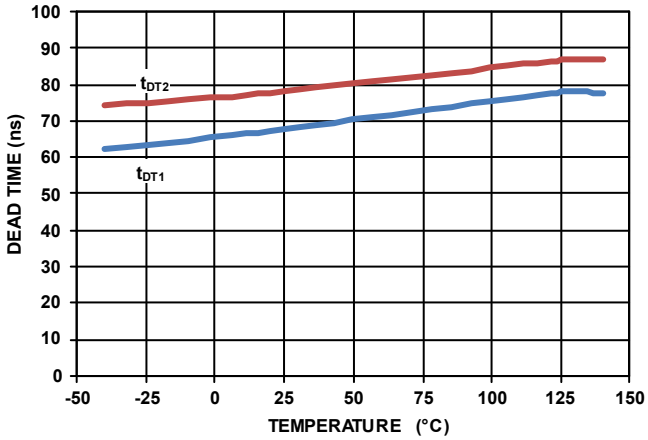


FIGURE 48. GATE DRIVE DEAD TIME vs TEMPERATURE, R_{DT} = 10k, t_{DT1} REFERS TO UG FALLING TO LG RISING, t_{DT2} REFERS TO LG FALLING TO UG RISING

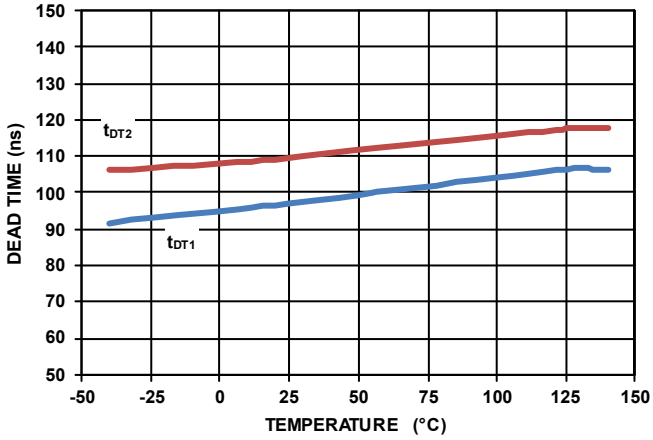


FIGURE 49. GATE DRIVE DEAD TIME vs TEMPERATURE, R_{DT} = 18.2k, t_{DT1} REFERS TO UG FALLING TO LG RISING, t_{DT2} REFERS TO LG FALLING TO UG RISING

Operation Description

The ISL78227 is a 2-phase, synchronous boost controller with integrated drivers. It supports wide input and output ranges of 5V to 55V during normal operation and the VIN pin withstands transients up to 60V.

The ISL78227 is integrated with 2A sourcing/3A sinking strong drivers to support high efficiency and high current synchronous boost applications. The drivers have a unique feature of adaptive dead time control of which the dead time can be programmed for different external MOSFETs, achieving both optimized efficiency and reliable MOSFET driving. The ISL78227 has selectable diode emulation and phase dropping functions for enhanced light-load efficiency.

The PWM modulation method is a constant frequency, Peak Current Mode Control (PCMC), which has benefits of input voltage feed-forward, a simpler loop to compensate compared to voltage mode control, and inherent current sharing capability.

The ISL78227 offers a track function with unique features of accepting either digital or analog signals for the user to adjust reference voltage externally. The digital signal track function greatly reduces the complexity of the interface circuits between the central control unit and the boost regulator. Equipped with cycle-by-cycle positive and negative current limiting, the track function can be reliably facilitated to achieve an envelope tracking feature in audio amplifier applications, which can significantly improve system efficiency.

In addition to the cycle-by-cycle current limiting, the ISL78227 is implemented with a dedicated, average Constant Current (CC) control loop for input current. For devices having only peak current limiting, the average current under peak current limiting varies significantly because the inductor ripple varies with changes of V_{IN} and V_{OUT} and tolerances of f_{SW} and inductors. The ISL78227's unique CC control feature accurately controls the average input current accurately to be constant without shutdown. Under certain constant input voltage, this means constant power limiting, which is especially useful for the boost converter. It helps the user optimize the system with the power devices' capability fully utilized by well-controlled constant input power.

The following sections describe the details of the functions.

Synchronous Boost

To improve efficiency, the ISL78227 employs synchronous boost architecture as shown in Figure 4 on page 8. The UGx output drives the high-side synchronous MOSFET, which replaces the freewheeling diode and reduces the power losses due to the voltage drop of the freewheeling diode.

While the boost converter is operating in steady state Continuous Conduction Mode (CCM), each phase's low-side MOSFET is controlled to turn on with duty cycle D and ideally, the upper MOSFET is ON for (1-D). Equation 1 shows the input to output voltage DC transfer function for boost is:

$$V_{OUT} = \frac{V_{IN}}{1-D} \quad \text{(EQ. 1)}$$

DRIVER CONFIGURATION

As shown in Figure 4 on page 8, the upper side UGx drivers are biased by the C_{BOOTx} voltage between BOOTx and PHx **(where "x" indicates the specific phase number and same note applied throughout this document)**. C_{BOOTx} is charged by a charge pump mechanism. PVCC charges BOOTx through the Schottky diode D_{BOOTx} when LGx is high, pulling PHx low. BOOTx rises with PHx and maintains the voltage to drive UGx as the D_{BOOTx} is reverse biased.

At start-up, charging to C_{BOOTx} from 0 to ~4.5V causes PVCC to dip slightly. So a typical 5.1Ω resistor R_{PVCCBT} is recommended between PVCC and D_{BOOTx} to prevent PVCC from falling below VPORL_PVCC. The typical value for C_{BOOTx} is 0.47µF.

The BOOTx to PHx voltage is monitored by UVLO circuits. When BOOTx to PHx falls below a 3V threshold, the UGx output is disabled. When BOOTx to PHx rises back above this threshold plus 150mV hysteresis, the high-side driver output is enabled.

For standard boost applications when upper side drivers are not needed, both UG1 and UG2 can be disabled by connecting either BOOT1 or BOOT2 to ground before part start-up initialization. PHx should be connected to ground.

PROGRAMMABLE ADAPTIVE DEAD TIME CONTROL

The UGx and LGx drivers are designed to have an adaptive dead time algorithm that optimizes operation with varying operating conditions. In this algorithm, the device detects the off timing of LGx (UGx) voltages before turning on UGx (LGx).

In addition to the adaptive dead time control, the dead time between UGx ON and LGx ON can be programmed by the resistor at the RDT pin while the adaptive dead time control is still functioning at the same time. The typical range of programmable dead time is 55ns to 200ns, or larger. This is intended for different external MOSFETs applications to adjust the dead time, maximizing the efficiency while at the same time preventing shoot-through. Refer to Figure 50 on page 25 for the selection of the RDT resistor and dead time, where t_{DT1} refers to the dead time between UG Falling to LG Rising, and t_{DT2} refers to the dead time between LG Falling to UG Rising. The dead time is smaller with a lower value RDT resistor, and it is clamped to minimum 57ns when RDT is shorted to ground. Because a current as large as 4mA is pulled from the RDT pin if the RDT pin is shorted to ground, it is recommended to use 5kΩ as the smallest value for the RDT resistor where the current drawing from the RDT pin is 0.5V/5kΩ = 100µA.

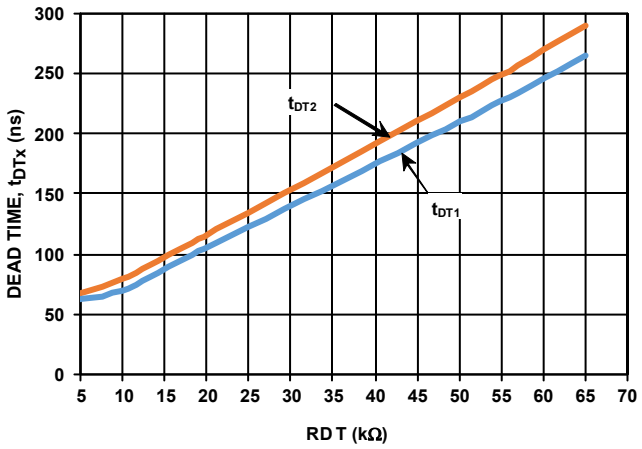


FIGURE 50. DEAD TIME vs RDT, t_{DT1} REFERS TO UG FALLING TO LG RISING, t_{DT2} REFERS TO LG FALLING TO UG RISING

PWM Control

The ISL78227 uses fixed frequency peak current mode control architecture. As shown in Figure 3 on page 7 and the typical schematic diagram (Figure 4 on page 8), error amplifier (Gm1) compares the FB pin voltage and reference voltage and generates a voltage loop error signal at the COMP pin. This error signal is compared with the current ramp signal (VRAMP) by the PWM comparator. The PWM comparator output combined with fixed frequency clock signal controls the SR flip-flop to generate the PWM signals (refer to "Peak Current Mode Control" on page 26).

OUTPUT VOLTAGE REGULATION LOOP

The resistor divider R_{FB2} and R_{FB1} from V_{OUT} to FB (Figure 4 on page 8) can be selected to set the desired V_{OUT}. V_{OUT} can be calculated by Equation 2.

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad \text{(EQ. 2)}$$

where in normal operation after soft-start, V_{REF} can be either VREF_1.6V or VREF_TRK, whichever is lower.

Gm1 has three inputs for reference voltage: soft-start ramp SS, VREF_TRK, and VREF_1.6V. The Gm1 uses the lowest value among SS, VREF_TRK, and VREF_1.6V. SS, VREF_TRK, and VREF_1.6V are valid for Gm1 during and after soft-start. In general operation, VREF_TRK is normally HIGH before soft-start and SS normally ramps up from a voltage lower than VREF_TRK and VREF_1.6V, in which case SS controls the output voltage ramp-up during soft-start. After soft-start is complete, the user can adjust VREF_TRK for the desired voltage. Because VREF_TRK is valid before soft-start, setting VREF_TRK lower than SS can make the SS ramp ineffective because Gm1 uses the lower VREF_TRK voltage. In such a case, the VREF_TRK becomes the real soft-start ramp that controls the output voltage ramp-up.

Digital/Analog Track Function

The TRACK input provides an external reference voltage to be applied for the output voltage loop to follow, which is useful if the user wants to change the output voltage as required. An example is to employ envelope tracking technology in audio power amplifier applications. The ISL78227 boost stage output is powering the audio power amplifier stage input, where the boost output tracks the music envelope signal applied at the TRACK pin. Ultimately, higher system efficiency can be achieved.

The TRACK pin can accept either a digital signal or an analog signal by configuring the ATRK/DTRK pin to be connected to ground or VCC. Figure 51 on page 26 shows the track function block diagram. VREF_TRK is fed into Gm1 as one of the reference voltages. The Gm1 takes the lowest voltage of SS, VREF_TRK, and VREF_1.6V as the actual reference. When VREF_TRK is the lowest voltage, it becomes the actual reference voltage for Gm1 and the output voltage can be adjusted with TRACK signal changes. Regarding the effective VREF_TRK range:

- There is no limit for the minimum voltage on the TRACK pin, but note the lower reference voltage and the lower voltage feedback regulation accuracy. Note the SS_DONE signal is checking VREF_TRK ≥0.3V as one of the conditions (refer to Figure 58 on page 29 and the t_8-t_9 description on page 29). Also, for the boost converter, the regulated output minimum voltage is usually the input voltage minus the upper MOSFET's body diode drop, in which case, the corresponding voltage at FB voltage is the minimum effective voltage for the VREF_TRK.
- The Gm1 takes the lowest voltage of SS, VREF_TRK, and VREF_1.6V as the actual reference. The maximum effective range for VREF_TRK is determined by VREF_1.6V or SS signal, whichever is lower. For example, after soft-start, when the SS pin equals to 3.47V (typical), the maximum effective voltage for VREF_TRK is 1.6V (VREF_1.6V).

When ATRK/DTRK = GND (DTRK mode), the TRACK pin accepts digital signal inputs. VREF_TRK (as one of the references input for the error amplifier Gm1) equals to the average duty cycle value of the PWM signal's at the TRACK pin. As shown in Figure 51 on page 26, the MUX is controlled by the ATRK/DTRK pin configurations. When ATRK/DTRK = GND, the MUX connects the output of the Q1 and Q2 switch bridge to the input of a 2-stage RC filter (R_1, C_1, R_2, and C_2). The PWM signal at the TRACK pin controls Q1 and Q2 to chop the 2.5V internal reference voltage. The phase node of Q1 and Q2 is a PWM signal with accurate 2.5V amplitude and duty cycle D, where D is the input PWM duty cycle on the TRACK input pin. The RC filter smooths out the PWM AC components and the voltage VREF_TRK after the RC filter becomes a DC voltage equal to 2.5V*D:

$$V_{REFTRK} = 2.5 \cdot D \quad \text{(EQ. 3)}$$

According to Equation 3, the PWM signals' amplitude at the TRACK pin does not affect the VREF_TRK accuracy and only the duty cycle value changes the VREF_TRK value. In general, the VREF_TRK reference accuracy is as good as the 2.5V reference. The built-in low pass filter (R_1, C_1, R_2, and C_2) converts the PWM signal's duty cycle value to a low noise reference. The low pass filter has a cutoff frequency of 1.75kHz and a gain of -40dB at 400kHz. The

2.5V PWM signal at phase node of Q1 and Q2 has around 25mV at VREF_TRK, which is 1.56% of 1.6V reference. This will not affect the boost output voltage because of the limited bandwidth of the system. A frequency of 400kHz is recommended for the PWM signal at the TRACK pin. Lower frequency at the TRACK input is possible, but VREF_TRK has a higher AC ripple. Bench test evaluation is needed to make sure the output voltage is not affected by this VREF_TRK AC ripple.

When ATRK/DTRK = VCC (ATRK mode), the MUX connects the TRACK pin voltage to the input of the 2-stage RC filter $R_1/C_1/R_2/C_2$. The TRACK pin accepts analog signal inputs, with the Gm1's VREF_TRK input equal to the voltage on the TRACK pin. The low-pass filter has the same cutoff frequency of 1.75kHz.

If not used, the TRACK pin should be left floating or tied to VCC and the internal VREF_1.6V working as the reference.

The TRACK function is enabled before the SS pin soft-start. The V_{OUT} reference can be controlled by TRACK inputs at start-up. After the SS pin ramps up to the upper clamp AND the VREF_TRK reaches 0.3V, the upper side FET is controlled to turn on gradually to achieve smooth transitions from DCM mode to CCM mode, of which the transition duration is 100ms (when set at CCM mode). After this transition, PGOOD is allowed to be pulled HIGH as long as output voltage is in regulation (within OV/UV threshold).

The maximum TRACK reference frequency for the boost V_{OUT} to track (VREF_TRK at Figure 51) is limited by the boost converter's loop bandwidth. Generally, the tracking reference signal's frequency should be 10 times lower than the boost loop crossover frequency. Otherwise, the boost output voltage cannot track the tracking reference signal and the output voltage is distorted. For example, for a boost converter with 4kHz loop crossover frequency, the boost can track reference signals up to 400Hz, typically. Figures 23 and 24 on page 19 show performances tracking 100Hz and 300Hz signals.

PEAK CURRENT MODE CONTROL

As shown in Figure 3 on page 7, each phase's PWM operation is initialized by the fixed clock for this phase from the oscillator (refer to "Oscillator and Synchronization" on page 27). The clocks for Phase 1 and Phase 2 are 180° out of phase. The low-side MOSFET is turned on (LGx) by the clock (after a dead time delay of t_{DT1}) at the beginning of a PWM cycle and the inductor current ramps up. The ISL78227's Current Sense Amplifiers (CSA) sense each phase inductor current and generate the current sense signal I_{SENx}. The I_{SENx} is added with the compensating slope and generates V_{RAMPx}. When V_{RAMPx} reaches the error amplifier (Gm1) output voltage, the PWM comparator is triggered and LGx is turned off to shut down the low-side MOSFET. The low-side MOSFET stays off until the next clock signal comes for the next cycle.

After the low-side MOSFET is turned off, the high-side MOSFET turns on after dead time t_{DT2}. The turn-off time of the high-side MOSFET is determined by either the PWM turn-on time at the next PWM cycle, or when the inductor current becomes zero if the Diode Emulation mode is selected.

Multiphase Power Conversion

For an n-phase, interleaved, multiphase boost converter, the PWM switching of each phase is distributed evenly with 360°/n phase shift. The total combined current ripples at the input and output are reduced where smaller input and output capacitors can be used. In addition, it is beneficial to have a smaller equivalent inductor for a faster loop design. Also in some applications, especially in a high current case, multiphase makes it possible to use a smaller inductor for each phase rather than one big inductor (single-phase), which is sometimes more costly or unavailable on the market at the high current rating. Smaller size inductors also help to achieve low profile design.

The ISL78227 is a controller for 2-phase interleaved converter where the two phases are operating with 180° phase shift, meaning each PWM pulse is triggered 1/2 of a cycle after the start of the PWM pulse of the previous phase. Figure 52 on page 27 illustrates the interleaving effect on input ripple current. The AC component of the two phase currents (I_{L1} and I_{L2}) are interleaving each other and the combined AC current ripple ($I_{L1} + I_{L2}$) at input are reduced. Equivalently, the frequency of the AC inductor ripple at input is two times of the switching frequency per phase.

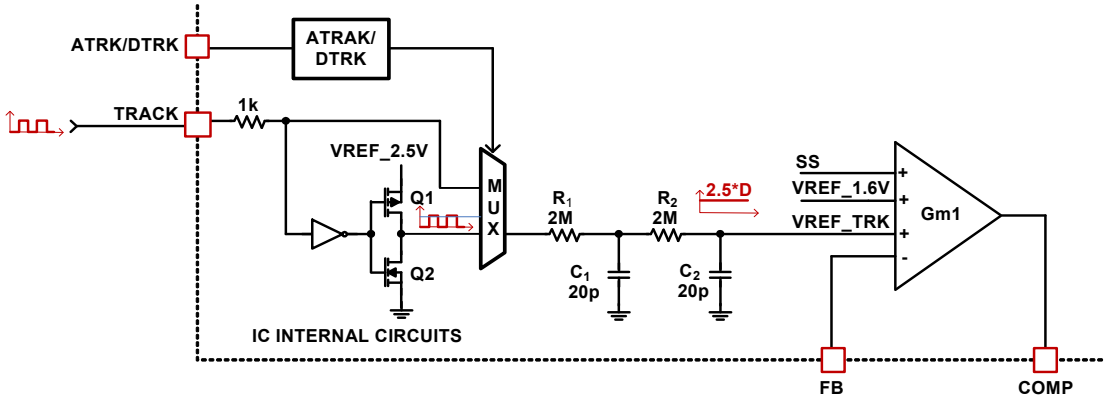


FIGURE 51. TRACK FUNCTION BLOCK DIAGRAM

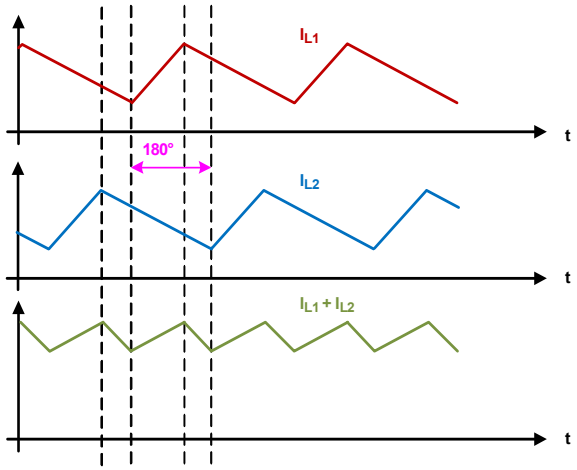


FIGURE 52. PHASE NODE AND INDUCTOR-CURRENT WAVEFORMS FOR 2-PHASE CONVERTER

To understand the reduction of the ripple current amplitude in the multiphase circuit, refer to Equation 4, which represents an individual phase's peak-to-peak inductor current.

In Equation 4, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-phase inductor value, and f_{SW} is the switching frequency.

$$I_{PPCH} = \frac{(V_{OUT} - V_{IN})V_{IN}}{L f_{SW} V_{OUT}} \quad \text{(EQ. 4)}$$

The input capacitors conduct the ripple component of the inductor current. In the case of a 2-phase boost converter, the capacitor current is the sum of the ripple currents from each of the individual phases. Use Equation 5 to calculate the peak-to-peak ripple of the total input current which goes through the input capacitors, where K_{P-P} can be found in Figure 53 under the specific duty cycle.

$$I_{PPALL} = K_{P-P} \cdot I_{PPCH} \quad \text{(EQ. 5)}$$

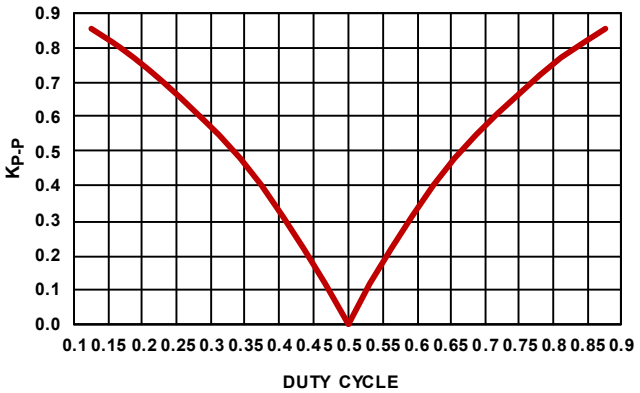


FIGURE 53. K_{P-P} vs DUTY CYCLE

CURRENT SHARING BETWEEN PHASES

The peak current mode control inherently has current sharing capability. As shown in Figure 3 on page 7, the current sense ramp, V_{RAMPx}, of each phase is compared to the same error amplifier's output at the COMP pin by the PWM comparators to turn off LGx when V_{RAMPx} reaches COMP. Thus, the V_{RAMPx} peaks are controlled to be the same for each phase. V_{RAMPx} is the sum of instantaneous inductor current sense ramp and the compensating slope. Because the compensating slopes are the same for both phases, the inductor peak current of each phase is controlled to be the same.

The same mechanism applies if multiple ISL78227s are configured in parallel for a multiphase boost converter. The COMP pin of each ISL78227 is tied together for each phase's current sense ramp peak to be compared with the same COMP voltage (V_{RAMPx} = COMP), thus, the inductor peak currents of all the phases are controlled to be the same. The "4-Phase Operation" section describes how to configure two ISL78227s in parallel for a 4-phase, interleaved boost converter.

4-PHASE OPERATION

Two ISL78227s can be used in parallel to achieve interleaved 4-phase operation. Figure 54 shows the recommended configuration. The CLKOUT from the master IC drives FSYNC of the slave IC to synchronize the switching frequencies. This achieves a 90° phase shift for the four phases switching and the respective COMP, FB, SS, EN, and IMON pins of the two ICs are connected.

CLKOUT is 90° out-of-phase with the rising edge of LG1. Therefore, the two phases of the second IC are interleaved with the two phases of the first IC.

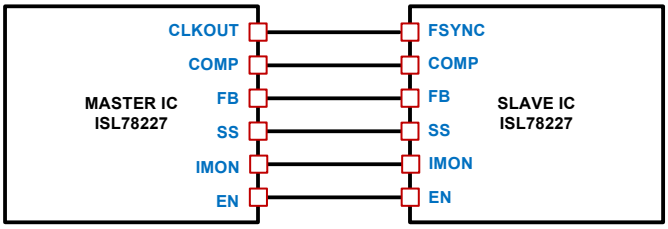


FIGURE 54. CONFIGURATIONS FOR DUAL IC, 4-PHASE OPERATION

Oscillator and Synchronization

The switching frequency is determined by the selection of the frequency-setting resistor, R_{FSYNC}, connected from the FSYNC pin to GND. Equation 6 is provided to assist in selecting the correct resistor value, where f_{SW} is the switching frequency of each phase.

$$R_{FSYNC} = 2.49 \times (10)^{10\left(\frac{0.505}{f_{SW}} - 5.5 \times 10^{-8}\right)} \quad \text{(EQ. 6)}$$

Figure 55 shows the relationship between R_{FSYNC} and switching frequency.

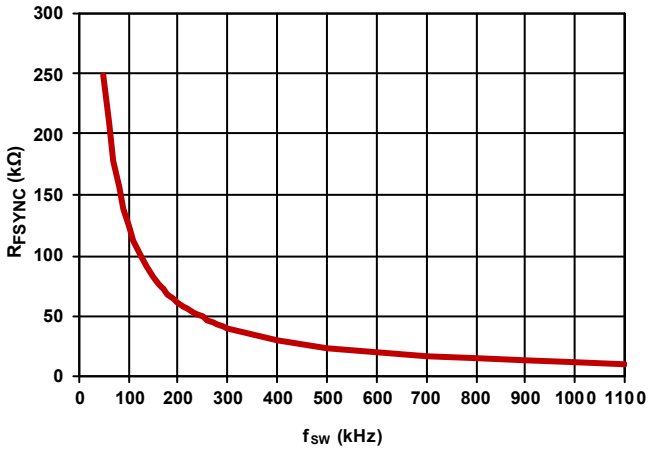


FIGURE 55. f_{SW} vs R_{FS}

The ISL78227 contains a Phase Lock Loop (PLL) circuit. Referring to Figure 4 on page 8, the PLL is compensated with a series resistor-capacitor (R_{PLL} and C_{PLL1}) from the PLLCOMP pin to GND and a capacitor (C_{PLL2}) from PLLCOMP to GND. At the 300kHz switching frequency, typical values are R_{PLL} = 3.24kΩ, C_{PLL1} = 6.8nF, and C_{PLL2} = 1nF. The PLL locking time is around 0.7ms. Generally, the same PLL compensating network can be used in the frequency range of 50kHz to 1.1MHz. With the same PLL compensation network, at a frequency range higher than 500kHz, the PLL is overcompensated. However, the PLL is stable just with slow frequency response. If a faster frequency response is required at a higher operating frequency, the PLL compensation network can be tuned to have a faster response. An Excel spreadsheet to calculate the PLL compensation is provided on the ISL78227 product page.

The ISL78227's switching frequency can be synchronized to the external clock signals applied at the FSYNC pin. The ISL78227 detects the input clock's rising edge and synchronizes the rising edge of LG1 to the input clock's rising edge with a dead time delay of t_{DT1}. The switching frequency of each phase equals the fundamental frequency of the clock input at FSYNC. Because the ISL78227 detects only the edge of the input clock instead of its pulse width, the input clock's pulse width can be as low as 20ns (as minimum), tens of ns, or hundreds of ns, depending on the capability of the specific system to generate the external clock.

The CLKOUT pin outputs a clock signal with the same frequency of the per-phase switching frequency. Its amplitude is V_{CC} and the pulse width is 1/12 of the per-phase switching period (t_{SW}/12). Figure 56 shows the application example to put two ISL78227s in parallel for 4-phase, interleaved operation, with the master IC's CLKOUT being connected to the FSYNC pin of the slave IC. The master IC outputs CLKOUT signal with a delay of $t_{SW}/4 - t_{DT1}$ after LG1_master. The slave IC FSYNC pin takes the CLKOUT_master as the input and the slave's IC LG1 is delayed by a time of 35ns + t_{DT1}. Therefore, the LG1_slave is delayed by $t_{SW}/4$+35ns to LG1_master, which is approximately a 90° phase shift. With 90°phase shift between LG1 and respective LG2 for each IC, an interleaved 4-phases with 90° phase shift boost is achieved.

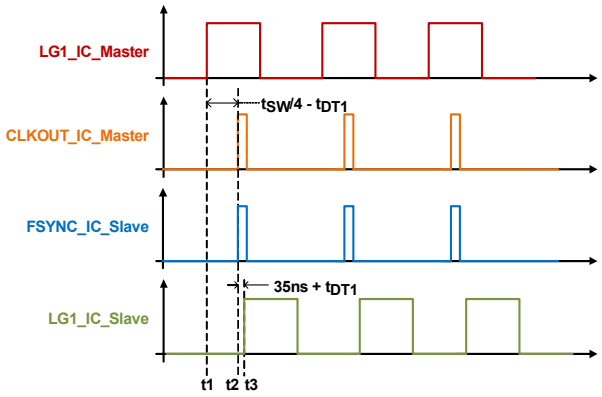


FIGURE 56. TIMING DIAGRAM OF CLKOUT vs LG1 AND FSYNC vs LG1 (CLKOUT_MASTER CONNECTED TO FSYNC_SLAVE)

After the ISL78227 latches to being synchronized with the external clock, if the external clock on the FSYNC pin is removed, the switching frequency oscillator shuts down. The part then detects PLL_LOCK fault (refer to Table 3 on page 34), and goes to either Hiccup mode or Latch-off mode, depending on the HIC/LATCHOFF pin configuration. If the part is set in Hiccup mode, it restarts with frequency set by the resistor at the FSYNC pin.

The switching frequency range of the ISL78227 set by R_{FSYNC} or by synchronization is typically 50kHz to 1.1MHz.

The low end 50kHz is determined by a PLL_LOCK fault protection, which shuts down the IC when frequency is lower than 37kHz typical.

The phase dropping mode is **not allowed** with external synchronization.

MINIMUM ON-TIME (BLANK TIME) CONSIDERATION

The minimum ON-time (also called BLANK time) of LGx is the minimum ON pulse width as long as LGx is turned ON. It is also intended for the internal circuits to blank out the noise spikes after LGx turns on. The t_{MINON} can be programmed by a resistor at the RBLANK pin.

The selection of the t_{MINON} depends on two considerations.

1. The noise spike durations after LGx turns on, which is normally in a range of tens of ns to 100ns or longer, depending on the external MOSFET switching characteristic and noise coupling path to current sensing.
2. Ensure the charging of the boot capacitor during operations of LGx operating at t_{MINON}. One typical case is an operation when the input voltage is close to the output voltage. The duty cycle is smallest at t_{MINON}, and C_{BOOTx} is charged by PVCC via D_{BOOTx} with short duration of t_{MINON} minus the delay to pull phase low. If such operation is required, especially when a large MOSFET with large Q_g is used to support heavy load application, larger t_{MINON} can be programmed with the resistor at the RBLANK pin to ensure C_{BOOTx} can be sufficiently charged during minimum duty cycle operation.

Refer to Figure 57 for the selection of RBLANK resistor and t_{MINON} time. A 5kΩ resistor is recommended as the minimum R_{BLANK} resistor.

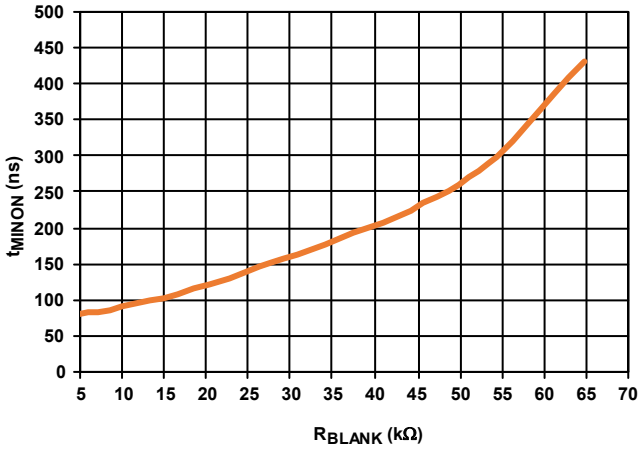


FIGURE 57. t_{MINON} vs RBLANK

Operation Initialization and Soft-Start

Before converter initialization, the EN pin voltage must be higher than its rising threshold and the PVCC/VCC pin must be higher than the rising POR threshold. When these conditions are met, the controller begins initialization and soft-start. Figure 58 shows the ISL78227 internal start-up timing diagram from the power-up to soft-start.

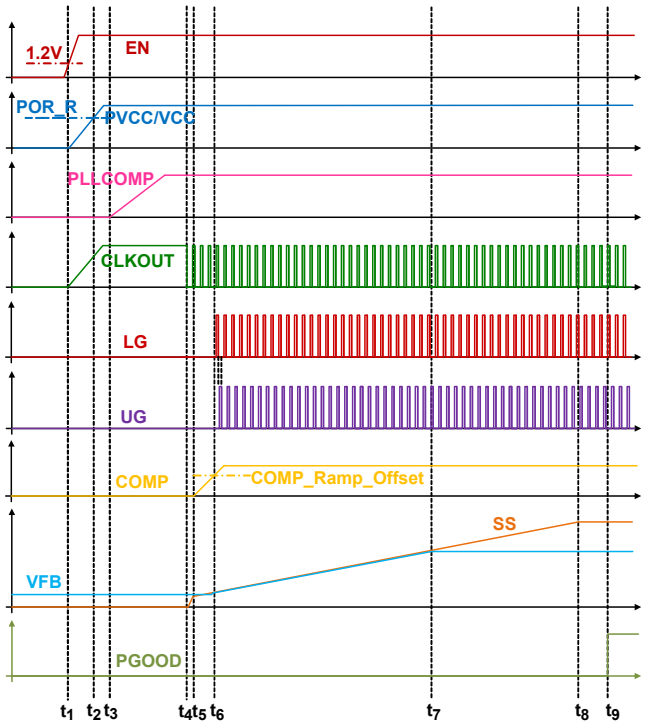


FIGURE 58. CIRCUIT INITIALIZATION AND SOFT-START

Assuming input voltage is applied to the VIN pin before t_1 and VCC is connected to PVCC, as shown on Figure 58, the descriptions for start-up procedures are described as follows:

t_1 - t_2: The enable comparator holds the ISL78227 in shutdown until the V_{EN} rises above 1.2V (typical) at the time of t_1. During t_1 - t_2, $V_{PVCC/VCC}$ gradually increases and reaches the internal Power-On Reset (POR) rising threshold 4.5V (typical) at t_2.

t_2 - t_3: During t_2 - t_3, the ISL78227 self-calibrates to detect certain pin configurations (HIC/LATCH, DE/PHDRP, ATRK/DTRAK) to latch in the selected operation modes. The time duration for t_2 - t_3 is typically 195µs.

t_3 - t_4: During this period, the ISL78227 waits until the internal PLL circuits are locked to the preset oscillator frequency. When PLL locking is achieved at t_4, the oscillator generates output at the CLK_OUT pin. The time duration for t_3 - t_4 depends on the PLLCOMP pin configuration. The PLL is compensated with a series resistor-capacitor (R_{PLL} and C_{PLL1}) from the PLLCOMP pin to GND and a capacitor (C_{PLL2}) from PLLCOMP to GND. At the 300kHz switching frequency, typical values are R_{PLL} = 3.24kΩ, C_{PLL1} = 6.8nF, and C_{PLL2} = 1nF. With this PLLCOMP compensation, the time duration for t_3 - t_4 is around 0.7ms.

t_4 - t_5: During this period, the PLL locks the frequency t_4 and the system prepares to soft-start. The ISL78227 has one unique feature to pre-bias the SS pin voltage to be equal to V_{FB} during t_4 - t_5, which is around 50µs.

t_5 - t_6: At t_5, the soft-start ramps up at the SS pin (V_{SSPIN}) and the COMP voltage starts to ramp up as well. Drivers are enabled but not switching during t_5 - t_6 because the COMP is still below the current sense ramp offset. The device operates in diode emulation mode during soft-start period t_5 - t_8. The slew rate of the SS ramp and the duration of t_5 - t_8 are determined by the capacitor used at the SS pin.

t_6 - t_7: At t_6, COMP is above the current sense ramp offset and the drivers start switching. Output voltage ramps up while FB voltage is following SS ramp during this soft-start period. At t_7, output voltage reaches the regulation level and FB voltage reaches VREF_1.6V.

t_7 - t_8: At this stage, SS continues ramping up until it reaches the SS clamp voltage ($V_{SSPCLAMP}$) 3.47V at t_8, indicating the SS pin ramp-up is completed. At t_8, the ISL78227 generates an internal SS_DONE signal, which goes HIGH when both V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥ 0.3V (as shown in Figure 3 on page 7). This indicates the soft-start has completed.

t_8 - t_9: After t_8, a delay time of either 0.5ms or 100ms is inserted before the PGOOD pin is released HIGH at t_9, depending on the selected mode (refer to Table 2 on page 33).

1. If the DE/PHDRP pin = VCC or FLOAT to have DE mode selected, the PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥0.3V to PGOOD rising is 0.5ms.
2. If the DE/PHDRP pin = GND to have CCM mode selected, the PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥0.3V to PGOOD rising is 100ms, during which period the device is transitioning from DE mode to CCM mode. The high-side gate UGx is controlled to gradually increase the ON-time to finally merge with CCM ON-time. This synchronous MOSFET “soft-ON” feature is unique and ensures smooth transition from DCM mode to CCM mode after soft-start completes. More importantly, this “SYNC FET soft-ON” function eliminates the large negative current, which often

occurs when starting up to a high pre-biased output voltage. This feature makes the system robust for all the challenging start-up conditions and greatly improves the system reliability.

Enable

To enable the device, the EN pin needs to be driven higher than 1.2V (typical) by the external enable signal or resistor divider between VIN and GND. The EN pin has an internal, 5MΩ (typical), pull-down resistor. This pin also has an internal 5.2V (typical) clamp circuit with a 5kΩ (typical) resistor in series to prevent excess voltage applied to the internal circuits. When applying the EN signal using resistor divider from VIN, internal pull-down resistance needs to be considered. Also, the resistor divider ratio needs to be adjusted as its EN pin input voltage may not exceed 5.2V.

To disable or reset all fault status, the EN pin needs to be driven lower than 1.1V (typical). When the EN pin is driven low, the ISL78227 turns off all of the blocks to minimize the off-state quiescent current.

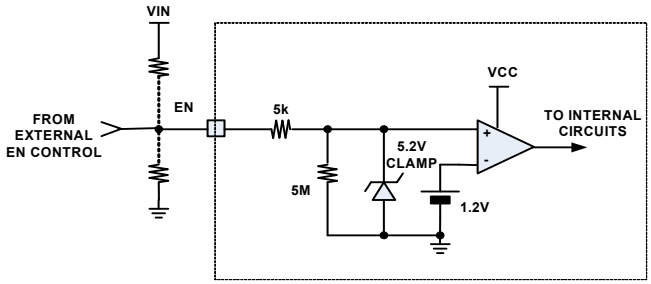


FIGURE 59. ENABLE BLOCK

Soft-Start

Soft-start is implemented by an internal 5µA current source charging the soft-start capacitor (C_{SS}) at SS to ground. The voltage on the SS pin slowly ramps up as the reference voltage for the FB voltage to follow during soft-start.

Typically, for boost converter before soft-start, its output voltage is charged up to be approximately a diode drop below the input voltage through the upper side MOSFETs' body diodes. To more accurately correlate the soft-start ramp time to the output voltage ramp time, the ISL78227 SS pin voltage is pre-biased with voltage equal to FB voltage before soft-start begins. The soft-start ramp time for the boost output voltage ramping from V_{IN} to the final regulated voltage V_{OUTreg}, can be calculated by Equation 7, where V_{REF} is 1.6V (VREF_1.6V) with the TRACK pin tied HIGH:

$$t_{SS} = V_{REF} \cdot \left(1 - \frac{V_{IN}}{V_{OUTreg}}\right) \cdot \frac{C_{SS}}{5\mu A} \quad \text{(EQ. 7)}$$

PGOOD Signal

The PGOOD pin is an open-drain logic output to indicate that the soft-start period is completed, the input voltage is within safe operating range, and the output voltage is within the specified range. The PGOOD comparator monitors the FB pin to check if the output voltage is within 80% to 120% of the reference voltage VREF_1.6V.

As described at the t_8 - t_9 duration in "Operation Initialization and Soft-Start" on page 29, the PGOOD pin is pulled low during soft-start and it is released high after SS_DONE with a 0.5ms or 100ms delay.

PGOOD is pulled low if any of the comparators for FB_UV, FB_OV or VIN_OV, is triggered for a duration longer than 10µs.

In normal operation after start-up, under fault recovery, PGOOD is released high with the same 0.5ms delay time after the fault is removed.

Current Sense

The ISL78227 peak current control architecture senses the inductor current continuously for fast response. A sense resistor is placed in series with the power inductor for each phase. The ISL78227 Current Sense Amplifiers (CSA) continuously sense the respective inductor current as shown in Figure 60 on page 31 by sensing the voltage signal across the sense resistor, R_{SENx} (where "x" indicates the specific phase number and same note applied throughout this document). The sensed current for each active phase is used for peak current mode control loop, phase current balance, individual phase cycle-by-cycle peak current limiting (OC1), individual phase overcurrent fault protection (OC2_PEAK), input average Constant Current (CC) control and average overcurrent protection (OC_AVG), diode emulation, and phase drop control. The internal circuitry shown in Figure 60 represents a single phase. This circuitry is repeated for each phase.

CURRENT SENSE FOR INDIVIDUAL PHASE - I_{SENX}

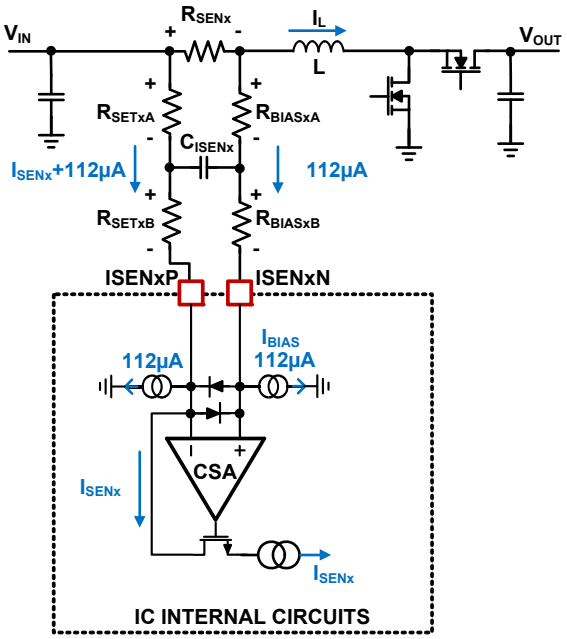


FIGURE 60. CURRENT-SENSING BLOCK DIAGRAM

The RC network between the R_{SENx} and ISENxP/N pins as shown in Figure 60 is the recommended configuration. The ISENxP pin should be connected to the positive potential of the R_{SEN_CHx} through resistor R_{SETx}, where in Figure 60, R_{SETx} is composed by R_{SETxA} plus R_{SETxB}. R_{SET} is used to set the current sense gain externally.

$$R_{SETx} = R_{SETxA} + R_{SETxB} \quad \text{(EQ. 8)}$$

Because there is an 112µA bias current sinking to each of the ISENxP and ISENxN pins, R_{BIASx} with the same value to R_{SETx} should be placed between the ISENxN pin to the low potential of the R_{SENx}, where in Figure 60, R_{BIASx} is composed by R_{BIASxA} plus R_{BIASxB}.

$$R_{BIASx} = R_{BIASxA} + R_{BIASxB} \quad \text{(EQ. 9)}$$

$$R_{BIASx} = R_{SETx} \quad \text{(EQ. 10)}$$

It is recommended to have $R_{SETxA} = R_{BIASxA}$ and $R_{SETxB} = R_{BIASxB}$, and insert a capacitor (C_{ISENx}) between them as shown in Figure 60. This will form a symmetric noise filter for the small current sense signals. The differential filtering time constant equals to $(R_{SETxA}+R_{BIASxA})*C_{ISENx}$. This time constant is typically selected in range of tens of ns depending on the actual noise levels.

CSA generates the sensed current signal I_{SENx} by forcing ISENxP voltage to be equal to ISENxN voltage. Because R_{SETx} is equal to R_{BIASx}, the voltage drop across R_{SETx} and R_{BIASx} incurred by the fixed 112µA bias current cancels each other. Therefore, the resulting current at CSA output I_{SENx} is proportional to each phase inductor current, I_{Lx}. I_{SENx} per phase can be derived in Equation 11, where I_{Lx} is the per-phase current flowing through R_{SENx}.

$$I_{SENx} = I_{Lx} \cdot \frac{R_{SENx}}{R_{SETx}} \quad \text{(EQ. 11)}$$

R_{SENx} is normally selected with smallest resistance to minimize the power loss on it. With R_{SENx} selected, R_{SETx} is selected by the desired cycle-by-cycle peak current limiting level OC1 (refer to "Peak Current Cycle-by-Cycle Limiting (OC1)" on page 35).

AVERAGE CURRENT SENSE FOR TWO PHASES - IMON

The IMON pin serves to monitor the total average input current of the 2-phase boost. As shown in Figure 3 on page 7, the individual current sense signals (I_{SENx}) are divided by eight and summed together. A 17µA offset current is added to form a current source output at the IMON pin with the value calculated as shown in Equation 12.

$$IMON = \left(\frac{I_{L1} \cdot R_{SEN1}}{R_{SET1}} + \frac{I_{L2} \cdot R_{SEN2}}{R_{SET2}}\right) \cdot 0.125 + 17 \cdot 10^{-6} \quad \text{(EQ. 12)}$$

Assume $R_{SEN1} = R_{SEN2}$, $R_{SET1} = R_{SET2}$, and $I_{IN} = I_{L1} + I_{L2}$, which is the total boost input average current:

$$IMON = I_{IN} \cdot \frac{R_{SEN}}{R_{SET}} \cdot 0.125 + 17 \cdot 10^{-6} \quad \text{(EQ. 13)}$$

As shown in Figure 4 on page 8, a resistor R_{IMON} is placed between the IMON pin and ground, which turns the current sense output from the IMON pin to a voltage V_{IMON}. A capacitor C_{IMON} should be used in parallel with R_{IMON} to filter out the ripple such that V_{IMON} represents the total average input current of the 2-phase boost. V_{IMON} can be calculated using Equation 14.

$$V_{IMON} = IMON \cdot R_{IMON} \quad \text{(EQ. 14)}$$

As shown in Figure 3 on page 7, V_{IMON} is sent to inputs of Gm2 and comparators of CMP_PD and CMP_OCAVG for the following functions:

1. V_{IMON} is compared with 1.6V (VREF_CC) at error amplifier Gm2 inputs to achieve constant current control function. The CC control threshold for the boost input current is typically set in a way that the per-phase average inductor current (when CC control) is lower than the per-phase cycle-by-cycle peak current limiting (OC1) threshold. Refer to "Constant Current Control (CC)" on page 35 for detailed descriptions.
2. V_{IMON} is compared with phase dropping thresholds (1.1V falling to drop Phase 2, 1.15V rising to add Phase 2). Refer to "Automatic Phase Dropping/Adding" on page 33 for detailed descriptions.
3. V_{IMON} is compared with 2V for OC_AVG fault protections. Refer to "Average Overcurrent Fault (OC_AVG) Protection" on page 36 for detailed descriptions.

The typical scenario when fast overloading is applied is described as follows: When a large overload is suddenly applied at boost output, the phase inductor peak currents are initially limited by OC1 cycle-by-cycle, during which time the IMON voltage slowly rises due to the filter delay of R_{IMON} and C_{IMON}. When V_{IMON} reaches 1.6V, the CC loop starts to limit and control the average current to be constant, which lowers the inductor current (as described previously, CC threshold normally is set lower than the OC1 cycle-by-cycle limiting threshold). Typically, tens of nF are used for C_{IMON}. When a longer time delay is needed, larger C_{IMON} can be used. Refer to "Constant Current Control (CC)" on page 35 for a more detailed description.

Adjustable Slope Compensation

For a boost converter with peak current mode control, slope compensation is needed when the duty cycle is larger than 50%. It is advised to add slope compensation when the duty cycle is approximately 30% to 40% because a transient load step can push the duty cycle higher than the steady state level. When slope compensation is too low, the converter suffers from subharmonic oscillation, which may result in noise emissions at half the switching frequency. On the other hand, overcompensation of the slope may reduce the phase margin. Therefore, proper design of the slope compensation is needed.

The ISL78227 features adjustable slope compensation by setting the resistor value, R_{SLOPE}, from the SLOPE pin to ground. This function eases the compensation design and provides more flexibility in choosing the external components.

Figure 61 shows the block diagram related to slope compensation. For current mode control, in theory, the compensation slope slew rate m_{SL} needs to be larger than 50% of the inductor current down ramp slope slew rate m_b.

Equation 15 shows the resistor value, R_{SLOPE}, at the SLOPE pin to create a compensation ramp:

$$R_{SLOPE} = \frac{6.67 \cdot 10^5 \cdot L_x \cdot R_{SETx}}{K_{SLOPE} \cdot (V_{OUT} - V_{IN}) \cdot R_{SENx}} (\Omega) \quad \text{(EQ. 15)}$$

where K_{SLOPE} is the selected gain of compensation slope over inductor down slope. For example, K_{SLOPE} = 1 gives the R_{SLOPE} value generating a compensation slope equal to inductor current down ramp slope. Theoretically, the K_{SLOPE} needs to be larger than 0.5, but practically more than 1.0 is used in the actual application. To cover the operating range, the maximum of V_{OUT} and minimum of V_{IN} should be used in Equation 15 to calculate the R_{SLOPE}.

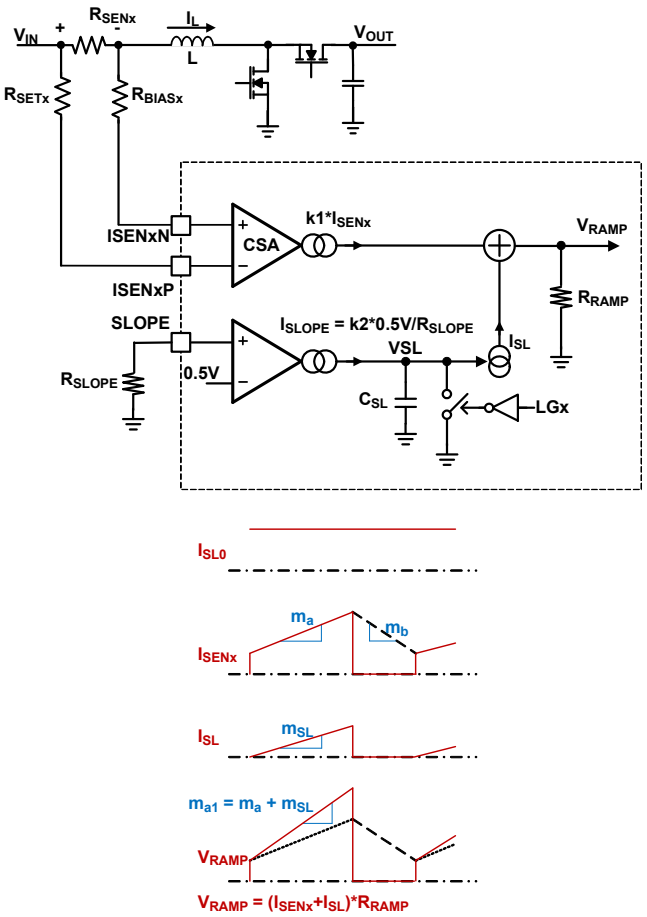


FIGURE 61. SLOPE COMPENSATION BLOCK DIAGRAM

Light-Load Efficiency Enhancement

For switching mode power supplies, the total loss is related to conduction loss and switching loss. The conduction loss dominates at heavy load, while the switching loss dominates at light-load condition. Therefore, if a multiphase converter is running at a fixed phase number for the entire load range, the efficiency starts to drop significantly below a certain load current. The ISL78227 has selectable automatic phase dropping, cycle-by-cycle diode emulation and pulse skipping features to enhance the light-load efficiency. By observing the total input current on-the-fly and dropping an active phase, the system can achieve optimized efficiency over the entire load range.

The Phase Dropping (PH_DROP) and Diode Emulation (DE) functions can be selected to be active or inactive by setting the DE/PHDRP pin. Refer to Table 2 on page 33 for the three configuration modes.

1. When DE/PHDRP = V_{CC}, Diode Emulation function is enabled and Phase Drop function is disabled.
2. When DE/PHDRP = FLOAT, both Diode Emulation and Phase Drop functions are enabled.
3. When DE/PHDRP = GND, both Diode Emulation and Phase Drop functions are disabled. The part is set in Continuous Conduction Mode (CCM).

TABLE 2. CCM/DE/PH_DROP MODE SETTING (DE/PHDRP PIN)

MODE NUMBER (NAME)	DE/PHDRP PIN SETTING	DE MODE	PHASE-DROP MODE
1 (DE)	VCC	Enabled	Disabled
2 (DE+PH_DROP)	FLOAT	Enabled	Enabled
3 (CCM)	GND	Disabled	Disabled

AUTOMATIC PHASE DROPPING/ADDING

When the Phase Drop function is enabled, the ISL78227 automatically drops or adds Phase 2 by comparing the V_{IMON} to the phase dropping/adding thresholds. V_{IMON} is proportional to the average input current indicating the level of the load.

The phase dropping mode is **not allowed** with external synchronization.

Phase Dropping

When load current drops and V_{IMON} falls below 1.1V, Phase 2 is disabled. For better transient response during phase dropping, the ISL78227 gradually reduces the duty cycle of the phase from steady state to zero, typically within 8 to 10 switching cycles. This gradual dropping scheme helps smooth the change of the PWM signal and stabilizes the system when phase dropping happens.

From Equations 13 and 14, the phase dropping current threshold level for the total, 2-phase boost input current can be calculated by Equation 16.

$$I_{INphDRP} = \left(\frac{1.1}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot \frac{R_{SET}}{R_{SEN}} \cdot 8(A) \quad \text{(EQ. 16)}$$

Phase Adding

Phase adding is decided by the two mechanisms listed below. Phase 2 is added immediately if either of the two following conditions are met.

1. V_{IMON} >1.15V, the IMON pin voltage is higher than phase adding threshold 1.15V. The phase adding current threshold level for the total 2-phase boost input current can be calculated by Equation 17.

$$I_{INphADD} = \left(\frac{1.15}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot \frac{R_{SET}}{R_{SEN}} \cdot 8(A) \quad \text{(EQ. 17)}$$

2. I_{SENx} >80µA (OC1), individual phase current triggers OC1.

The first is similar to the phase dropping scheme. When the load increases causing V_{IMON} >1.15V, Phase 2 is added back immediately to support the increased load demand. Because the IMON pin normally has large RC filter and V_{IMON} is average current signal, this mechanism has a slow response and is intended for slow load transients.

The second mechanism is intended to handle the case when load increases quickly. If the quick load increase triggers OC1 (I_{SENx} >80µA) in either of the two phases, Phase 2 is added back immediately.

After Phase 2 is added, the phase dropping function is disabled for 1.5ms. After this 1.5ms expires, the phase dropping circuit is activated again and Phase 2 can be dropped automatically as usual.

DIODE EMULATION AT LIGHT-LOAD CONDITION

When the Diode Emulation mode (DE) is selected to be enabled (Mode 1 and Mode 2 in Table 2), the ISL78227 has cycle-by-cycle diode emulation operation at light load achieving Discontinuous Conduction Mode (DCM) operation. With DE mode operation, negative current is prevented and the conduction loss is reduced, therefore, high efficiency can be achieved at light-load conditions.

Diode emulation occurs during t_5-t_8 (on Figure 58 on page 29), regardless of the DE/PHDRP operating modes (Table 2).

PULSE SKIPPING AT DEEP LIGHT-LOAD CONDITION

If the converter enters Diode Emulation mode and the load is still reducing, eventually pulse skipping occurs to increase the deep light-load efficiency. Either Phase 1, Phase 2, or both, pulse skips at these deep light-load conditions.

Fault Protections/Indications and Current Limiting

The ISL78227 is implemented with comprehensive fault protections/indications and current limitings to design a highly reliable boost converter. Most of the fault protections' responses can be selected to be either Hiccup or Latch-off by configuring the HIC/LATCH pin, which offers the flexibility upon the specific requirements for different applications.

SELECTABLE HICCUP OR LATCH-OFF FAULT RESPONSE

Table 3 on page 34 lists the fault protections that can have either Hiccup or Latch-off fault response determined by HIC/LATCH pin configurations.

- When the HIC/LATCH pin is pulled high (VCC), the fault response is in Hiccup mode.
- When the HIC/LATCH pin is pulled low (GND), the fault response is in Latch-off mode.

In Hiccup mode, the device stops switching when a fault condition in Table 3 on page 34 is detected, and restarts from soft-start after 500ms (typical). This operation is repeated until fault conditions are completely removed.

In Latch-off mode, the device stops switching when a fault condition in Table 3 on page 34 is detected and PWM switching being kept off even after fault conditions are removed. In Latch-off status, the internal LDO is alive to keep PVCC voltage regulated. By either toggling the EN pin or cycling VCC/PVCC below the POR threshold restarts the system.

TABLE 3. FAULT NAMES LIST FOR THE HICCUP OR LATCH-OFF FAULT RESPONSE

FAULT NAME	FAULT RESPONSE HIC/LATCH = VCC: HICCUP HIC/LATCH = GND: LATCH-OFF	DESCRIPTION
VIN_OV	Set by the HIC/LATCH pin	Input overvoltage fault (VIN_PIN >58V) protection response is Hiccup when HIC/LATCH = VCC, and Latch-off when HIC/LATCH = GND
OC_AVG	Set by the HIC/LATCH pin	Input average overcurrent fault (IMON_PIN >2V) protection response is Hiccup when HIC/LATCH = VCC, and Latch-off when HIC/LATCH = GND
OC2_PEAK	Set by the HIC/LATCH pin	Peak overcurrent fault (I_{SENx} >105µA) protection response is Hiccup when HIC/LATCH = VCC, and Latch-off when HIC/LATCH = GND
VOUT_OV	Set by the HIC/LATCH pin	Output overvoltage fault (FB_PIN >120%*VREF_1.6V) protection response is Hiccup when HIC/LATCH = VCC, and Latch-off when HIC/LATCH = GND
PLLCOMP_SHORT	Set by the HIC/LATCH pin	PLLCOMP_SHORT fault (PLLCOMP_PIN >1.7V) protection response is Hiccup when HIC/LATCH = VCC, and Latch-off when HIC/LATCH = GND
PLL_LOCK	Set by the HIC/LATCH pin	PLL fault (detect the minimum frequency of 37kHz as typical) protection response is Hiccup when HIC/LATCH = VCC, and Latch-off when HIC/LATCH = GND

INPUT OVERVOLTAGE FAULT PROTECTION

As shown in Figure 3 on page 7, the ISL78227 monitors the VIN pin voltage divided by 48 (VIN/48) as the input voltage information. This fault detection is active at the beginning of soft-start (t_5 as shown in Figure 58 on page 29).

The VIN_OV comparator compares VIN/48 to 1.21V reference to detect if VIN_OV fault is triggered. Equivalently, when V_{IN} >58V (for 5µs), VIN_OV fault event is triggered. The PGOOD pin is pulled low.

At the same time the VIN_OV fault condition is triggered, the ISL78227 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode, depending on HIC/LATCH pin configuration as described in "Selectable Hiccup or Latch-Off Fault Response" on page 33 and Table 3 on page 34.

Under the selection of Hiccup response for the VIN_OV fault, when the output voltage falls lower than the VIN_OV threshold 58V, the device returns to normal switching through Hiccup soft-start. PGOOD is released to be pulled high after a 0.5ms delay.

OUTPUT OVERVOLTAGE FAULT PROTECTION

The ISL78227 monitors the FB pin voltage to detect if an output overvoltage fault (VOUT_OV) occurs. This fault detection is active at the beginning of soft-start (t_5 as shown in the Figure 58 on page 29).

If the FB pin voltage is higher than 120% of the voltage regulation reference, VREF_1.6V, the VOUT_OV comparator is triggered to indicate an VOUT_OV fault and the PGOOD pin is pulled low.

At the same time, when a VOUT_OV fault is triggered, the ISL78227 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode, depending on HIC/LATCH pin configuration as described in "Selectable Hiccup or Latch-Off Fault Response" on page 33 and Table 3 on page 34.

Under the selection of Hiccup response for the VOUT_OV fault, when the output voltage falls down to be lower than the VOUT_OV threshold of 120% * VREF_1.6V minus 4% hysteresis, the device returns to normal switching through Hiccup soft-start. The PGOOD pin is released to be pulled high after 0.5ms delay.

Equivalently, the V_{OUT} overvoltage threshold is set at the same percentage of V_{OUT} target voltage V_{OUT_TARGET} (set by VREF_1.6V) because the device uses the same FB voltage to regulate the output voltage with the same resistor divider between V_{OUT} and the FB pin (refer to Equation 2 on page 25). Therefore, the V_{OUT} overvoltage protection threshold is set at 120% of V_{OUT_TARGET}. According to Equation 2 on page 25, the V_{OUT} overvoltage protection threshold can be calculated using Equation 18.

$$VOUT_{OVP} = 1.2 \cdot 1.6 \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad \text{(EQ. 18)}$$

OUTPUT UNDERVOLTAGE INDICATION

The ISL78227 monitors the FB pin voltage to detect if an output undervoltage (VOUT_UV) occurs.

If the FB pin voltage is lower than 80% of the voltage regulation reference VREF_1.6V, the VOUT_UV comparator is triggered to indicate VOUT_UV occurring and the PGOOD pin is pulled low. However, there is no fault protection action for the VOUT_UV condition; the ISL78227 continues PWM switching and normal operation when VOUT_UV occurs.

When the output voltage rises back above the VOUT_UV threshold of 80% * VREF_1.6V plus 4% hysteresis, PGOOD is released to be pulled high after a 0.5ms delay.

Equivalently, the V_{OUT} undervoltage threshold is set at the same percentage of V_{OUT} target voltage V_{OUT_TARGET} (set by VREF_1.6V) because the device uses the same FB voltage to regulate the output voltage with the same resistor divider between V_{OUT} and the FB pin (refer to Equation 2 on page 25). Therefore, the V_{OUT} undervoltage threshold is set at 80% of V_{OUT_TARGET}. According to Equation 2 on page 25, the V_{OUT} undervoltage protection threshold can be calculated using Equation 19.

$$VOUT_{UV} = 0.8 \cdot 1.6 \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad \text{(EQ. 19)}$$

OVERCURRENT LIMITING AND FAULT PROTECTION

The ISL78227 has multiple levels of overcurrent protection/limiting. Each phase's peak inductor current is protected from overcurrent conditions by limiting its peak current. The combined total current is protected on an average basis. Also, each phase is implemented with instantaneous, cycle-by-cycle negative current limiting (OC_NEG_TH = -48µA).

Peak Current Cycle-by-Cycle Limiting (OC1)

Each individual phase's inductor peak current is protected with cycle-by-cycle peak current limiting (OC1) **without** triggering Hiccup or Latch-off shutdown of the IC. The controller continuously compares the CSA output current sense signal, I_{SENx} (calculated by Equation 11 on page 31) to an overcurrent limiting threshold (OC1_TH = 80µA) in every cycle. When I_{SENx} reaches 80µA, the respective phase's LGx is turned off to stop inductor current further ramping up. In such a way, peak current cycle-by-cycle limiting is achieved.

The equivalent cycle-by-cycle peak inductor current limiting for OC1 can be calculated using Equation 20:

$$I_{OC1x} = 80 \cdot 10^{-6} \cdot \frac{R_{SETx}}{R_{SENx}}(A) \quad \text{(EQ. 20)}$$

Negative Current Cycle-by-Cycle Limiting (OC_NEG)

Each individual phase's inductor current is protected with cycle-by-cycle negative current limiting (OC_NEG) **without** triggering Hiccup or Latch-off shutdown of the IC. The controller continuously compares the CSA output current sense signal, I_{SENx}, (calculated by Equation 11 on page 31) to a negative current limiting threshold (OC_NEG_TH = -48µA) in every cycle. When I_{SENx} falls below -48µA, the respective phase's UGx is turned off to stop the inductor current further ramping down. In such a way, negative current cycle-by-cycle limiting is achieved.

The equivalent negative inductor current-limiting level can be calculated by Equation 21:

$$I_{OCNEGx} = -48 \cdot 10^{-6} \cdot \frac{R_{SETx}}{R_{SENx}}(A) \quad \text{(EQ. 21)}$$

Peak Overcurrent Fault (OC2_PEAK) Protection

If either of the two individual phase's current sense signals I_{SENx} (calculated by Equation 11 on page 31) reaches 105µA (OC2_TH = 105µA) for three consecutive switching cycles, the Peak Overcurrent fault (OC2_PEAK) is triggered. The ISL78227 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode depending on HIC/LATCH pin configuration as described in "Selectable Hiccup or Latch-Off Fault Response" on page 33 and Table 3 on page 34.

This fault protection is intended to protect the device by shutdown (Hiccup or Latch-off) from the worst case condition where OC1 cannot limit the inductor peak current.

This fault detection is active at the beginning of soft-start (t_5 as shown in the Figure 58 on page 29).

Under the selection of Hiccup response for the OC2_PEAK fault, when both phases' peak current sense signals I_{SENx} no longer trip the OC2_PEAK thresholds (105µA), the device returns to normal switching and regulation through Hiccup soft-start.

The equivalent inductor peak current threshold for the OC2_PEAK fault protection can be calculated by Equation 22:

$$I_{OC2x} = 105 \cdot 10^{-6} \cdot \frac{R_{SETx}}{R_{SENx}}(A) \quad \text{(EQ. 22)}$$

Constant Current Control (CC)

A dedicated constant average Current Control (CC) loop is implemented in the ISL78227 to control the input current to be constant at overload conditions, which means constant input power control under certain constant input voltage.

As shown in Figure 3 on page 7, the V_{IMON} represents the total input average current and is sent to the error amplifier Gm2 input to be compared with the internal CC reference V_{REF_CC} (1.6V). Gm2 output is driving the COMP voltage through a diode, D_{CC}. Thus, the COMP voltage can be controlled by either Gm1 output or Gm2 output through D_{CC} depending on load conditions.

At normal operation without overloading, V_{IMON} is lower than the V_{REF_CC} (1.6V at default). Therefore, Gm2 output is HIGH and D_{CC} is reversely blocked and not forward conducting. In this case, the COMP voltage is controlled by the voltage loop error amplifier Gm1's output to have the output voltage regulated.

At input average current overloading case, when V_{IMON} reaches V_{REF_CC} (1.6V), Gm2 output falls, D_{CC} is forward conducting, and Gm2 output overrides Gm1 output to drive COMP. In this way, the CC loop overrides the voltage loop, meaning V_{IMON} is controlled to be constant and input average constant current operation is achieved. Under certain constant input voltage, input CC makes input power constant for the boost converter. Compared to peak current limiting schemes, the average constant current control is more accurate to control the average current to be constant, which is beneficial for the user to accurately control the maximum average power for the converter to handle.

The CC current threshold should be set lower than the OC1 peak current threshold with margin. Generally, the OC1 peak current threshold (per phase) is set 1.5 to 2 times higher than the CC current threshold (here referred to per phase average current).

This matches with the physics of the power devices that normally have higher transient peak current rating and lower average current ratings. The OC1 provides protection against the transient peak current. The CC controls the average current with slower response, but with much more accurate control of the maximum power the system has to handle at overloading conditions.

1. When fast changing overloading occurs, because V_{IMON} has a sensing delay of $R_{IMON}*C_{IMON}$, CC does not trip at the initial transient load current until it reaches the CC reference of 1.6V. OC1 is triggered at the beginning to limit the inductor peak current cycle-by-cycle.
2. After the delay of $R_{IMON}*C_{IMON}$, when V_{IMON} reaches the CC reference of 1.6V, CC control starts to work and limit duty cycles to reduce the inductor current and keep the sum of the two phases' inductor currents constant. The time constant of the $R_{IMON}*C_{IMON}$ is typically on the order of 10 times slower than the voltage loop bandwidth so that the two loops do not interfere with each other.

CC loop is active at the beginning of soft-start.

From Equations 13 and 14 on page 31, the constant current control current threshold level for the total 2-phase boost input current can be calculated by Equation 23.

$$I_{INCC} = \left(\frac{1.6}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot \frac{R_{SET}}{R_{SEN}} \cdot 8(A) \quad \text{(EQ. 23)}$$

Average Overcurrent Fault (OC_AVG) Protection

The ISL78227 monitors the IMON pin voltage (which represents the boost total input average current signal) to detect if the Average Overcurrent (OC_AVG) fault occurs. As shown in Figure 3 on page 7, the comparator CMP_OCAVG compares V_{IMON} to 2V threshold to detect this fault. This fault detection is active at the beginning of soft-start (t_5 as shown in Figure 58 on page 29).

When V_{IMON} is higher than 2V, the OC_AVG fault is triggered. The ISL78227 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode, depending on HIC/LATCH pin configuration as described in "Selectable Hiccup or Latch-Off Fault Response" on page 33 and Table 3 on page 34.

Under the selection of Hiccup response for the OC_AVG fault, when the IMON voltage falls to lower than the 2V threshold, the device returns to normal switching through Hiccup soft-start.

From Equations 13 and 14 on page 31, the OC_AVG fault's current threshold level for the total 2-phase boost input current can be calculated using Equation 24.

$$I_{INOCAVG} = \left(\frac{2}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot \frac{R_{SET}}{R_{SEN}} \cdot 8(A) \quad \text{(EQ. 24)}$$

Because the Constant Current Loop uses the same IMON signal and has a lower threshold (1.6V) than the OC_AVG threshold (2V), the OC_AVG can hardly be tripped. The CC loop limits the IMON signal around 1.6V, which is below 2V. Generally, the OC_AVG functions as a worst-case backup protection.

INTERNAL DIE OVER-TEMPERATURE PROTECTION

The ISL78227 PWM is disabled if the junction temperature reaches +160°C (typical) while the internal LDO is alive to keep PVCC/VCC biased (VCC connected to PVCC). A +15°C hysteresis ensures that the device restarts with soft-start when the junction temperature falls below +145°C (typical).

Internal 5.2V LDO

The ISL78227 has an internal LDO with input at VIN and a fixed 5.2V/100mA output at PVCC. The internal LDO tolerates an input supply range of VIN up to 55V (60V absolute maximum). A 10µF, 10V or higher X7R type of ceramic capacitor is recommended between PVCC to GND. At low VIN operation when the internal LDO is saturated, the dropout voltage from the VIN pin to the PVCC pin is typically 0.3V under 80mA load at PVCC, as shown in the "Electrical Specifications" table on page 9. This is one of the constraints to estimate the required minimum VIN voltage.

The output of this LDO is mainly used as the bias supply for the gate drivers. With VCC connected to PVCC as in the typical application, PVCC also supplies other internal circuitry. To provide a quiet power rail to the internal analog circuitry, it is recommended to place an RC filter between PVCC and VCC. A minimum of 1µF ceramic capacitor from VCC to ground should be used for noise decoupling purpose. Because PVCC is providing noisy drive current, a small resistor (10Ω or smaller) between the PVCC and VCC helps to prevent the noises from interfering from PVCC to VCC.

Figure 62 shows the internal LDO output voltage (PVCC) regulation versus its output current. The PVCC drops to 4.5V (typical) when the load is 195mA (typical) because of the LDO current-limiting circuits. When the load current further increases, the voltage drops further and finally enters current foldback mode where the output current is clamped to 100mA (typical). At the worst case when LDO output is shorted to ground, the LDO output is clamped to 100mA.

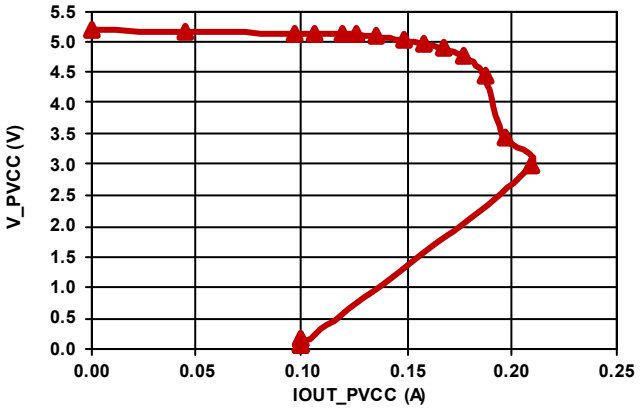


FIGURE 62. INTERNAL LDO OUTPUT VOLTAGE vs LOAD

Based on the junction to ambient thermal resistance, R_{JA}, of the package, the maximum junction temperature should be kept below +125°C. However, the power losses at the LDO need to be considered, especially when the gate drivers are driving external MOSFETs with large gate charges. At high V_{IN}, the LDO has significant power dissipation that may raise the junction temperature where the thermal shutdown occurs.

With an external PNP transistor as shown in Figure 63, the power dissipation of the internal LDO can be moved from the ISL78227 to the external transistor. Set R_S to 68Ω so that the LDO delivers about 10mA when the external transistor begins to turn on. The external circuit increases the minimum input voltage to approximately 6.5V.

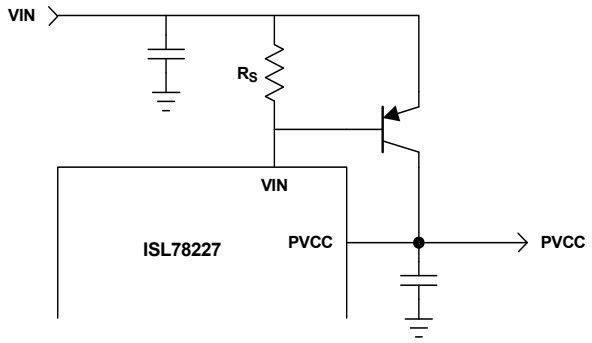


FIGURE 63. SUPPLEMENTING LDO CURRENT

Application Information

There are several ways to define the external components and parameters of boost regulators. This section shows one example of how to decide the parameters of the external components based on the typical application schematics as shown in Figure 4 on page 8. In the actual application, the parameters may need to be adjusted and additional components may be needed for the specific applications regarding noise, physical sizes, thermal, testing, and/or other requirements.

Output Voltage Setting

The Output Voltage (V_{OUT}) of the regulator can be programmed by an external resistor divider connecting from V_{OUT} to FB and FB to GND as shown in Figure 4 on page 8. Use Equation 2 on page 25 to calculate the desired V_{OUT}, where V_{REF} can be either VREF_1.6V or VREF_TRK, whichever is lower. In the actual application, the resistor value should be decided by considering the quiescent current requirement and loop response. Typically, between 4.7kΩ to 20kΩ is used for the R_{FB1}.

Switching Frequency

Switching frequency is determined by requirements of transient response time, solution size, EMC/EMI, power dissipation and efficiency, ripple noise level, input, and output voltage range. Higher frequency may improve the transient response and help to reduce the solution size. However, this may increase the switching losses and EMC/EMI concerns. Thus, a balance of these parameters is needed when deciding the switching frequency.

When the switching frequency f_{SW} is decided, the frequency setting resistor R_{FSYNC} can be determined by Equation 6 on page 27.

Input Inductor Selection

While the boost converter is operating in steady state Continuous Conduction Mode (CCM), the output voltage is determined by Equation 1 on page 24. With the required input and output voltage, duty cycle D can be calculated by Equation 25:

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad \text{(EQ. 25)}$$

where D is the on-duty of the boost low-side power transistor.

Under this CCM condition, the inductor peak-to-peak ripple current of each phase can be calculated using Equation 26:

$$I_{L(P\text{-}P)} = D \cdot T \cdot \frac{VIN}{L} \quad \text{(EQ. 26)}$$

where T is the switching cycle $1/f_{SW}$ and L is each phase inductor's inductance.

From the previous equations, the inductor value is determined using Equation 27:

$$L = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{V_{IN}}{I_{L(P\text{-}P)} \cdot f_{SW}} \quad \text{(EQ. 27)}$$

Use Equation 27 to calculate L, where values of V_{IN}, V_{OUT} and $I_{L(P\text{-}P)}$ are based on the considerations described in following:

- One method is to select the minimum input voltage and the maximum output voltage under long term operation as the conditions to select the inductor. In this case, the inductor DC current is the largest.
- The general rule to select the inductor is to have its ripple current $I_{L(P\text{-}P)}$ around 30% to 50% of maximum DC current. The individual maximum DC inductor current for the 2-phase boost converter can be calculated using Equation 28, where P_{OUTmax} is the maximum DC output power, and EFF is the estimated efficiency:

$$I_{Lmax} = \frac{P_{OUTmax}}{V_{INmin} \cdot EFF \cdot 2} \quad \text{(EQ. 28)}$$

Using Equation 27 with the two conditions listed above, a reasonable starting point for the minimum inductor value can be estimated from Equation 29, where K is typically selected as 30%.

$$L_{min} = \left(1 - \frac{V_{INmin}}{V_{OUTmax}}\right) \cdot \frac{V_{INmin}^2 \cdot EFF \cdot 2}{P_{OUTmax} \cdot K \cdot f_{SW}} \quad \text{(EQ. 29)}$$

Increasing the value of the inductor reduces the ripple current and therefore, the ripple voltage. However, the large inductance value may reduce the converter's response time to a load transient. This also reduces the current sense ramp signal and may cause a noise sensitivity issue.

The peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current may be observed at some transient conditions like the start-up or heavy load transient. Therefore, the inductor's size needs to be determined with the consideration of these conditions. To avoid exceeding the inductor's saturation rating, OC1 peak current limiting (refer to "Peak Current Cycle-by-Cycle Limiting (OC1)" on page 35) should be selected below the inductor's saturation current rating.

Output Capacitor

To filter the inductor current ripples and to have sufficient transient response, output capacitors are required. A combination of electrolytic and ceramic capacitors is normally used.

The ceramic capacitors filter the high frequency spikes of the main switching devices. In layout, these output ceramic capacitors must be placed as close as possible to the main switching devices to maintain the smallest switching loop in layout. To maintain capacitance over the biased voltage and temperature range, good quality capacitors such as X7R or X5R are recommended.

The electrolytic capacitors normally handle the load transient and output ripples. The boost output ripples are mainly dominated by the load current and output capacitance volume.

For boost converter, the maximum output voltage ripple can be estimated using Equation 30, where I_{OUTmax} is the load current at output, C is the total capacitance at output, and D_{MIN} is the minimum duty cycle at VIN_{max} and $VOUT_{min}$.

$$V_{OUTripple} = \frac{I_{OUTmax} \cdot (1 - D_{MIN})}{C \cdot 2 \cdot f_{SW}} \quad \text{(EQ. 30)}$$

For 2-phase boost converter, the RMS current going through the output current can be calculated by Equation 30 for D > 0.5, where I_L is per phase inductor DC current. For D < 0.5, time domain simulation is recommended to get the accurate calculation of the input capacitor RMS current.

$$I_{CoutRMS} = I_L \cdot \sqrt{(1 - D) \cdot (2D - 1)} \quad \text{(EQ. 31)}$$

It is recommended to use multiple capacitors in parallel to handle this output RMS current.

Input Capacitor

Depending upon the system input power rail conditions, the aluminum electrolytic type capacitor is normally used to provide a stable input voltage. The input capacitor should be able to handle the RMS current from the switching power devices. Refer to Equation 5 and Figure 53 on page 27 to estimate the RMS current the input capacitors need to handle.

Ceramic capacitors must be placed near the VIN and PGND pin of the IC. Multiple ceramic capacitors including 1µF and 0.1µF are recommended. Place these capacitors as close as possible to the IC.

Power MOSFET

The external MOSFETs driven by the ISL78227 controller must be carefully selected to optimize the design of the synchronous boost regulator.

The MOSFET's BV_{DSS} rating must have enough voltage margin against the maximum boost output voltage plus the phase node voltage transient spikes during switching.

As the UG and LG gate drivers are 5V output, the MOSFET V_{GS} need to be in this range.

The MOSFET should have low Total Gate Charge (Q_g), low ON-resistance ($r_{DS(ON)}$) at VGS = 4.5V, and small gate resistance (R_g <1.5Ω is recommended). It is recommended that the minimum V_{GS} threshold is higher than 1.2V, but does not exceed 2.5V, in order to prevent false turn-on by noise spikes due to high dv/dt during phase node switching and to maintain low $r_{DS(ON)}$ under limitation of maximum gate drive voltage, which is 5.2V (typical) for low-side MOSFET and 4.5V (typical) due to diode drop of boot diode for high-side MOSFET.

Bootstrap Capacitor

The power required for high-side MOSFET drive is provided by the boot capacitor connected between BOOT and PH pins. The bootstrap capacitor can be chosen using Equation 32:

$$C_{BOOT} > \frac{Q_{gate}}{dV_{BOOT}} \quad \text{(EQ. 32)}$$

where Q_{gate} is the total gate charge of the high-side MOSFET and dV_{BOOT} is the maximum droop voltage across the bootstrap capacitor while turning on the high-side MOSFET.

Though the maximum charging voltage across the bootstrap capacitor is PVCC minus the bootstrap diode drop (~4.5V), large excursions below GND by PH node requires at least 10V rating for this ceramic capacitor. To keep enough capacitance over the biased voltage and temperature range, a good quality capacitor such as X7R or X5R is recommended.

RESISTOR ON BOOTSTRAP CIRCUIT

In the actual application, sometimes a large ringing noise at the PH node and the BOOT node occurs. This noise is caused by high dv/dt phase node switching, parasitic PH node capacitance due to PCB routing, and the parasitic inductance. To reduce this noise, a resistor can be added between the BOOT pin and the bootstrap capacitor. A large resistor value reduces the ringing noise at PH node, but limits the charging of the bootstrap capacitor during the low-side MOSFET on-time, especially when the controller is operating at very low duty cycle. Also, large resistance causes a voltage dip at BOOT each time the high-side driver turns on the high-side MOSFET. Make sure this voltage dip does not trigger the high-side BOOT to PH UVLO threshold 3V (typical), especially when a MOSFET with large Q_g is used.

Loop Compensation Design

The ISL78227 uses constant frequency peak current mode control architecture with a Gm amp as the error amplifier. Figures 64 and 65 on page 39 show the conceptual schematics and control block diagram, respectively.

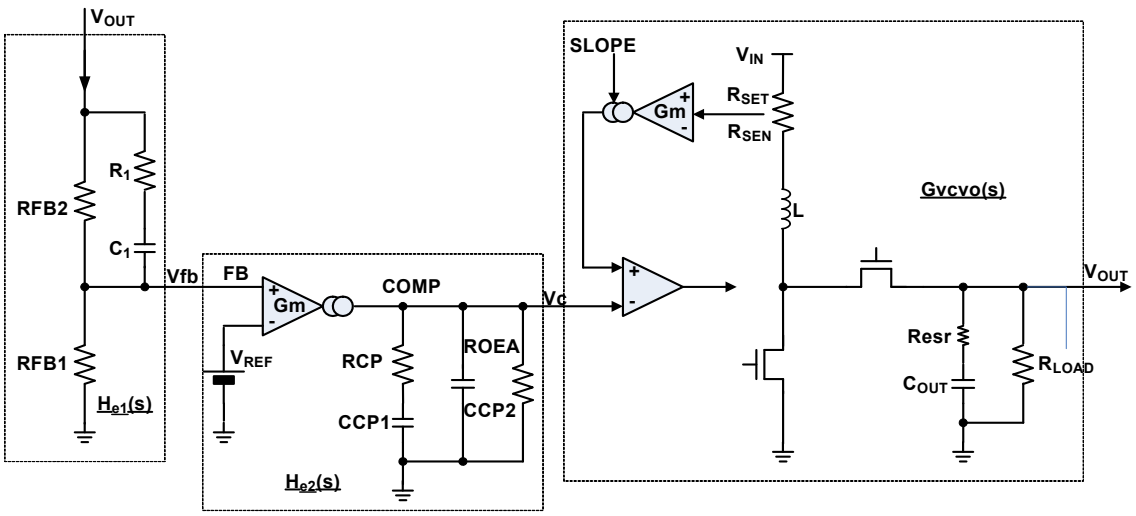


FIGURE 64. CONCEPTUAL BLOCK DIAGRAM OF PEAK CURRENT MODE CONTROLLED BOOST REGULATOR

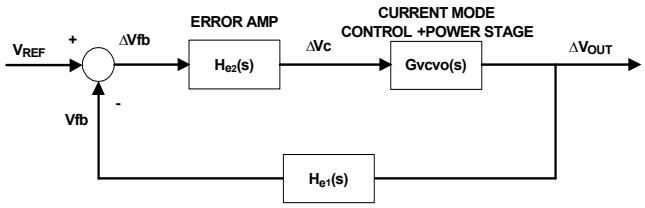


FIGURE 65. CONCEPTUAL CONTROL BLOCK DIAGRAM

TRANSFER FUNCTION FROM V_C TO V_{OUT}

Transfer function from error amplifier output V_C to output voltage V_{OUT} $G_{vcvo}(s)$ can be expressed as Equation 33.

$$G_{vcvo}(s) = K_{DC} \cdot \frac{\left(1+\frac{s}{\omega_{esr}}\right)\cdot\left(1-\frac{s}{\omega_{RHZ}}\right)}{\left(1+\frac{s}{\omega_p PS}\right)\cdot\left(1+\frac{s}{Q_p\cdot\omega_n}+\left(\frac{s}{\omega_n}\right)^2\right)} \quad \text{(EQ. 33)}$$

The expressions of the poles and zeros are listed below:

$$K_{DC} = \frac{R_{LOAD}\cdot(1-D)}{2\cdot K_{ISEN}}$$

$$\omega_{RHZ} = \frac{R_{LOAD}\cdot(1-D)^2}{L_{eq}}$$

$$\omega_{esr} = \frac{1}{C_{OUT}\cdot R_{esr}}$$

$$\omega_{pPS} = \frac{2}{C_{OUT}\cdot R_{LOAD}}$$

$$Q_p = \frac{1}{\pi\cdot\left[(1-D)\cdot\frac{S_e}{S_n}+0.5-D\right]}$$

$$\omega_n = \pi\cdot f_{SW}$$

where:

- N is the number of phases, R_{ESR} is the output capacitor's Equivalent Series Resistance (ESR) of the total capacitors, R_{LOAD} is the load resistance, L_{eq} is the equivalent inductance for multiphase boost with N number of phases, and L is each phase's inductor's inductance.

$$L_{eq} = \frac{L}{N}$$

- K_{ISEN} is the current sense gain as shown in Equation 34, where R_{SENx} and R_{SETx} are per-phase current sense resistors and setting resistors described in "Current Sense for Individual Phase - I_{SENX}" on page 31.

$$K_{ISEN} = \frac{R_{SENx}\cdot 6500}{N\cdot R_{SETx}} \quad \text{(EQ. 34)}$$

- Se/Sn is the gain of the selected compensating slope over the sensed inductor current up-ramp. It can be calculated in Equation 35, where K_{SLOPE} is the gain of selected compensating slope over the sensed IL down slope (refer to Equation 15 on page 32).

$$\frac{S_e}{S_n} = K_{SLOPE}\cdot\left(\frac{V_{OUT}}{V_{IN}}-1\right) \quad \text{(EQ. 35)}$$

Equation 33 shows that the system is mainly a single order system plus a Right Half Zero (RHZ), which commonly exists for boost converters. The main pole ω_{pPS} is determined by load and output capacitance and the ESR zero ω_{ESR} is the same as the buck converter.

Because the ω_{RHZ} changes with load, typically the boost converter crossover frequency is set 1/5 to 1/3 of the ω_{RHZ} frequency.

The double pole ω_n is at half of the f_{SW} and has minimum effects at crossover frequency for most of the cases when the crossover frequency is fairly low.

COMPENSATOR DESIGN

Generally, a simple Type-2 compensator can be used to stabilize the system. In the actual application, however, an extra phase margin is provided by a Type-3 compensator.

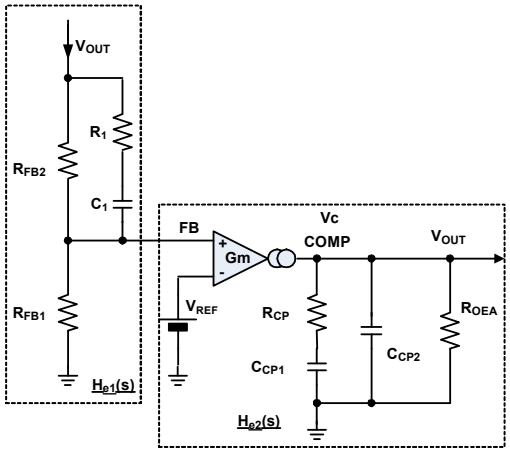


FIGURE 66. TYPE-3 COMPENSATOR

The transfer function at the error amplifier and its compensation network can be expressed as Equation 36.

$$e2(s) = \frac{V_C}{V_{FB}} = g_m \cdot Z_{COMP} = \frac{g_m (1 + sR_{CP}C_{CP1})R_{OEA}}{1 + s[R_{CP}C_{CP1} + R_{OEA}(C_{CP1} + C_{CP2})] + C_{CP2}C_{CP1}R_{CP}R_{OEA}s^2} \quad \text{(EQ. 36)}$$

If $R_{OEA} >> R_{CP}$, $C_{CP1} >> C_{CP2}$, and R_{OEA} = infinite, the equation can be simplified as shown in Equation 37:

$$H_{e2}(s) = g_m \cdot \frac{1 + s \cdot R_{CP} \cdot C_{CP1}}{s \cdot C_{CP1} \cdot (1 + s \cdot R_{CP} \cdot C_{CP2})} = \frac{\omega_1}{s} \cdot \frac{1 + \frac{s}{\omega_{z2}}}{1 + \frac{s}{\omega_{p2}}} \quad \text{(EQ. 37)}$$

where:

$$\omega_{p2} = \frac{g_m}{C_{CP1}}$$

$$\omega_{z2} = \frac{1}{R_{CP} \cdot C_{CP1}}$$

$$\omega_{p3} = \frac{1}{R_{CP} \cdot C_{CP2}}$$

If Type-3 compensation is needed, the transfer function at the feedback resistor network is:

$$H_{e1}(s) = \frac{R_{FB1}}{R_{FB1} + R_{FB2}} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}} \quad \text{(EQ. 38)}$$

where:

$$\omega_{z1} = \frac{1}{C_1 \cdot (R_{FB2} + R_1)}$$

$$\omega_{p1} = \frac{1}{C_1 \cdot \frac{R_{FB2} \cdot R_{FB1} + R_{FB2} \cdot R_1 + R_{FB1} \cdot R_1}{R_{FB2} + R_{FB1}}}$$

The total transfer function with compensation network and gain stage is expressed as:

$$G_{open}(s) = G_{vcvo}(s) \cdot H_{e1}(s) \cdot H_{e2}(s) \quad \text{(EQ. 39)}$$

Use f = ω/2π to convert the pole and zero expressions to frequency domain, and from Equations 33, 38, and 39, select the compensator's pole and zero locations.

In general, as described earlier, a Type-2 compensation is enough. Typically, the crossover frequency is set 1/5 to 1/3 of the ω_{RHZ} frequency. As a general rule, set the compensator $\omega_{p2}/2\pi$ at the very low end frequency; set $\omega_{z2}/2\pi$ at 1/5 of the crossover frequency, and set $\omega_{p3}/2\pi$ at the ESR zero or the RHZ frequency $\omega_{RHZ}/2\pi$, whichever is lower.

V_{CC} Input Filter

To provide a quiet power rail to the internal analog circuitry, it is recommended to place an RC filter between PVCC and VCC. A 10Ω resistor between PVCC and VCC and at least 1µF ceramic capacitor from VCC to GND are recommended.

Current Sense Circuit

To set the current sense resistor, the voltage across the current sense resistor should be limited to within ±0.3V. In a typical application, it is recommended to set the voltage across the current sense resistor in range around 30mV to 100mV for the typical load current condition.

Configuration to Support Single Phase Boost

The IC can be configured to support single phase operation either using Phase 1 or Phase 2. The configurations needed to use Phase 1 for single phase operation are listed below (to use Phase 2 for single phase operation, change the corresponding phase number to the other phase number):

- BOOT2 = GND (UG2 disabled)
- ISEN2P = ISEN2N = GND
- PH2 = GND

The extra notes are listed below with upper single phase configurations:

- LG2 can be left floating. LG2 has PWM signals which are fine with no external MOSFET to drive.
- IMON pin output current signal has only Phase 1's inductor current sensed signal. Equation 12, which calculates the IMON output current, is expressed as Equation 40.

$$IMON = \frac{I_{L1} \cdot R_{SEN1}}{R_{SET1}} \cdot 0.125 + 17 \cdot 10^{-6} \quad \text{(EQ. 40)}$$

The Constant Current Loop works on the same principle.

Layout Considerations

For DC/DC converter design, the PCB layout is very important to ensure the desired performance.

1. Place input ceramic capacitors as close as possible to the IC's VIN and PGND/SGND pins.
2. Place the output ceramic capacitors as close as possible to the power MOSFETs. Keep this loop (output ceramic capacitor and MOSFETs for each phase) as small as possible to reduce voltage spikes induced by the trace parasitic inductances when MOSFETs switching ON and OFF.
3. Place the output aluminum capacitors close to the power MOSFETs.
4. Keep the phase node copper area small, but large enough to handle the load current.
5. Place the input aluminum and some ceramic capacitors close to the input inductors and power MOSFETs.
6. Place multiple vias under the bottom pad of the IC. Connect the bottom pad to the ground copper plane with as large an area as possible in multiple layers to effectively reduce the thermal impedance. Figure 67 shows the layout example for vias in the IC bottom pad.

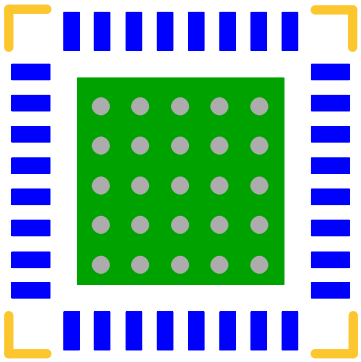


FIGURE 67. RECOMMENDED LAYOUT PATTERN FOR VIAS IN THE IC BOTTOM PAD

7. Place the 10µF decoupling ceramic capacitor at the PVCC pin and as close as possible to the IC. Put multiple vias close to the ground pad of this capacitor.
8. Place the 1µF decoupling ceramic capacitor at the VCC pin and as close as possible to the IC. Put multiple vias close to the ground pad of this capacitor.
9. Keep the bootstrap capacitors as close as possible to the IC.
10. Keep the driver traces as short as possible and with relatively large width (25 mil to 40 mil is recommended), and avoid using via or minimal number of vias in the driver path to achieve the lowest impedance.
11. Place the current sense setting resistors and the filter capacitors (shown as R_{SETxB}, R_{BIASxB}, and C_{ISENx} in Figure 60 on page 31) as close as possible to the IC. Keep each pair of the traces close to each other to avoid undesired switching noise injections.
12. The current-sensing traces must be laid out very carefully because they carry tiny signals with only tens of mV. For the current-sensing traces close to the power sense resistor (R_{SENx}), the layout pattern shown in Figure 68 is recommended. Assuming the R_{SENx} is placed in the top layer (red), route one current sense connection from the middle of one R_{SENx} pad in the top layer under the resistor (red trace). For the other current-sensing trace, from the middle of the other pad on R_{SENx} in the top layer, after a short distance, via down to the second layer and route this trace right under the top layer current sense trace.
13. Keep the current-sensing traces far from the noisy traces such as gate driving traces (LGx, UGx, and PHx), phase nodes in power stage, BOOTx signals, output switching pulse currents, driving bias traces, and input inductor ripple current signals, etc.

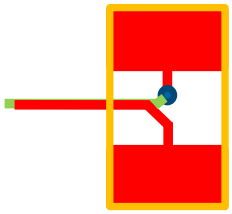


FIGURE 68. RECOMMENDED LAYOUT PATTERN FOR CURRENT SENSE TRACES REGULATOR

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Jul 13, 2018	FN8808.5	Updated the ordering information table by adding tape and reel column, adding tape and reel parts to table, and updating Note 1. Added two lines to the “Absolute Maximum Ratings” on page 9. Changed “If the DE/PHDRP pin = GND” to “If the DE/PHDRP pin = VCC” in “Operation Initialization and Soft-Start” on page 29. Removed the About Intersil section.
Sep 18, 2017	FN8808.4	Fixed Equation 7 on page 30. Applied new header/footer.
Feb 6, 2017	FN8808.3	-Added Related Literature on page 1. -Added third sentence in the VIN pin description on page 5. -Figures 26 and 28 on page 19, changed "D" to "D_TRACK" in the title to avoid confusion. -Figure 44 on page 22, swapped VPORL_PVCC and VPORL_VCC data labels for the 2 curves. -Added “while the adaptive dead time control is still functioning at the same time” to the first sentence in “Programmable Adaptive Dead Time Control” on page 24. -Added “for three consecutive switching cycles” to the first sentence in “Peak Overcurrent Fault (OC2_PEAK) Protection” on page 35. -Added the last paragraph in “Average Overcurrent Fault (OC_AVG) Protection” on page 36. -Updated Figures 64, 65, and 66. -Updated Equation 33 on page 39, and expressions K_{DC}, wpPS, Q_p, and w_n. -Updated Equation 34 on page 39. -Added section “Configuration to Support Single Phase Boost” on page 40.
Feb 24, 2016	FN8808.2	-Figure 16 on page 17: changed the label "IL1" to "IL2" and in figure title, changed "PHASE1" to "PHASE 2". -Updated POD L32.5x5H to most recent revision with change as follows: Detail "X" - Added dimple dimension 0.10 ±0.05 back on (left side). Detail "X" - Changed the tolerance back (in the seating plane box) to 0.08. Bottom View - Removed 0.15 ±0.10 this is a duplicate dim with detail A. Bottom View - Extended the dimension line to the bottom of the exposed pad
Dec 24, 2015	FN8808.1	Updated expression Qp and Equation 35 on page 39. Removed text after Equation 35 on page 39 and before paragraph that begins with “Equation 33”.
Nov 23, 2015	FN8808.0	Initial release

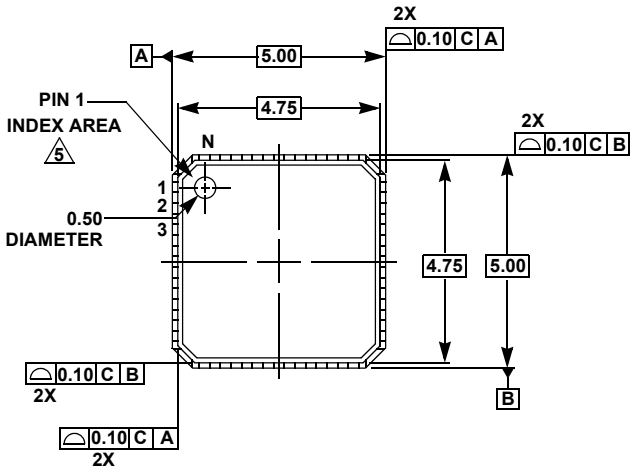
Package Outline Drawing

For the most recent package outline drawing, see L32.5x5H.

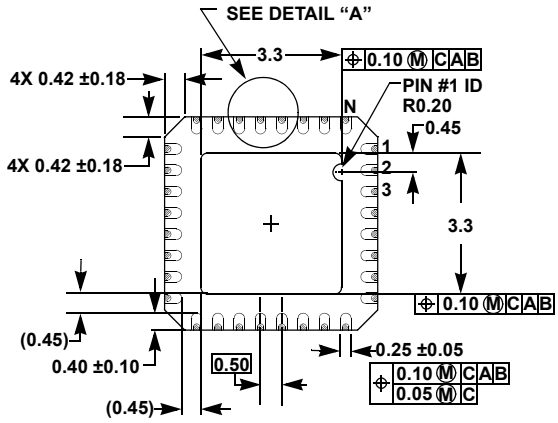
L32.5x5H

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN WITH WETABLE FLANK)

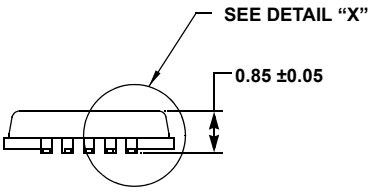
Rev 2, 1/16



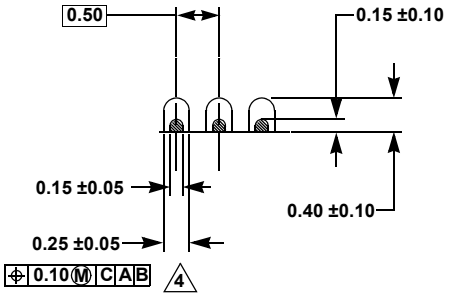
TOP VIEW



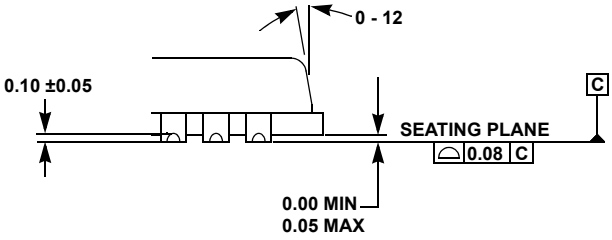
BOTTOM VIEW



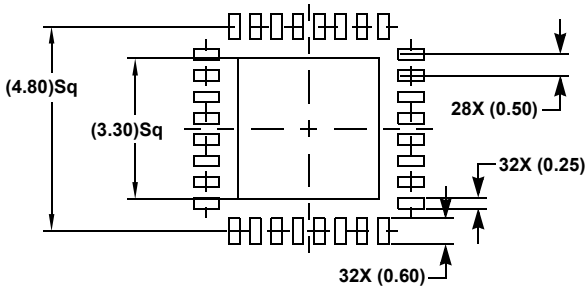
SIDE VIEW



DETAIL "A"



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASMEY 14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Reference document: JEDEC MO220

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