40V Low I_Q, 3MHz Dual, 2-Phase Synchronous Step-Down Controller with Spread Spectrum

FEATURES

- **Wide Input Voltage Range: 4.5V to 40V**
- **Wide Output Voltage Range: 0.8V to 99% • V_{IN}**
- **Low Operating I_Q: 12µA (14V to 3.3V, Channel 1 On)**
- **Fixed 3.3V Output Voltage on Channel 1**
- **Spread Spectrum Operation**
- **R_{SENSE} or DCR Current Sensing**
- Out-of-Phase Controllers Reduce Required Input Capacitance and Power Supply Induced Noise
- Programmable Fixed Frequency (100kHz to 3MHz)
- Phase-Lockable Frequency (100kHz to 3MHz)
- Selectable Continuous, Pulse-Skipping, or Low Ripple, Burst Mode® Operation at Light Loads
- Very Low Dropout Operation: 99% Duty Cycle
- Power Good Output Voltage Monitors
- Output Overvoltage Protection
- Internal LDO Powers Gate Drive from V_{IN} or $EXTV_{CC}$
- Low Shutdown I_Q: 1.5µA
- Side Wettable 4mm × 5mm QFN-28 Package

APPLICATIONS

- Automotive and Transportation
- Industrial
- Military / Avionics

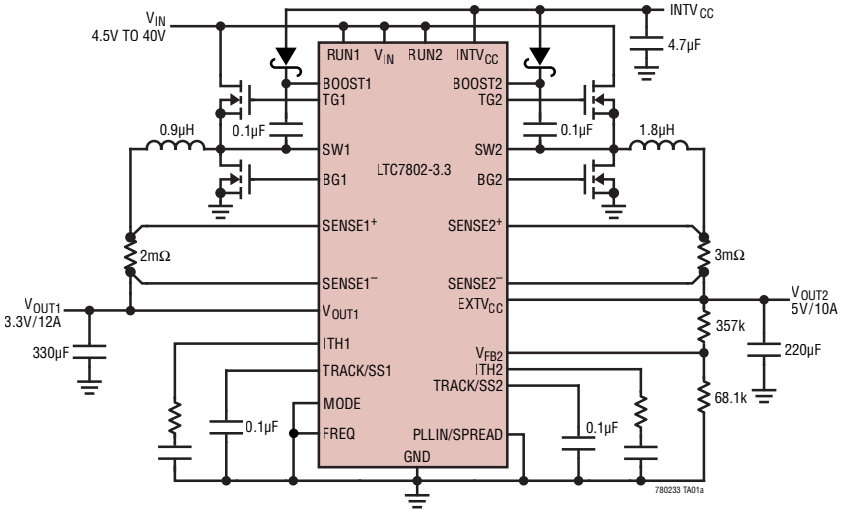
DESCRIPTION

The LTC®7802-3.3 is a high performance dual step-down synchronous DC/DC switching regulator controller that drives all N-channel power MOSFET stages. Constant frequency current mode architecture allows a phase-lockable switching frequency of up to 3MHz. The LTC7802-3.3 operates from a wide 4.5V to 40V input supply range. Power loss and supply noise are minimized by operating the two controller output stages out-of-phase.

The very low no-load quiescent current extends operating runtime in battery powered systems. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC7802-3.3 features a precision 0.8V reference and power good output indicators. The MODE pin selects among Burst Mode operation, pulse-skipping mode, or continuous inductor current mode at light loads.

The LTC7802-3.3 additionally features spread spectrum operation which significantly reduces the peak radiated and conducted noise on both the input and output supplies, making it easier to comply with electromagnetic interference (EMI) standards.

TYPICAL APPLICATION

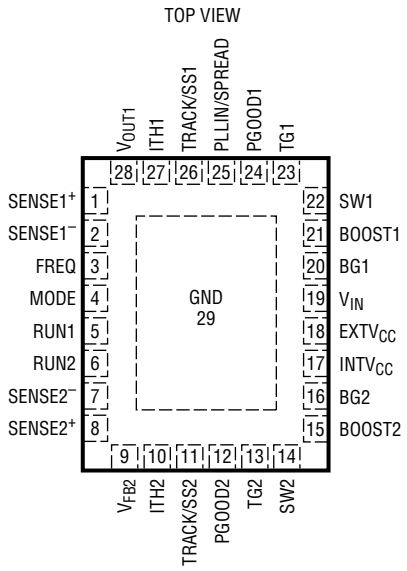


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 40V
BOOST1, BOOST2 ..... –0.3V to 46V
Switch Voltage (SW1, SW2) ..... –5V to 40V
RUN1, RUN2 Voltages ..... –0.3V to 40V
$EXTV_{CC}$ Voltage ..... –0.3V to 30V
$INTV_{CC}$ Voltage ..... –0.3V to 6V
(BOOST1–SW1), (BOOST2–SW2) ..... –0.3V to 6V
$SENSE1^+$, $SENSE1^-$ Voltages ..... –0.3V to 40V
$SENSE2^+$, $SENSE2^-$ Voltages ..... –0.3V to 40V
TRACK/SS1, V_{OUT1} Voltages ..... –0.3V to 6V
TRACK/SS2, V_{FB2} Voltages ..... –0.3V to 6V
MODE, PGOOD1, PGOOD2 Voltages ..... –0.3V to 6V
PLLIN/SPREAD, FREQ Voltages ..... –0.3V to 6V
ITH1, ITH2 Voltages ..... –0.3V to 2V
BG1, BG2, TG1, TG2 ..... (Note 9)
Operating Junction Temperature Range (Notes 2, 8)
LTC7802E-3.3, LTC7802I-3.3 ..... –40°C to 125°C
LTC7802J-3.3, LTC7802H-3.3 ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFDM PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7802EUFDM-3.3#PBF	LTC7802-3.3EUFDM#TRPBF	78023	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC7802IUFDM-3.3#WPBF	LTC7802IUFDM-3.3#WTRPBF	78023	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7802JUFDM-3.3#WPBF	LTC7802JUFDM-3.3#WTRPBF	78023	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C
LTC7802HUFDM-3.3#WPBF	LTC7802HUFDM-3.3#WTRPBF	78023	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, RUN1,2 > 1.25V, $EXTV_{CC}$ = 0V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply (V_{IN})							
V_{IN}	Input Supply Operating Range			4.5		40	V
I_{VIN}	V_{IN} Current in Regulation	Front Page Circuit, 14V to 3.3V, No Load, RUN2 = 0V			12		µA
Controller Operation							
V_{OUT2}	Channel 2 Output Voltage Operating Range			0.8		40	V
V_{OUT1}	Channel 1 Regulated Output Voltage	(Note 4) V_{IN} = 4.5V to 40V, ITH1 Voltage = 0.6V to 1.2V	●	3.25	3.3	3.35	V
V_{FB2}	Channel 2 Regulated Feedback Voltage	(Note 4) V_{IN} = 4.5V to 40V, ITH2 Voltage = 0.6V to 1.2V	●	0.788	0.800	0.812	V
	Feedback Current	Channel 1 Channel 2			1 ±5	 ±50	µA nA
	Feedback Overvoltage Protection Threshold	Measured at V_{OUT1}, V_{FB2} Relative to Regulated V_{OUT1}, V_{FB2}		7	10	13	%
$g_{m1,2}$	Transconductance Amplifier g_m	(Note 4) ITH1,2 = 1.2V, Sink/Source = 5µA			1.8		mmho
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{OUT1} = 2.9V, V_{FB2} = 0.7V, $V_{SENSE1,2^-}$ = 3.3V	●	45	50	55	mV
	Matching Between Channels	$V_{SENSE1,2^-}$ = 3.3V		–3.5	0	3.5	mV
$I_{SENSE1,2^+}$	SENSE1, 2^+ Pin Current	$V_{SENSE1,2^+}$ = 3.3V				±1	µA
I_{SENSE1^-}	$SENSE1^-$ Pin Current	V_{SENSE1^-} = 3.3V			50		µA
I_{SENSE2^-}	$SENSE2^-$ Pin Current	V_{SENSE2^-} = 3.3V V_{SENSE2^-} > $INTV_{CC}$ + 0.5V			 650	±2	µA µA
	Soft-Start Charge Current	$V_{TRACK/SS1,2}$ = 0V		10	12.5	15	µA
	RUN Pin ON Threshold	$V_{RUN1,2}$ Rising	●	1.15	1.20	1.25	V
	RUN Pin Hysteresis				100		mV
DC Supply Current (Note 5)							
	V_{IN} Shutdown Current	RUN1,2 = 0V			1.5		µA
	V_{IN} Sleep Mode Current Only Channel 2 On	V_{SENSE1^-} < 3.2V, $EXTV_{CC}$ = 0V			15	24	µA
	Sleep Mode Current (Note 3) Only Channel 1 On	V_{IN} Current, $EXTV_{CC}$ = 0V V_{IN} Current, $EXTV_{CC}$ ≥ 4.8V $EXTV_{CC}$ Current, $EXTV_{CC}$ ≥ 4.8V $SENSE1^-$ Current			5 1 5 10	9 4 10 18	µA µA µA µA
	Sleep Mode Current (Note 3) Both Channels On	$EXTV_{CC}$ ≥ 4.8V V_{IN} Current $EXTV_{CC}$ Current $SENSE1^-$ Current			 1 7 12	 4 14 22	 µA µA µA
	Pulse-Skipping or Forced Continuous Mode V_{IN} or $EXTV_{CC}$ Current (Notes 3, 5)	One Channel On Both Channels On			2 3		mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, RUN1,2 > 1.25V, $EXTV_{CC}$ = 0V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers							
	TG or BG On-Resistance	Pull-Up Pull-Down			2.0 1.0		Ω Ω
	TG or BG Transition Time Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 15		 ns ns
	TG Off to BG On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			15		ns
	BG Off to TG On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			15		ns
$t_{ON(MIN)1,2}$	TG Minimum On-Time	(Note 7)			40		ns
	Maximum Duty Factor for TG	f_{OSC} = 350kHz		98	99		%
$INTV_{CC}$ Low Dropout (LDO) Linear Regulator							
	$INTV_{CC}$ Regulation Point			4.9	5.1	5.3	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 100mA, V_{IN} ≥ 6V I_{CC} = 0mA to 100mA, V_{EXTVCC} ≥ 6V			1.2 1.2	2 2	% %
	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Rising		4.5	4.7	4.8	V
	$EXTV_{CC}$ Switchover Hysteresis				250		mV
UVLO	Undervoltage Lockout	$INTV_{CC}$ Rising $INTV_{CC}$ Falling	● ●	4.10 3.75	4.20 3.85	4.35 4.00	V V
Spread Spectrum Oscillator and Phase-Locked Loop							
f_{OSC}	Low Fixed Frequency	V_{FREQ} = 0V, PLLIN/SPREAD = 0V		320	350	380	kHz
	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$, PLLIN/SPREAD = 0V	●	2.0	2.25	2.5	MHz
	Programmable Frequency	R_{FREQ} = 374kΩ, PLLIN/SPREAD = 0V R_{FREQ} = 75kΩ, PLLIN/SPREAD = 0V R_{FREQ} = 12.1kΩ, PLLIN/SPREAD = 0V		 450	100 500 3	 550	kHz kHz MHz
	Synchronizable Frequency Range	PLLIN/SPREAD = External Clock	●	0.1		3	MHz
	PLLIN Input High Level PLLIN Input Low Level		● ●	2.2		 0.5	V V
	Spread Spectrum Frequency Range (Relative to f_{OSC})	PLLIN/SPREAD = $INTV_{CC}$ Minimum Frequency Maximum Frequency			 –12 15		 % %
PGOOD1 and PGOOD2 Outputs							
	PGOOD Voltage Low	$I_{PGOOD1,2}$ = 2mA			0.2	0.4	V
	PGOOD Leakage Current	$V_{PGOOD1,2}$ = 5V				±1	µA
	PGOOD Trip Level V_{OUT1}, V_{FB2} Relative to Set Regulation Point	V_{OUT1}, V_{FB2} Rising Hysteresis		7	10 2.5	13	% %
		V_{OUT1}, V_{FB2} Falling Hysteresis		–13	–10 2.5	–7	% %
	PGOOD Delay for Reporting a Fault				25		µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7802-3.3 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7802E-3.3 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7802I-3.3 is guaranteed over the –40°C to 125°C operating junction temperature range, and the LTC7802J-3.30/LTC7802H-3.3 are guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: When $SENSE1^- \geq 3.2V$ or $EXTV_{CC} \geq 4.8V$, V_{IN} supply current is transferred to these pins to reduce the total input supply quiescent current. $SENSE1^-$ bias current is reflected to the channel 1 input supply by the formula $I_{VIN1} = I_{SENSE1-} \bullet V_{OUT1}/(V_{IN1} \bullet \eta)$, where η is the efficiency. $EXTV_{CC}$ bias current is similarly reflected to the input supply when biased by an output. Input supply current is minimized when $EXTV_{CC}$ is connected to the lowest output-derived voltage greater than 4.8V.

Note 4: The LTC7802-3.3 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant V_{OUT1}, V_{FB2}.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

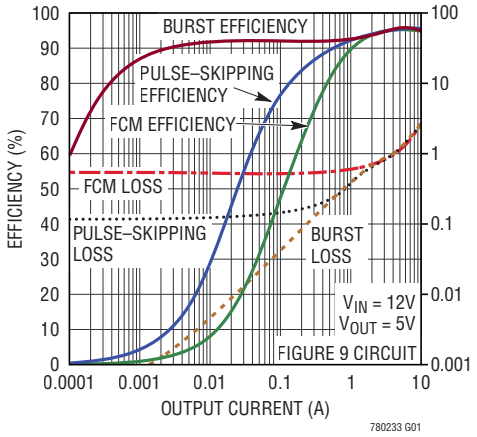
Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of $I_{L(MAX)}$ (See Minimum On-Time Considerations in the Applications Information section).

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

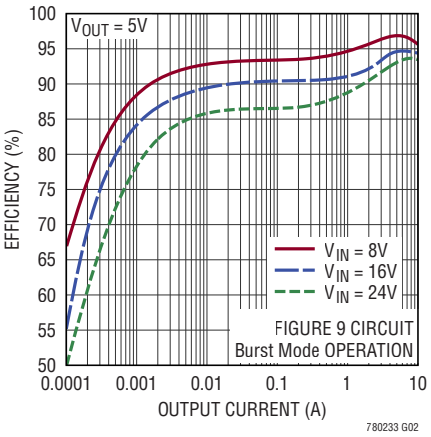
Note 9: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

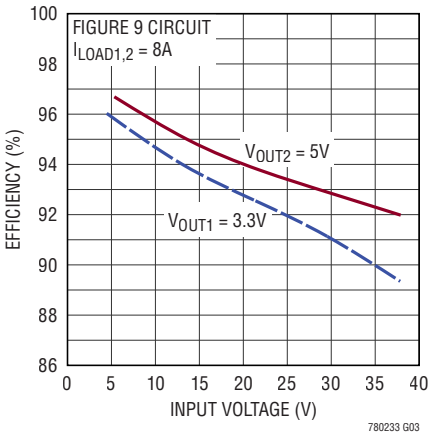
Efficiency and Power Loss vs Load Current



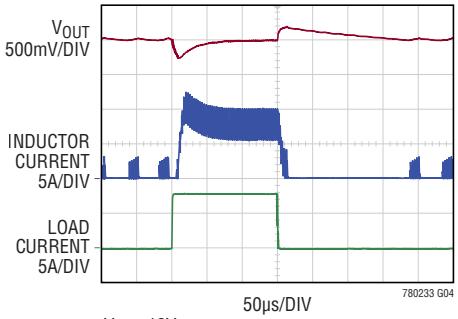
Efficiency vs Load Current



Efficiency vs Input Voltage

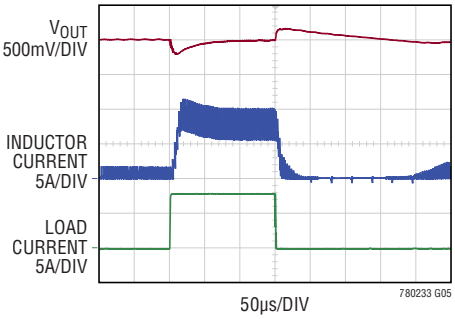


Load Step Burst Mode Operation



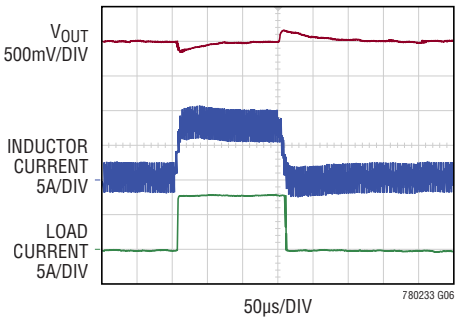
VIN = 12V
VOUT = 5V
300mA TO 8A LOAD STEP
FIGURE 9 CIRCUIT

Load Step Pulse-Skipping Mode



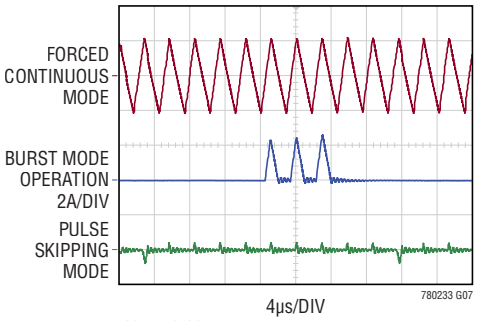
VIN = 12V
VOUT = 5V
300mA TO 8A LOAD STEP
FIGURE 9 CIRCUIT

Load Step Forced Continuous Mode



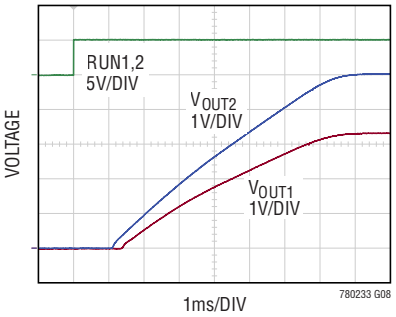
VIN = 12V
VOUT = 5V
300mA TO 8A LOAD STEP
FIGURE 9 CIRCUIT

Inductor Current at Light Load



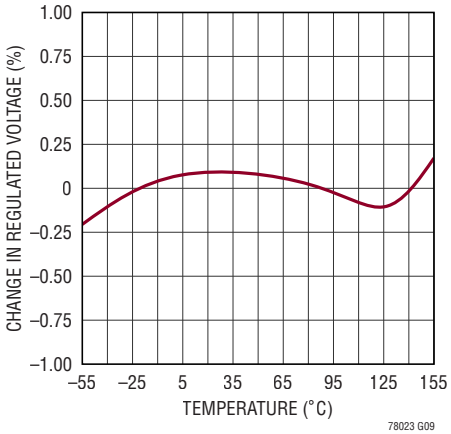
VIN = 12V
VOUT = 5V
NO LOAD
FIGURE 9 CIRCUIT

Soft Start-Up



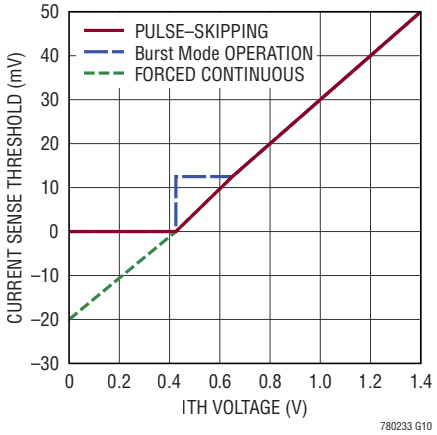
VIN = 12V
FORCED CONTINUOUS MODE
FIGURE 9 CIRCUIT

Regulated Feedback Voltage vs Temperature

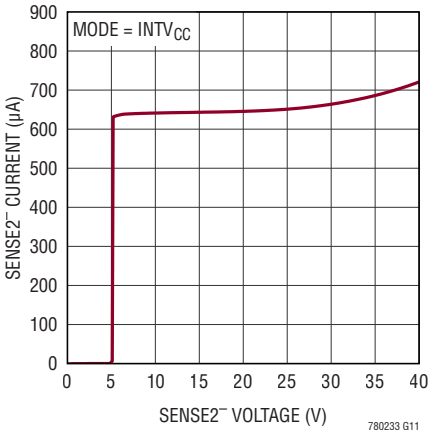


TYPICAL PERFORMANCE CHARACTERISTICS

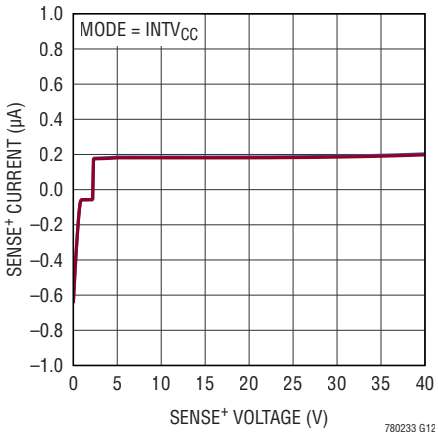
Current Sense Threshold vs ITH Voltage



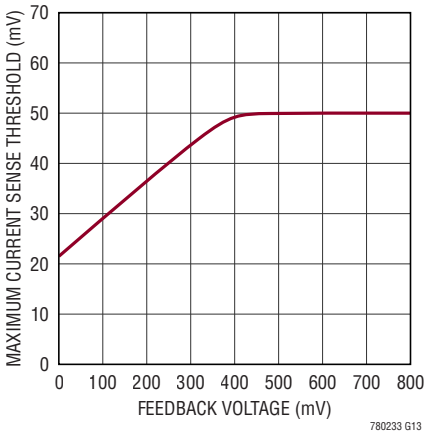
SENSE1,2⁻ Input Current vs V_{SENSE} Voltage



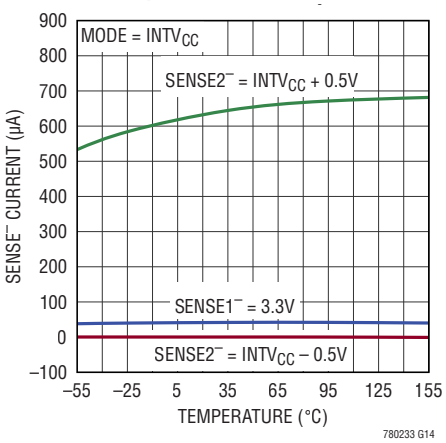
SENSE1,2⁺ Input Current vs V_{SENSE} Voltage



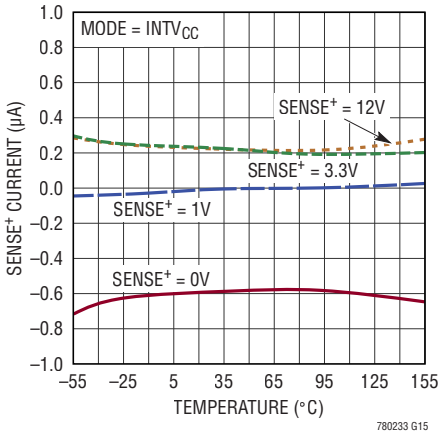
Foldback Current Limit



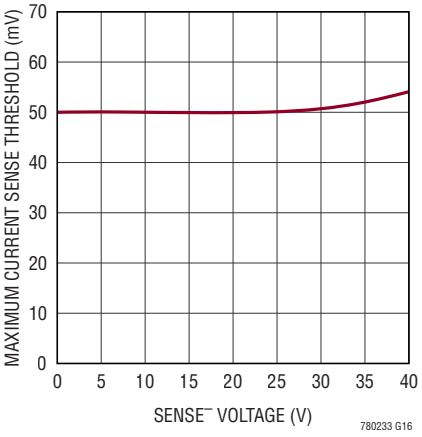
SENSE1,2⁻ Input Current vs Temperature



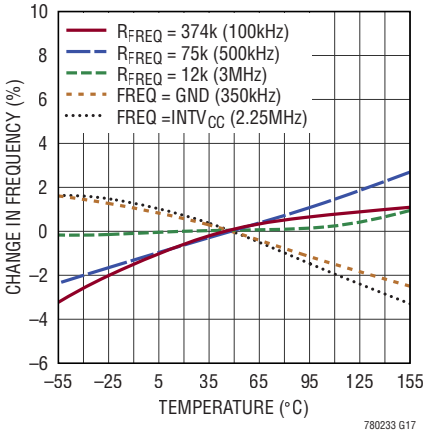
SENSE1,2⁺ Input Current vs Temperature



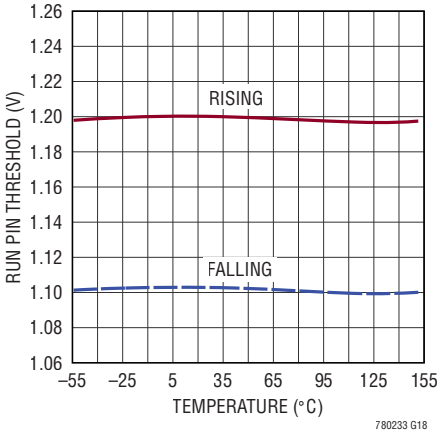
Maximum Current Sense Threshold vs SENSE⁻ Voltage



Oscillator Frequency vs Temperature

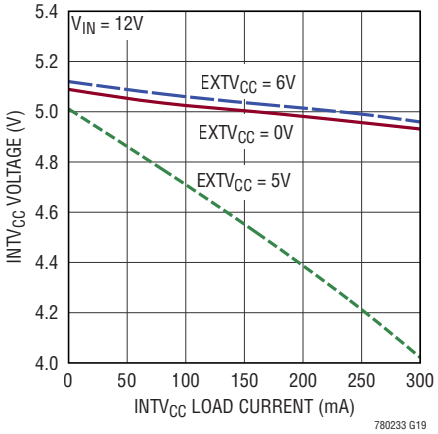


RUN Pin Thresholds vs Temperature

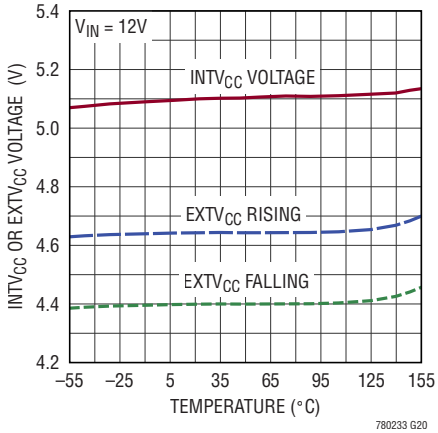


TYPICAL PERFORMANCE CHARACTERISTICS

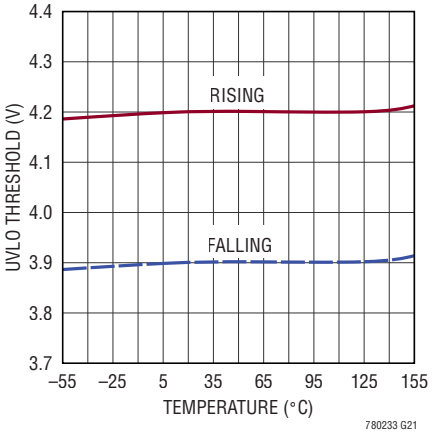
$INTV_{CC}$ Load Regulation



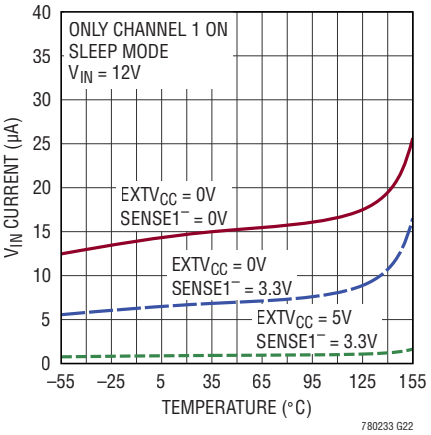
$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltage vs Temperature



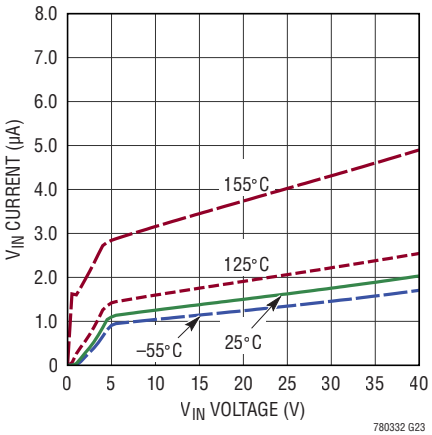
$INTV_{CC}$ Undervoltage Lockout Thresholds vs Temperature



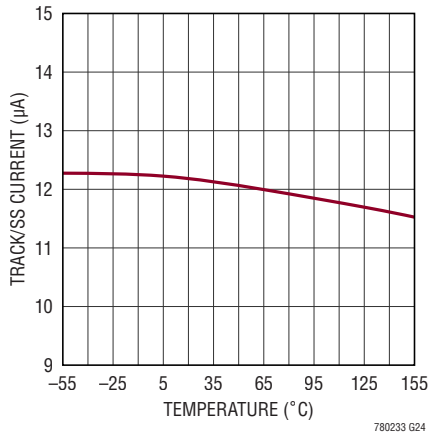
Quiescent Current vs Temperature



Shutdown Current vs V_{IN} Voltage



TRACK/SS Pull-Up Current vs Temperature



PIN FUNCTIONS

SENSE1$^+$, SENSE2$^+$ (Pins 1,8): The Positive (+) Input to the Differential Current Comparators. The ITH pin voltage and controlled offsets between the SENSE$^-$ and SENSE$^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

SENSE1$^-$, SENSE2$^-$ (Pins 2,7): The Negative (–) Input to the Differential Current Comparators. The SENSE2$^-$ pin supplies current to its current comparator when it is greater than $INTV_{CC}$. When SENSE1$^-$ is 3.2V or greater, it supplies the majority of the sleep mode quiescent current instead of V_{IN}, further reducing the input-referred quiescent current.

FREQ (Pin 3): Frequency Control Pin for the Internal Oscillator. Connect to ground to set the switching frequency to 350kHz. Connect to $INTV_{CC}$ to set the switching frequency to 2.25MHz. Frequencies between 100kHz and 3MHz can be programmed using a resistor between the FREQ pin and ground. Minimize the capacitance on this pin.

MODE (Pin 4): Mode Select Input. This input, which acts on both channels, determines how the LTC7802-3.3 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floating. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to $INTV_{CC}$ through a 100k resistor selects pulse-skipping operation.

RUN1, RUN2 (Pins 5,6): Run Control Inputs for Each Controller. Forcing either of these pins below 1.1V disables switching of the corresponding controller. Forcing both of these pins below 0.7V shuts down the entire LTC7802-3.3, reducing quiescent current to approximately 1.5µA. These pins can be tied to V_{IN} for always-on operation. Do not float the RUN pins.

$INTV_{CC}$ (Pin 17): Output of the Internal 5.1V Low Dropout Regulator. The driver and control circuits are powered by this supply. Must be decoupled to ground with a minimum of 4.7µF ceramic or tantalum capacitor.

$EXTV_{CC}$ (Pin 18): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.7V. See $INTV_{CC}$ Regulators in the Applications Information section. Do not exceed 30V on this pin. Connect this pin to ground if the $EXTV_{CC}$ LDO is not used.

V_{IN} (Pin 19): Main Bias Input Supply Pin. A bypass capacitor should be tied between this pin and GND.

PLLIN/SPREAD (Pin 25): External Synchronization Input and Spread Spectrum Selection. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 signal to be synchronized with the rising edge of the external clock. When an external clock is present, the regulators operate in pulse-skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator or to ground to disable spread spectrum.

BG1, BG2 (Pins 20,16): High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

BOOST1, BOOST2 (Pins 21,15): Bootstrapped Supplies to the Top Side Floating Drivers. Connect capacitors between the corresponding BOOST and SW pins for each channel. Also connect Schottky diodes between the BOOST1 and $INTV_{CC}$ pins and the BOOST2 and $INTV_{CC}$ pins. Voltage swing at the BOOST pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

SW1, SW2 (Pins 22,14): Switch Node Connections to Inductors.

TG1, TG2 (Pins 23,13): High Current Gate Drives for Top N Channel MOSFETs. These are the outputs of floating drivers with a voltage swing of $INTV_{CC}$ superimposed on the switch node voltage SW.

PGOOD1, PGOOD2 (Pins 24,12): Open-Drain Power Good Outputs. The V_{OUT1}, V_{FB2} pins are monitored to ensure that $V_{OUT1,2}$ are in regulation. When V_{OUT} is not

PIN FUNCTIONS

within ±10% of its regulation point, the corresponding PGOOD pin is pulled low.

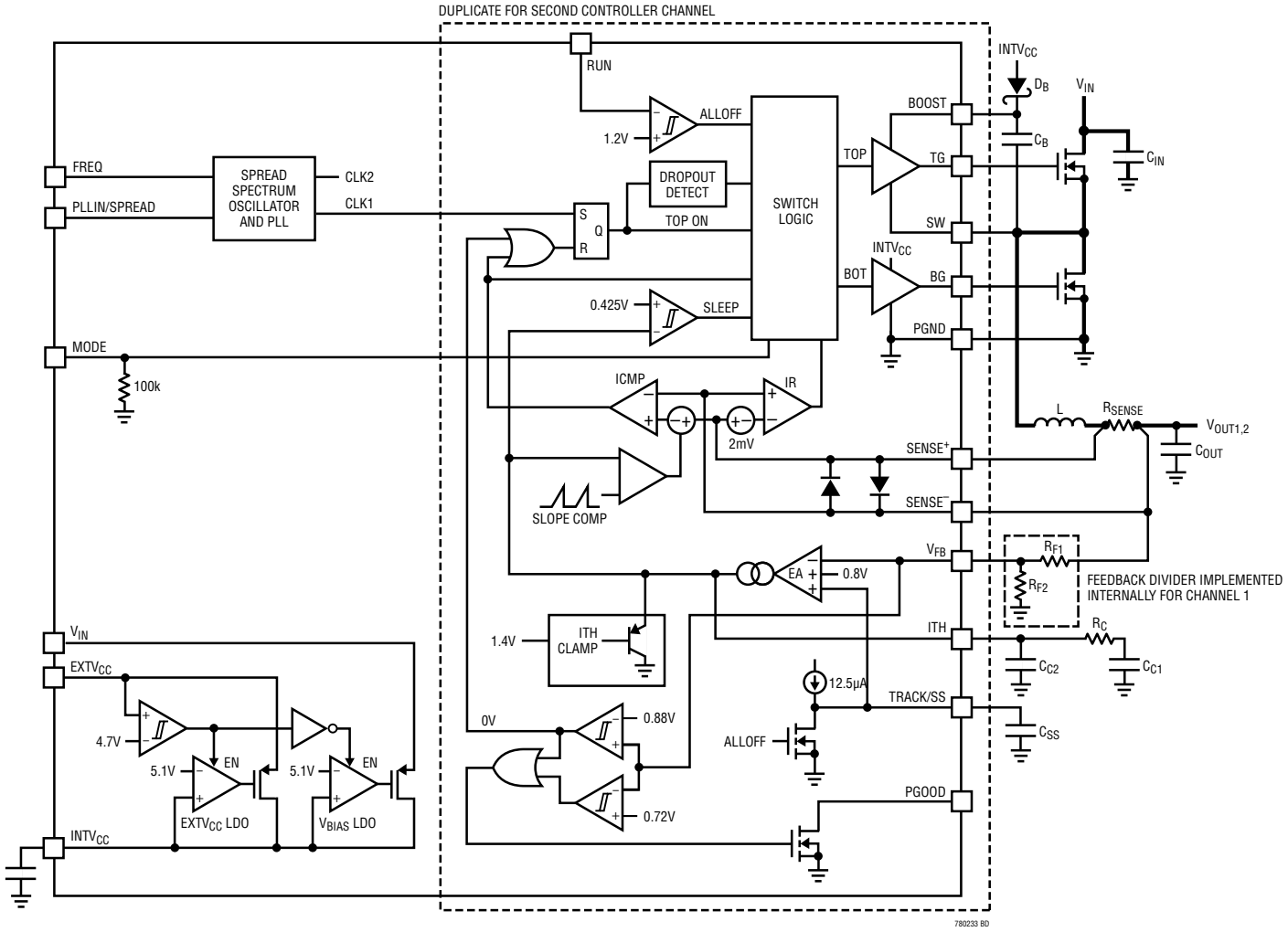
TRACK/SS1, TRACK/SS2 (Pins 26,11): External Tracking and Soft-Start Input. The LTC7802-3.3 regulates the negative input of the Error Amplifier (EA–) voltage to the lesser of 0.8V or the voltage on the TRACK/SS1,2 pin. Internal 12.5µA pull-up current sources are connected to these pins. A capacitor to ground sets the start-up ramp time to the final regulated output voltage. The ramp time is equal to 0.65ms for every 10nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to the TRACK/SS pins allows the LTC7802-3.3 output to track the other supply during start-up.

ITH1, ITH2 (Pins 27,10): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage. Place compensation components between the ITH pins and ground.

V_{OUT1}, V_{FB2} (Pins 28,9): Controller Feedback Inputs. Connect V_{OUT1} directly to the channel 1 output voltage. Connect an external resistor divider between the channel 2 output voltage and the V_{FB2} pin to set the regulated V_{OUT2} voltage. Tie V_{FB2} to $INTV_{CC}$ to configure the channels for a 2-phase 3.3V output, in which both channels share V_{OUT1}, ITH1, and TRACK/SS1.

GND (Exposed Pad Pin 29): Ground. Connects to the sources of the bottom N-Channel MOSFETs and the (–) terminal(s) of decoupling capacitors. The exposed pad must be soldered to PCB ground for rated electrical and thermal performance.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC7802-3.3 is a dual step-down (buck) synchronous controller utilizing a constant frequency, peak current mode architecture. The two controller channels operate 180° out of phase which reduces the required input capacitance and power supply induced noise. During normal operation, the external top MOSFET is turned on when the clock for that channel sets the SR latch, causing the inductor current to increase. The main switch is turned off when the main current comparator, ICMP, resets the SR latch. After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin, (which is generated with a resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.8V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference,which causes the EA to increase the I_{TH} voltage until the average inductor current matches the new load current.

Power and Bias Supplies (V_{IN}, $EXTV_{CC}$, and $INTV_{CC}$)

The $INTV_{CC}$ pin supplies power for the top and bottom MOSFET drivers and most of the internal circuitry. LDOs (low dropout linear regulators) are available from both the V_{IN} and $EXTV_{CC}$ pins to provide power to $INTV_{CC}$, which has a regulation point of 5.1V. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, the V_{IN} LDO supplies power to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.7V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC7802-3.3 switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each cycle through an external diode when the switch voltage goes low.

If the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for a short time every tenth cycle to allow C_B to recharge, resulting in a 99% duty cycle at 350kHz operation and approximately 98% duty cycle at 2MHz operation.

Start-Up and Shutdown (RUN and TRACK/SS Pins)

The two channels of the LTC7802-3.3 can be independently shut down using the RUN1 and RUN2 pins. Pulling a RUN pin below 1.1V shuts down the main control loop for that channel. Pulling both RUN pins below 0.7V disables both controllers and most internal circuits, including the $INTV_{CC}$ LDOs. In this shutdown state, the LTC7802-3.3 draws only 1.5µA of quiescent current.

The RUN pins may be externally pulled up or driven directly by logic. Each pin can tolerate up to 40V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where one or both controllers are enabled continuously and never shut down. Additionally, a resistive divider from V_{IN} to a RUN pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user adjustable level.

The start-up of each channel's output voltage V_{OUT} is controlled by the voltage on the corresponding TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference voltage, the LTC7802-3.3 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference voltage. This allows the TRACK/SS pin to be used as a soft-start which smoothly ramps the output voltage on start-up, thereby limiting the input supply inrush current. An external capacitor from the TRACK/SS pin to GND is charged by an internal 12.5µA pull-up current, creating a voltage ramp on the TRACK/SS pin. As

OPERATION

the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively, the TRACK/SS pins can be used to make the start-up of V_{OUT} track that of another supply. Typically this requires connecting to the TRACK/SS pin through an external resistor divider from the other supply to ground (see the Applications Information section).

Light Load Operation: Burst Mode Operation, Pulse-Skipping, or Forced Continuous Mode (MODE Pin)

The LTC7802-3.3 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at low load currents.

To select Burst Mode operation, tie the MODE pin to ground. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100k resistor to ground invokes Burst Mode operation when the MODE pin is floating and pulse-skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100k resistor.

When the controllers are enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of its maximum value even though the voltage on the ITH pin might indicate a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.45V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC7802-3.3 draws. If one channel is in sleep mode and the other channel is shut down, the LTC7802-3.3 draws only 15µA of quiescent current. If both channels are in sleep mode, the LTC7802-3.3 draws only 20µA of quiescent current. When V_{OUT} on channel 1 is 3.2V or higher, the majority of this quiescent current is supplied by the $SENSE1^-$ pin, which further reduces the input-referred quiescent current by the ratio of V_{IN}/V_{OUT} multiplied by the efficiency.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top MOSFET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7802-3.3 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode cannot be synchronized to an external clock.

OPERATION

Therefore, if Burst Mode is selected and the switching frequency is synchronized to an external clock applied to the PLLIN/SPREAD pin, the LTC7802-3.3 switches from Burst Mode to forced continuous mode.

Frequency Selection, Spread Spectrum, and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The free running switching frequency of the LTC7802-3.3 controllers is selected using the FREQ pin. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100kHz and 3MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7802-3.3 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within typical boundaries of –12% to +15% of the frequency set by the FREQ pin.

A phase-locked loop (PLL) is available on the LTC7802-3.3 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The LTC7802-3.3's PLL aligns the turn-on of controller 1's external top MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external top MOSFET is 180° out-of-phase to the rising edge of the external clock source.

The PLL frequency is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes in order to synchronize the rising edge of the external clock to the rising edge of TG1. For more rapid lock-in to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The LTC7802-3.3's PLL is guaranteed to lock to an external clock source whose frequency is between 100kHz and 3MHz.

The PLLIN/SPREAD pin is TTL compatible with thresholds of 1.6V (rising) and 1.1V (falling) and is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

Output Overvoltage Protection

Each channel has an overvoltage comparator that guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{OUT1}, V_{FB2} pin rises more than 10% above its regulation point, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Foldback Current

When the output voltage falls to less than 50% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS1,2 voltage).

Power Good

Each channel has a PGOOD pin that is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} voltage is not within ±10% of the 0.8V reference. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the V_{FB} voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V, such as $INTV_{CC}$.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7802-3.3 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors, and power MOSFETs can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for soft-start, biasing, and loop compensation.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered. The inductor value has a direct effect on ripple current.

The maximum average inductor current $I_{L(MAX)}$ is equal to the maximum output current. The peak current is equal to the average inductor current plus half of the inductor ripple current, ΔI_L, which decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{L(MAX)}$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Current Sense Selection

The LTC7802-3.3 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing has become popular because it saves expensive current sensing resistors and is more power efficient, particularly in higher current and lower frequency applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value.

The $SENSE^+$ and $SENSE^-$ pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 40V (absolute maximum), enabling the LTC7802-3.3 to regulate output voltages up to a maximum of 40V. The $SENSE^+$ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparators to be used in inductor DCR sensing. The

APPLICATIONS INFORMATION

impedance of the SENSE⁻ pin changes depending on the common mode voltage. When less than $INTV_{CC}$ – 0.5V, these pins are relatively high impedance, drawing ≈ 1µA. When above $INTV_{CC}$ + 0.5V, a higher current (≈650µA) flows into each pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. Channel 1's SENSE1⁻ pin has an additional ≈ 50µA current when its voltage is above 3.2V to bias internal circuitry from V_{OUT1} instead of V_{IN}, thereby reducing the input-referred supply current.

Filter components mutual to the sense lines should be placed close to the LTC7802-3.3, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small signal nodes.

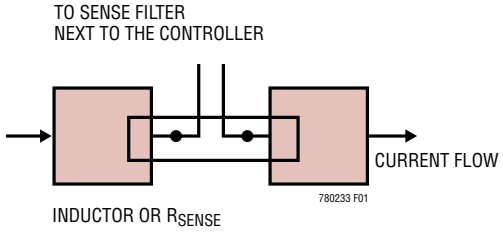


Figure 1. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current. Each controller's current comparator has a maximum threshold $V_{SENSE(MAX)}$ of 50mV. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current (ΔI_L) from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} \le \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

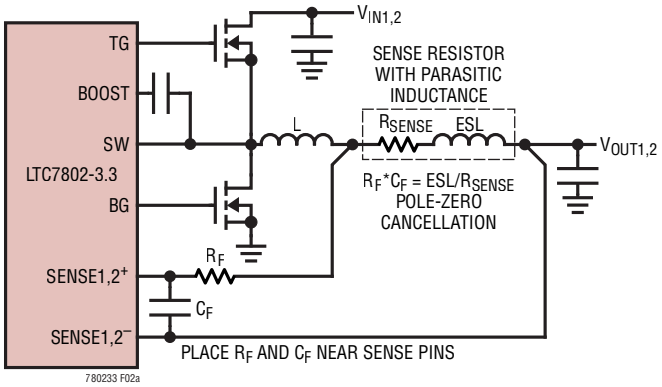
To avoid potential jitter or instability due to PCB noise coupling into the current sense signal, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta_{IL} \bullet R_{SENSE}$ should also be checked to ensure a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a target ΔV_{SENSE} voltage of 10mV to 20mV at nominal input voltage is recommended for both R_{SENSE} and DCR sensing applications.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor value (<3µH) or higher current (>5A) applications. This error is proportional to input voltage and may degrade line regulation or cause loop instability. An RC filter into the sense pins, as shown in Figure 2a, can be used to compensate for this error. Set the RC filter time constant $R_F \bullet C_F = ESL/R_{SENSE}$ for optimal cancellation of the ESL. In general, select C_F to be in the range of 1nF to 10nF and calculate the corresponding R_F. Surface mount sense resistors in low ESL wide footprint geometries are recommended to minimize this error. If not specified on the manufacturer's data sheet, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint and 0.2nH for a 1225 footprint.

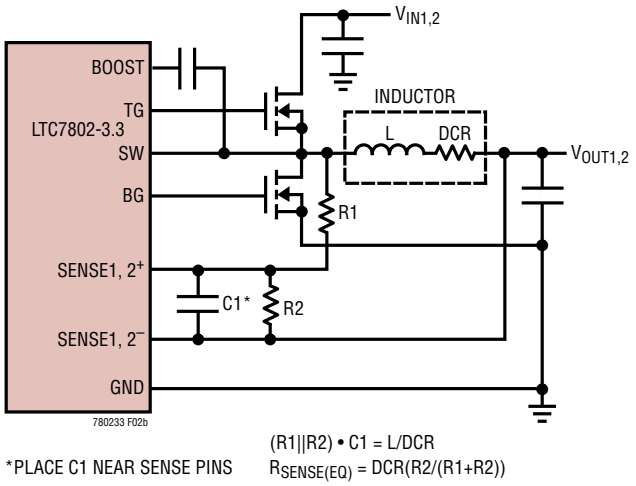
Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7802-3.3 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current

APPLICATIONS INFORMATION



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Current Sensing Methods

inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1+R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current (ΔI_L) from the Inductor Value Calculation section, the target sense resistor value is calculated from the nominal inductance, C1 value, and DCR:

$$R_{SENSE(EQUIV)} \le \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C. To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX\ at\ T_{L(MAX)}}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1||R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ≈1µA current.

The target equivalent resistance R1||R2 is calculated from the nominal inductance, C1 value, and DCR:

$$R1 \| R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1 \| R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

APPLICATIONS INFORMATION

The maximum power loss in R1 is related to duty cycle and occurs in continuous mode at the maximum input voltage:

$$P_{LOSS\ R1} = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Setting the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses, but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications transition losses contribute more significantly to power loss, and a good balance between size and efficiency is generally achieved with a switching frequency between 300kHz and 900kHz. Lower voltage applications benefit from lower switching losses and can therefore more readily operate at higher switching frequencies up to 3MHz if desired. The switching frequency is set using the FREQ and PLLIN/SPREAD pins as shown in Table 1

Table 1.

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
0V	0V	350kHz
$INTV_{CC}$	0V	2.25MHz
Resistor to GND	0V	100kHz to 3MHz
Any of the Above	External Clock 100kHz to 3MHz	Phase-Locked to External lock
Any of the Above	$INTV_{CC}$	Spread Spectrum Modulated

Tying the FREQ pin to ground selects 350kHz while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and ground allows the frequency to be programmed anywhere between 100kHz and 3MHz. Choose a FREQ pin resistor from Figure 3 or the following equation:

$$R_{FREQ}\,(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{OSC}}$$

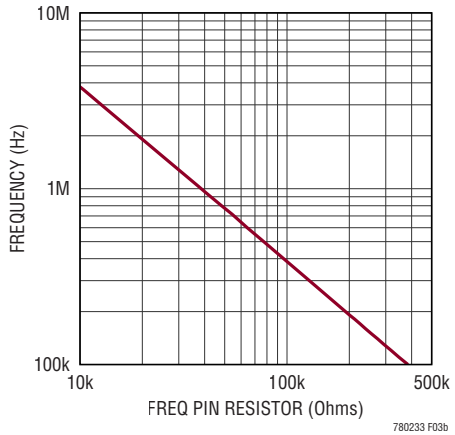


Figure 3. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

To improve electromagnetic interference (EMI) performance, spread spectrum mode can optionally be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum is enabled, the switching frequency modulates within –12% to +15% of the frequency selected by the FREQ pin. Spread spectrum may be used in any operating mode selected by the MODE pin (Burst Mode, pulse-skipping, or forced continuous mode).

A phase-locked loop (PLL) is also available on the LTC7802-3.3 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. After the PLL locks, TG1 is synchronized to the rising edge of the external clock signal, and TG2 is 180° out of phase from TG1. See the Phase-Locked Loop and Frequency Synchronization section for details.

APPLICATIONS INFORMATION

Selecting the Light-Load Operating Mode

The LTC7802-3.3 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE to ground. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100k resistor. An internal 100k resistor from the MODE pin to ground selects Burst Mode if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7802-3.3 operates in pulse-skipping mode if it is selected, or in forced continuous mode otherwise. Table 2. summarizes the use of the MODE pin to select the light load operating mode.

Table 2.

MODE PIN	LIGHT-LOAD OPERATING MODE	MODE WHEN SYNCHRONIZED
0V or Floating	Burst Mode	Forced Continuous
100k to $INTV_{CC}$	Pulse-Skipping	Pulse-Skipping
$INTV_{CC}$	Forced Continuous	Forced Continuous

In general, the requirements of each application will dictate the appropriate choice for light-load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the regulator operates in discontinuous operation. In addition, when the load current is very light, the inductor current will begin bursting at frequencies lower than the switching frequency and enter a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light load.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher light load efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple and EMI.

In some applications, it may be desirable to change light load operating mode based on the conditions present in the system. For example, if a system is inactive, one might select high efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, one might send an external clock to PLLIN/SPREAD, or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. Such on-the-fly mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

Power MOSFET Selection

Two external power MOSFETs must be selected for each controller in the LTC7802-3.3: one N-channel MOSFET for the top (main) switch and one N-channel MOSFET for the bottom (synchronous) switch. The peak-to-peak gate drive levels are set by the $INTV_{CC}$ regulation point of 5.1V. Consequently, logic level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage, and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is

APPLICATIONS INFORMATION

then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{MAIN SWITCH DUTY CYCLE} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{SYNCHRONOUS SWITCH DUTY CYCLE} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ ($\delta \approx 0.005/°C$) and R_{DR} is the effective driver resistance at the MOSFET's Miller threshold voltage ($R_{DR} \approx 2\Omega$). V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $V_{OUT} \bullet I_{OUT}$ product needs to be used in the equation below to determine the maximum RMS capacitor current requirement.

Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single-phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. At maximum load current I_{MAX}, the maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7802-3.3, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC7802-3.3 2-phase operation can be calculated by using this equation for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of

APPLICATIONS INFORMATION

current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing.

The drains of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC7802-3.3, is also suggested. An optional 1Ω to 10Ω resistor placed between C_{IN} and the V_{IN} pin provides further isolation from a noisy input supply.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting the Output Voltage

For channel 1, directly connect the LTC7802-3.3's V_{OUT1} pin to the output to regulate the output voltage to 3.3V. For channel 2, the output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 4. The regulated output voltage is determined by:

$$V_{OUT2} = 0.8V \left(1 + \frac{R_B}{R_A} \right)$$

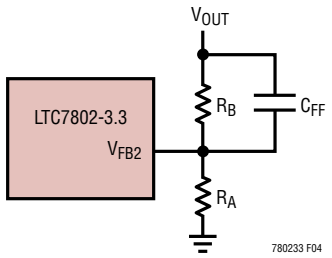


Figure 4. Setting Channel 2 Output Voltage

Place resistors R_A and R_B very close to the V_{FB2} pin to minimize PCB trace length and noise on the sensitive V_{FB2} node. Great care should be taken to route the V_{FB2} trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C_{FF}) may be used.

RUN Pins and Undervoltage Lockout

The two channels of the LTC7802-3.3 are enabled using the RUN1, and RUN2 pins. The RUN pins have a rising threshold of 1.2V with 100mV of hysteresis. Pulling a RUN pin below 1.1V shuts down the main control loop and resets the soft-start for that channel. Pulling both RUN pins below 0.7V disables the controllers and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC7802-3.3 draws only ≈1.5µA of quiescent current.

The RUN pins are high impedance and must be externally pulled up/down or driven directly by logic. Each RUN pin can tolerate up to 40V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down. Do not float the RUN pins.

The RUN pins can also be configured as precise undervoltage lockouts (UVLOs) on the input supply with a resistor divider from V_{IN} to ground, as shown in Figure 5.

The V_{IN} UVLO thresholds can be computed as:

$$UVLO\ RISING = 1.2V \left(1 + \frac{R_1}{R_2} \right)$$

$$UVLO\ FALLING = 1.1V \left(1 + \frac{R_1}{R_2} \right)$$

APPLICATIONS INFORMATION

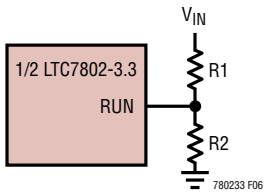


Figure 5. Using the RUN Pins As a UVLD

The current that flows through the R1-R2 divider directly adds to the shutdown, sleep, and active current of the LTC7802-3.3, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range may be required to keep the impact on quiescent shutdown and sleep currents low.

Soft-Start and Tracking (TRACK/SS Pins)

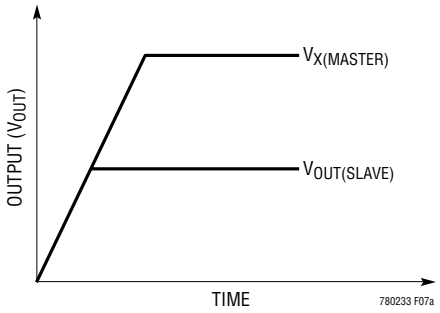
The start-up of each V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2). When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC7802-3.3 regulates the negative input of the Error Amplifier (EA–) to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground. An internal 12.5µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC7802-3.3 will regulate V_{OUT} proportional to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. For a desired soft-start time, t_{SS}, select a soft-start capacitor $C_{SS} = t_{SS} \bullet 15\mu F/sec$.

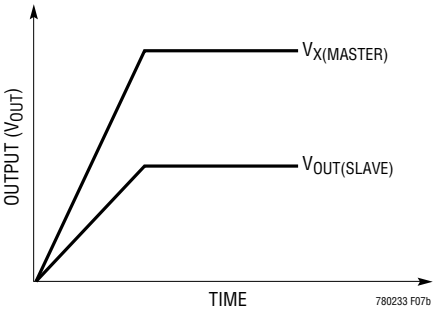
Alternatively, the TRACK/SS pins can be used to track two or more supplies during start-up, as shown qualitatively in Figure 6a and Figure 6b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 7. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

Set $R_{TRACKA} = R_A$ and $R_{TRACKB} = R_B$ for coincident tracking ($V_{OUT} = V_X$ during start-up).



(a) Coincident Tracking



(b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

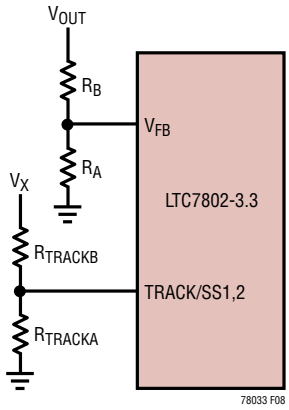


Figure 7. Using the TRACK/SS Pin for Tracking

APPLICATIONS INFORMATION

Single Output 2-Phase Operation

For high power 3.3V output applications, the two channels can be operated in a 2-phase single output configuration. The channels switch 180° out-of-phase, which reduces the required output capacitance in addition to the required input capacitance and power supply induced noise. To configure the LTC7802-3.3for 2-phase operation, tie V_{FB2} to $INTV_{CC}$, ITH2 to ground, and RUN2 to RUN1.

The RUN1, V_{OUT1}, ITH1, TRACK/SS1 pins are then used to control both channels, but each channel uses its own ICMP and IR comparators to monitor their respective inductor currents. Figure 10 is a typical application configured for single output 2-phase operation.

$INTV_{CC}$ Regulators

The LTC7802-3.3 features two separate internal low dropout linear regulators (LDOs) that supply power at the $INTV_{CC}$ pin from either the V_{IN} pin or the $EXTV_{CC}$ pin depending on the $EXTV_{CC}$ pin voltage. $INTV_{CC}$ powers the MOSFET gate drivers and most of the internal circuitry. The V_{IN} LDO and the $EXTV_{CC}$ LDO each regulate $INTV_{CC}$ to 5.1V and can provide a peak current of at least 100mA.

The $INTV_{CC}$ pin must be bypassed to ground with a minimum of 4.7µF ceramic capacitor, placed as close as possible to the pin. An additional 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and GND pins is also highly recommended to supply the high frequency transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7802-3.3 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the V_{IN} LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the V_{IN} LDO is enabled. Power dissipation for the IC in this case is equal to $V_{IN} \bullet IINTV_{CC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC7802-3.3 $INTV_{CC}$ current is limited to less than 35mA from a 36V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$$T_J = 70°C + (35mA)(36V)(43°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above 4.7V (typical), the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above approximately 4.5V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage to 5.1V, so while $EXTV_{CC}$ is less than 5.1V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 5.1V (up to an absolute maximum of 30V), $INTV_{CC}$ is regulated to 5.1V. Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the LTC7802-3.3's switching regulator outputs ($4.8V \le V_{OUT} \le 30V$) during normal operation and from the V_{IN} LDO when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from an output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of $V_{OUT}/(V_{IN} \bullet Efficiency)$. For 5V to 30V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (35mA)(8.5V)(43°C/W) = 83°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

APPLICATIONS INFORMATION

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause $INTV_{CC}$ to be powered from the internal V_{IN} LDO resulting in an efficiency penalty of up to 10% or more at high input voltages.
2. $EXTV_{CC}$ connected directly to one of the regulator outputs. This is the normal connection for an application with an output in the range of 5V to 30V and provides the highest efficiency. If both outputs are in the 5V to 30V range, connect $EXTV_{CC}$ to the lesser of the two outputs to maximize efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available, it may be used to power $EXTV_{CC}$ provided that it is compatible with the MOSFET gate drive requirements. This supply may be higher or lower than V_{IN}; however, a lower $EXTV_{CC}$ voltage results in higher efficiency.
4. $EXTV_{CC}$ connected to an output-derived boost or charge pump. For regulators where both outputs are below 5V, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.8V.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low.

When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). For a typical application, a value of $C_B = 0.1\mu F$ is generally sufficient.

The external diode D_B can be a Schottky diode or silicon diode, but in either case it should have low leakage and fast recovery. The reverse breakdown of the diode must be greater than $V_{IN(MAX)}$. Pay close attention to the reverse leakage at high temperatures where it generally increases substantially.

A leaky diode not only increases the quiescent current of the regulator, but it can create current path from the BOOST pin to $INTV_{CC}$. This will cause $INTV_{CC}$ to rise if the diode leakage exceeds the current consumption on $INTV_{CC}$, which is primarily a concern in Burst Mode operation where the load on $INTV_{CC}$ can be very small. There is an internal voltage clamp on $INTV_{CC}$ that prevents the $INTV_{CC}$ voltage from running away, but this clamp should be regarded as a failsafe only.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC7802-3.3 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the MOSFET. Low duty cycle applications may approach this minimum on time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase. The minimum on-time for the LTC7802-3.3 is approximately 40ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 60ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

APPLICATIONS INFORMATION

Fault Conditions: Current Limit and Foldback

The LTC7802-3.3 includes current foldback to reduce the load current when the output is shorted to ground. If the output voltage falls below 50% of its regulation point, then the maximum sense voltage is progressively lowered from 100% to 40% of its maximum value. Under short-circuit conditions with very low duty cycles, the LTC7802-3.3 will begin cycle skipping to limit the short circuit current. In this situation the bottom MOSFET dissipates most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)} \approx 40ns$, the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet V_{IN}/L$$

The resulting average short-circuit current is:

$$I_{SC} = 40\% \bullet I_{LIM(MAX)} - \Delta I_{L(SC)}/2$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

If an output voltage rises 10% above the set regulation point, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating (such as a short from $INTV_{CC}$ to ground) internal overtemperature shutdown circuitry will shut down the LTC7802-3.3. When the internal die temperature exceeds 180°C, the $INTV_{CC}$ LDO and gate drivers are disabled. When the die cools to 160°C, the LTC7802-3.3 enables the $INTV_{CC}$ LDO and resumes operation beginning with a soft-start startup. Long-term overstress ($T_J > 125°C$) should be avoided as it can degrade the performance or shorten the life of the part.

Phase-Locked Loop and Frequency Synchronization

The LTC7802-3.3 has an internal phase-locked loop (PLL) which allows the turn-on of the top MOSFET of controller 1 to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin. The turn on of controller 2's top MOSFET is thus 180° out of phase with the external clock.

Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase-lock and synchronization. Although it is not required that the free-running frequency be near the external clock frequency, doing so will prevent the oscillator from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7802-3.3 operates in pulse-skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. The LTC7802-3.3 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2V and down to 0.5V or less. Note that the LTC7802-3.3 can only be synchronized to an external clock frequency within the range of 100kHz to 3MHz.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would

APPLICATIONS INFORMATION

produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7802-3.3 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. Other than at very light loads in burst mode, V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f_{SW}(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the top and bottom MOSFETs.

   Supplying $INTV_{CC}$ from an output-derived source through $EXTV_{CC}$ will scale the V_{IN} current required for the driver and control circuits by a factor of $V_{OUT}/(V_{IN} \bullet Efficiency)$. For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the input fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses.

   For example, if each $R_{DS(ON)}$ = 30mΩ, R_L = 50mΩ, R_{SENSE} = 10mΩ and ESR = 40mΩ (sum of both input and output capacitance losses), then the total resistance is 130mΩ. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. This percentage loss varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the top MOSFETs and become significant only when operating at higher input voltages (typically 15V or greater). Transition losses can be estimated from the equation for the main switch power dissipation in the power MOSFET Selection section.

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC7802-3.3 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet (ESR)$, where ESR is the effective

APPLICATIONS INFORMATION

series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Typical Applications circuits provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their initial values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately C_{LOAD} • 25µs/µF. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume $V_{IN(NOMINAL)}$ = 12V, $V_{IN(MAX)}$ = 22V, V_{OUT} = 3.3V, I_{OUT} = 20A, and f_{SW} = 1MHz.

1. Set the operating frequency. The frequency is not one of the internal preset values, so a resistor from the FREQ pin to GND is required, with a value of:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{1\text{MHz}} = 37\text{k}\Omega$$

2. Determine the inductor value. Initially select a value based on an inductor ripple current of 30%. The inductor value can then be calculated from the following equation:

$$L = \frac{V_{OUT}}{f_{SW}(\Delta I_L)}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right) = 0.4\mu\text{H}$$

The highest value of ripple current occurs at the maximum input voltage. In this case the ripple at V_{IN} = 22V is 35%

APPLICATIONS INFORMATION

3. Verify that the minimum on-time of 40ns is not violated. The minimum on-time occurs at $V_{IN(MAX)}$:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f_{SW})} = 150ns$$

This is more than sufficient to satisfy the minimum on time requirement. If the minimum on time is violated, the LTC7802-3.3 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value accordingly adjusted) to avoid operation near the minimum on-time.

4. Select the R_{SENSE} resistor value. The peak inductor current is the maximum DC output current plus half of the inductor ripple current. Or 20A • (1+0.30/2) = 23A in this case. The R_{SENSE} resistor value can then be calculated based on the minimum value for the maximum current sense threshold (45mV):

$$R_{SENSE} \approx \frac{45mV}{23A} \approx 2m\Omega$$

To allow for additional margin, a lower value R_{SENSE} may be used (for example, 1.8mΩ); however, be sure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}/R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.

For this low inductor value and high current application, an RC filter into the SENSE pins should be used to compensate for the parasitic inductance (ESL) of the sense resistor. Assuming an R_{SENSE} geometry of 1225 with a parasitic inductance of 0.2nH, the RC filter time constant should be RC = ESL/R_{SENSE} = 0.2nH/2mΩ = 100ns, which may be implemented with 100Ω resistor in series with the $SENSE^+$ pin and 1nF capacitor between SENSE+ and $SENSE^-$.

5. Select the feedback resistors. If very light load efficiency is required, high value feedback resistors may be used to minimize the current due to the feedback divider. However, in most applications a feedback divider current in the range of 10µA to 100µA or more is acceptable. For a 50µA feedback divider current, R_A = 0.8V/50µA = 16kΩ. R_B can then be calculated as $R_B = R_A(3.3V/0.8V – 1)$ = 50kΩ. For channel 1, the feedback resistor network is implemented internally. Directly connect the V_{OUT1} pin to the output.

6. Select the MOSFETs. The best way to evaluate MOSFET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7802-3.3 demo board. However, an educated guess about the application is helpful to initially select MOSFETs. Since this is a high current, low voltage application, I^2R losses will likely dominate over transition losses for the top MOSFET. Therefore, choose a MOSFET with lower $R_{DS(ON)}$ as opposed to lower gate charge to minimize the combined loss terms. The bottom MOSFET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the bottom MOSFET is typically chosen to be of lower $R_{DS(ON)}$ and subsequently higher gate charge than the top MOSFET.

Due to the high current in this application, two MOSFETs may needed in parallel to more evenly balance the dissipated power and to lower the $R_{DS(ON)}$. Be sure to select logic-level threshold MOSFETs, since the gate drive voltage is limited to 5.1V ($INTV_{CC}$). Minimize the inductance of the TG and BG gate drive traces and their respective return paths to the controller IC (SW and GND) by using wide traces and multiple parallel vias.

7. Select the input and output capacitors. C_{IN} is chosen for an RMS current rating of at least 10A ($I_{OUT}/2$, with margin) at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 3mΩ for low output ripple. Multiple capacitors connected in parallel may be required to reduce the ESR to this level. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE}$ = ESR • ΔI_L = 3mΩ • 6A = $18mV_{P-P}$

On the 3.3V output, this is equal to 0.55% of peak to peak voltage ripple.

APPLICATIONS INFORMATION

8. Determine the bias supply components. Since the regulated output is not greater than the $EXTV_{CC}$ switchover threshold (4.7V), it cannot be used to bias $INTV_{CC}$. However, if another supply is available, for example if the other channel is regulating to 5V, connect that supply to $EXTV_{CC}$ to improve the efficiency.

   For a 6.5ms soft-start, select a 0.1µF capacitor for the TRACK/SS pin. As a first pass estimate for the bias components, select C_{INTVCC} = 4.7µF, boost supply capacitor C_B = 0.1µF and low forward drop boost supply diode CMDSH-4E from Central Semiconductor.

9. Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUN pin can be used to control the minimum input voltage for regulator operation or can be tied to V_{IN} for always-on operation. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

   For more detailed layout guidance, see Analog Devices Application Notes AN136 “PCB Layout Considerations for Non-Isolated Switching Power Supplies” and AN139 “Power Supply Layout and EMI”.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. Figure 8 illustrates the current waveforms present in the various branches of the synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs located within 1cm of each other with a common drain connection at C_{IN}? Decoupling capacitors for the two channels should be close to each other to avoid a large resonant loop.

2. Are the signal and power grounds kept separate? The combined IC ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The area of the “hot loop” formed by the top N-channel MOSFET, bottom N-channel MOSFET and the high frequency (ceramic) input capacitors, as shown in Figure 8, should be minimized with short leads, planar connections, and multiple paralleled vias where needed. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.

3. Do the LTC7802-3.3 V_{OUT1} pin and V_{FB2} pin’s resistive divider connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. Place the divider close to the V_{FB2} pin to minimize noise coupling into the sensitive V_{FB2} node. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).

4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? Route these traces away from the high frequency switching nodes, on an inner layer if possible. The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.

5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET drivers’ current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially. The boost diodes should have separate routes directly to the $INTV_{CC}$ capacitor near the IC, not shared with any signal connections to $INTV_{CC}$.

6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the other channel’s voltage and current sensing feedback pins. All of these nodes have very large and fast-moving signals and therefore should be kept on the output side of the LTC7802-3.3 and occupy minimum PC trace area. Minimize the inductance of the TG and BG gate drive traces and their respective return paths to the controller IC (SW and GND) by using wide traces and multiple parallel vias.

APPLICATIONS INFORMATION

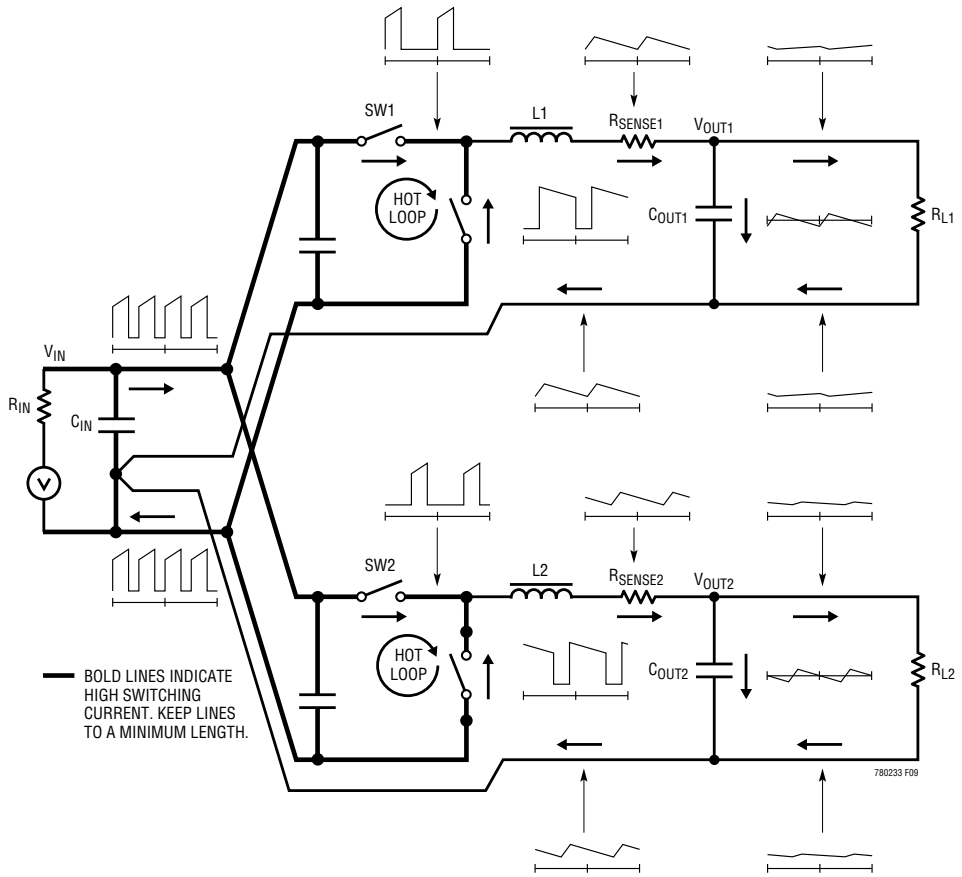


Figure 8. Branch Current Waveforms

APPLICATIONS INFORMATION

7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC. For more detailed layout guidance, see Analog Devices Application Notes AN136 "PCB Layout Considerations for Non-Isolated Switching Power Supplies" and AN139 "Power Supply Layout and EMI".

PC Board Layout Debugging

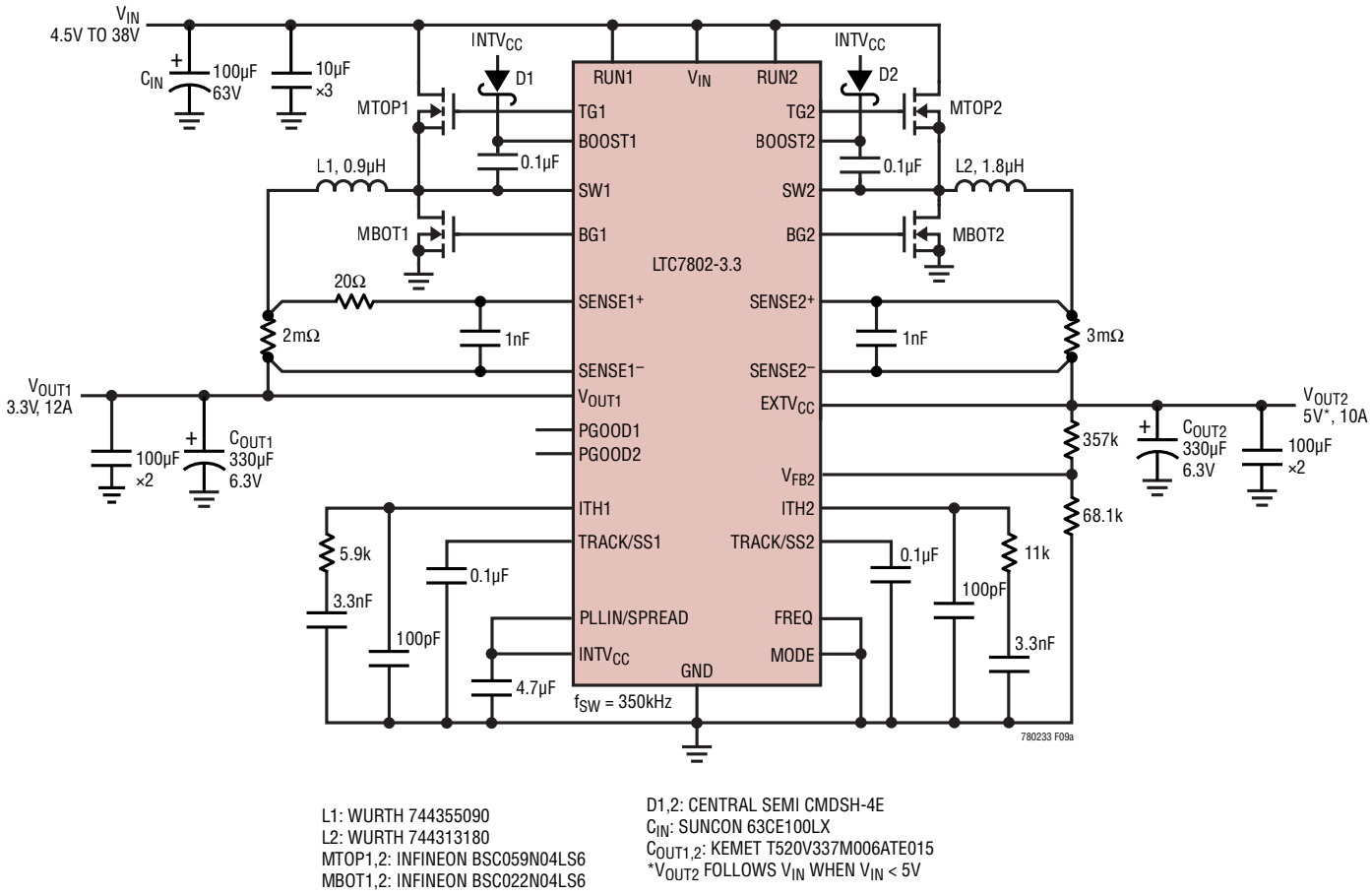
Start with one controller on at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation. Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the top MOSFET, and the bottom MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

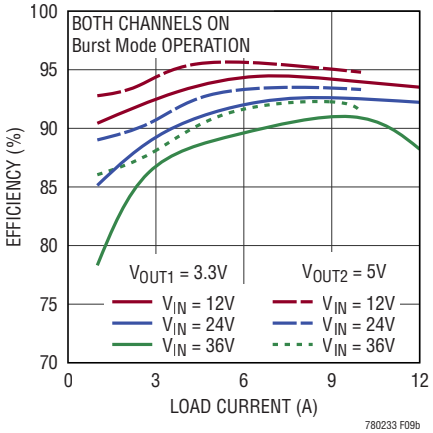
TYPICAL APPLICATIONS



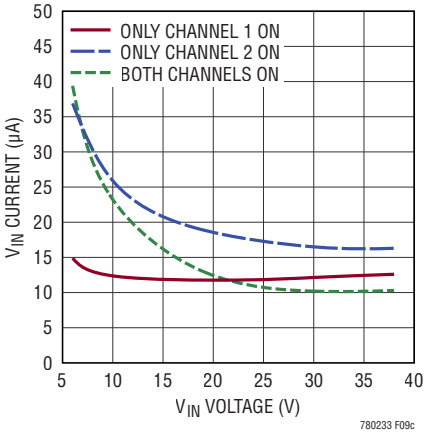
L1: WURTH 744355090
L2: WURTH 744313180
MTOP1,2: INFINEON BSC059N04LS6
MBOT1,2: INFINEON BSC022N04LS6

D1,2: CENTRAL SEMI CMDSH-4E
C_{IN}: SUNCON 63CE100LX
$C_{OUT1,2}$: KEMET T520V337M006ATE015
*V_{OUT2} FOLLOWS V_{IN} WHEN V_{IN} < 5V

Efficiency vs Load Current



No-Load Burst Mode Input Current vs Input Voltage



Short-Circuit Response

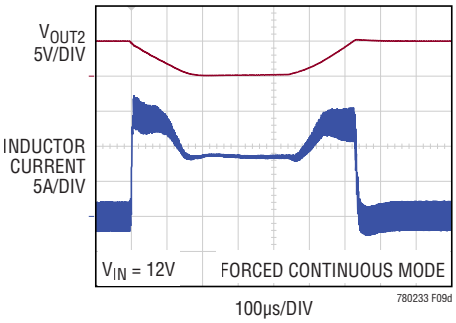
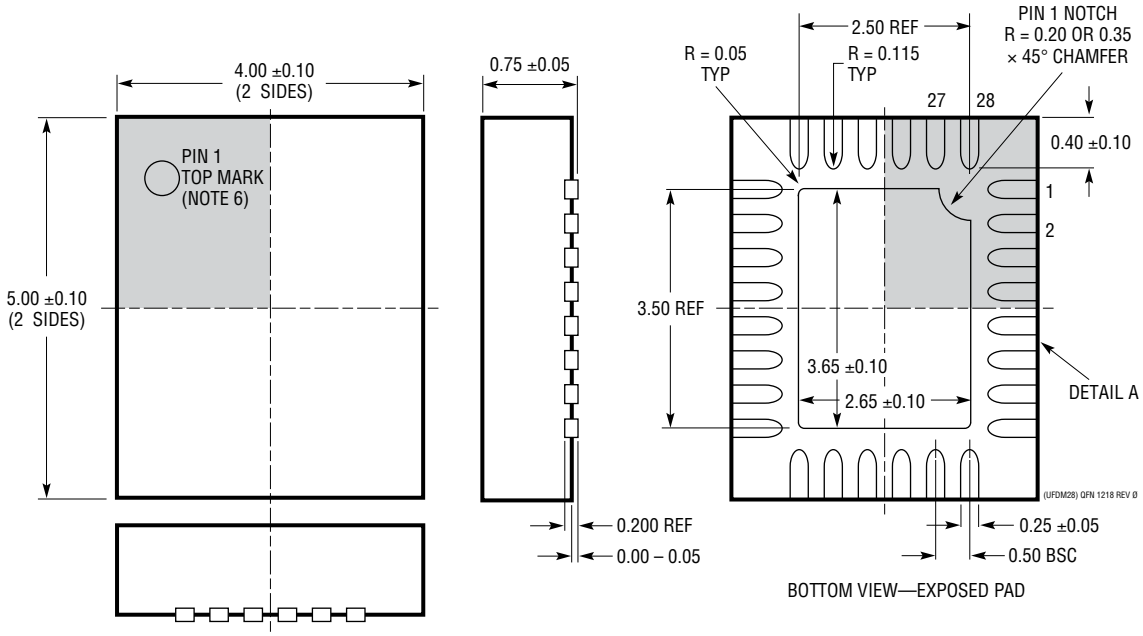


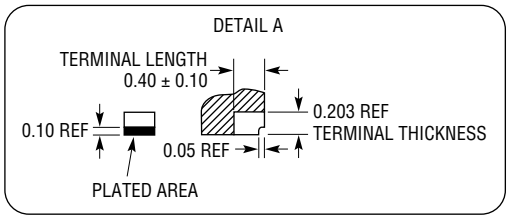
Figure 9. High Efficiency Dual 3.3V, 5V Step-Down Regulator with Spread Spectrum

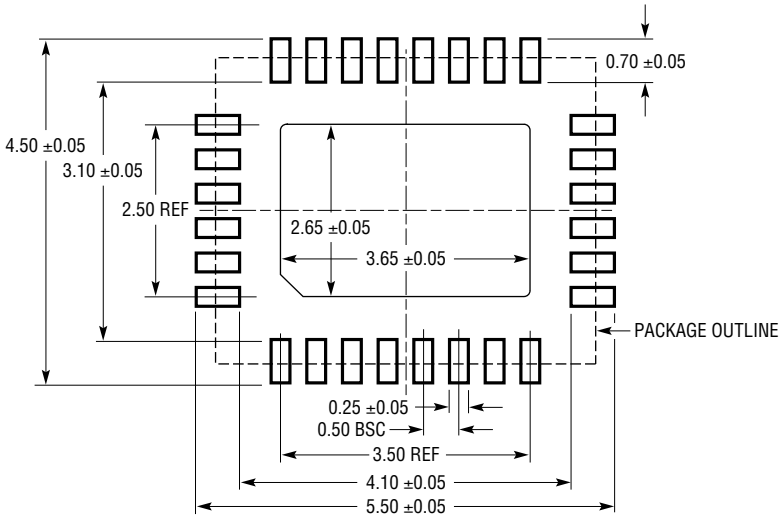
PACKAGE DESCRIPTION

UFDM Package
28-Lead Plastic Side Wettable QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1682 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION

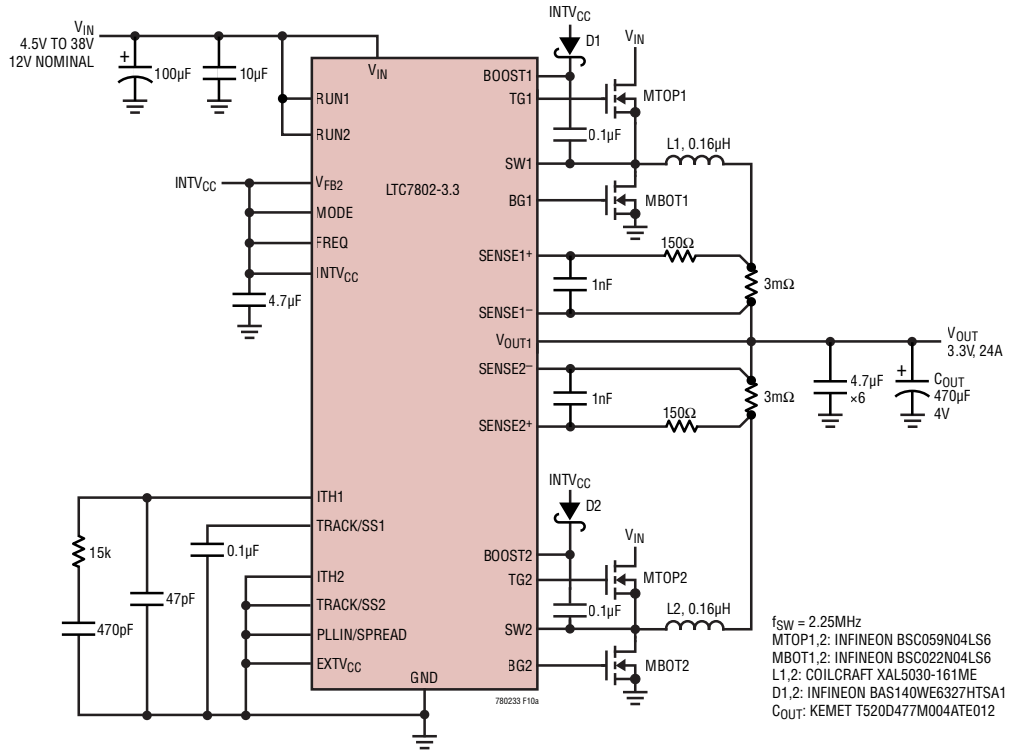


Figure 10. 2.25MHz 2-Phase Single Output 3.3V, 24A Step-Down Regulator

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7802	40V Dual Low I_Q, 3MHz 2-Phase Synchronous Step-Down Controller with Spread Spectrum	4.5V ≤ V_{IN} ≤ 40V, V_{OUT} Up to 40V, I_Q = 12µA Fixed Frequency 100kHz to 3MHz, 4mm X 5mm QFN-28
LTC7803	40V Low I_Q, 100% Duty Cycle, Synchronous Step-Down Controller with Spread Spectrum	4.5V ≤ V_{IN} ≤ 40V, V_{OUT} Up to 40V, I_Q = 12µA Fixed Frequency 100kHz to 3MHz, 3mm X 3mm QFN-16/ MSOP-16
LTC3807	38V Low I_Q, Synchronous Step-Down Controller with 24V Output Voltage Capability	4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA PLL Fixed Frequency 50kHz to 900kHz, 3mm x 4mm QFN-20/ TSSOP-20
LTC3890/LTC3890-1	60V, Low I_Q, Dual 2-Phase Synchronous	4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA PLL Fixed Frequency 50kHz to 900kHz
LTC3890-2/LTC3890-3	Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz
LTC3892	60V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with Adjustable Gate drive Voltage	4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 29µA PLL Fixed Frequency 50kHz to 900kHz,
LTC3850	Dual, 2-Phase Synchronous Step-Down DC/DC Controller	4V≤ V_{IN} ≤ 24V, V_{OUT} up to 5.5V PLL Fixed Frequency 250kHz to 750kHz
LTC3855	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temperature Compensation	4.5V≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 12V PLL Fixed Frequency 250kHz to 770kHz, Excellent current Share
LTC3869/LTC3869-2	Dual Output, 2-Phase Synchronous Step-Down DC/DC Controller, with Accurate Current Share	4V ≤ V_{IN} ≤ 38V, V_{OUT} up to 12.5V PLL Fixed 250kHz to 750kHz Frequency,
LTC3875	Dual, 2-Phase, Synchronous Controller with Sub-Milliohm DCR Sensing and Temperature Compensation	4.75V ≤ V_{IN} ≤ 38V; 0.6V ≤ V_{OUT} ≤ 3.5V/5V Excellent current Share
LTC3774	Dual, Mulitphase Curent Mode Synchronous Step-Down DC/DC Controller for Sub-Milliohm DCR Sensing	Operates with DrMOS, Power Blocks or External Drivers/MOSFETs, 4.5V≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V