FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00024-5v0-E

*Memory FRAM*

# 4 M (256 K × 16) Bit

# MB85R4M2T

## ■ DESCRIPTIONS

The MB85R4M2T is an FRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R4M2T is able to retain data without using a back-up battery, as is needed for SRAM.

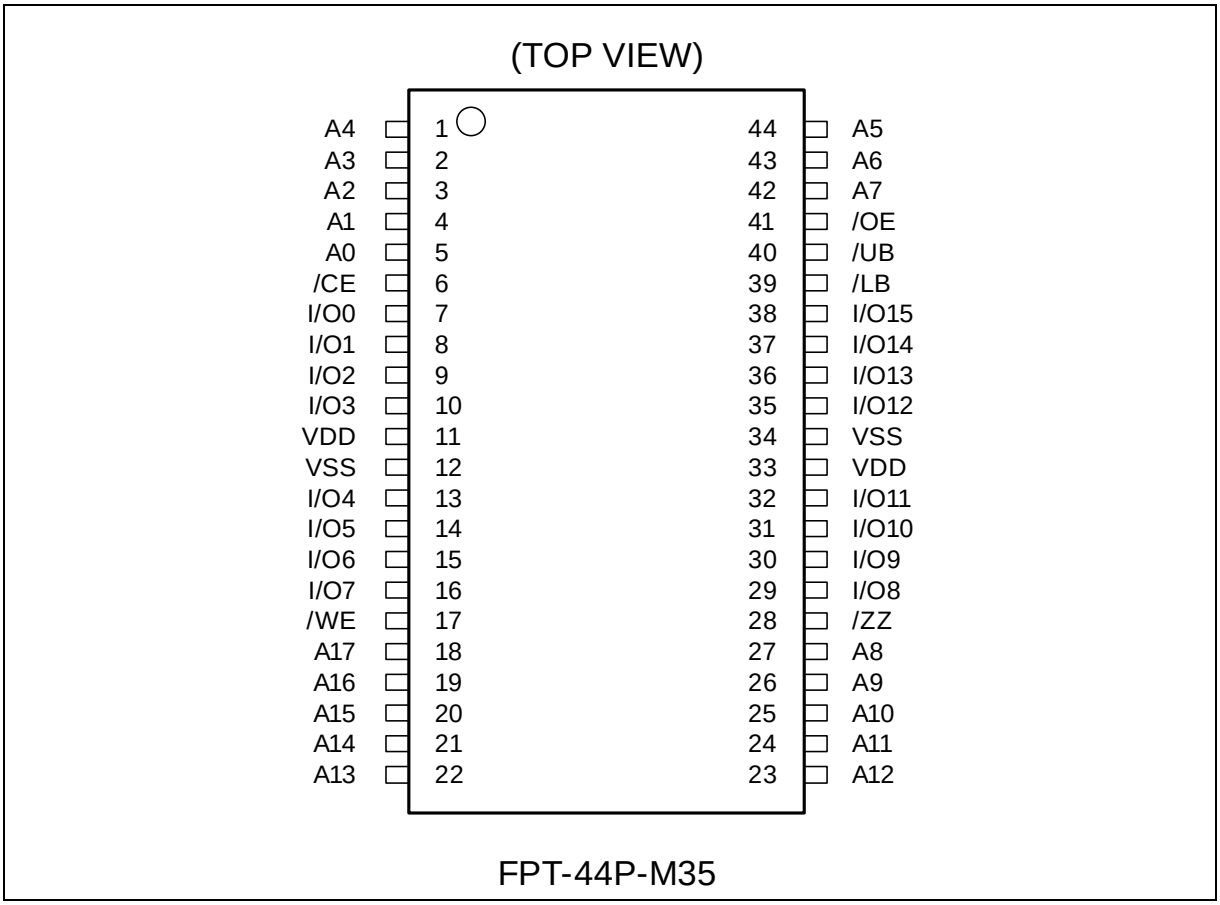
The memory cells used in the MB85R4M2T can be used for $10^{13}$ read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MB85R4M2T uses a pseudo-SRAM interface.

## ■ FEATURES

- Bit configuration : 262,144 words × 16 bits
- LB and UB data byte control : Available Configuration of 524,288 words × 8 bits
- Read/write endurance : $10^{13}$ times / 16 bits
- Data retention : 10 years ( + 85 °C), 95 years ( + 55 °C), over 200 years ( + 35 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power operation : Operating power supply current 20 mA (Max)
  Standby current 150 μA (Max)
  Sleep current 20 μA (Max)
- Operation ambient temperature range : − 40 °C to + 85 °C
- Package : 44-pin plastic TSOP (FPT-44P-M35)
  RoHS compliant


2019.02

## ■ PIN ASSIGNMENTS

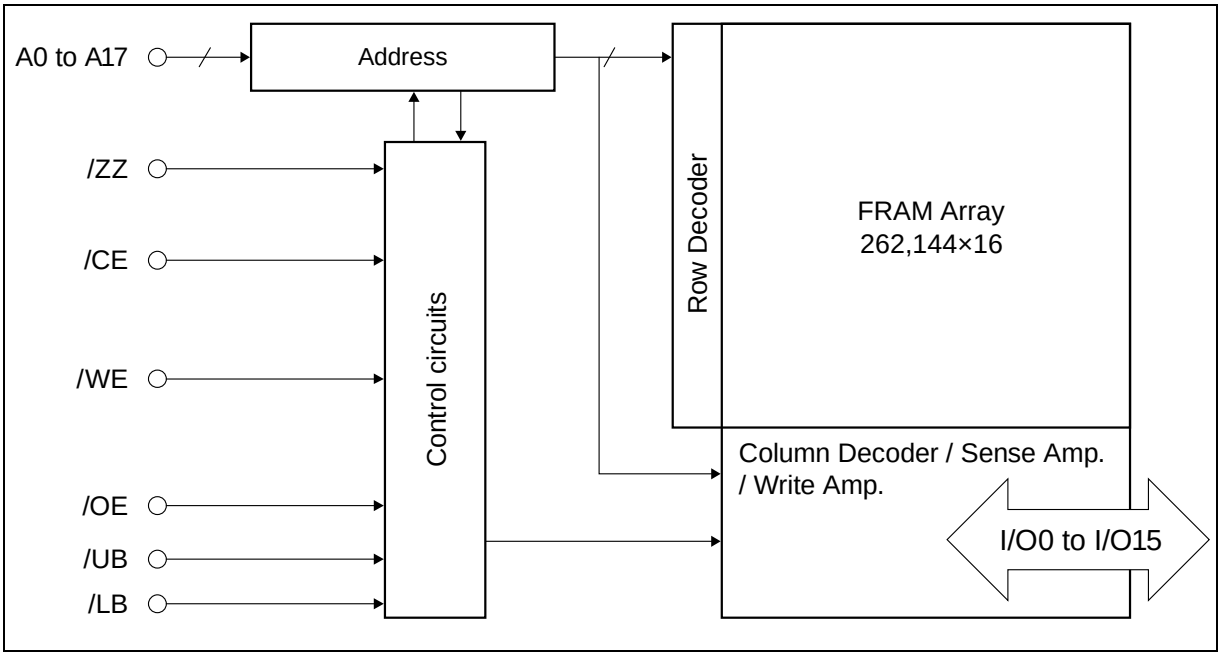


## ■ PIN DESCRIPTIONS

| Pin Number | Pin Name | Functional Description |
|---|---|---|
| 1 to 5, 18 to 22,<br>23 to 27, 42 to 44 | A0 to A17 | Address Input pins<br>Select 262,144 words in FRAM memory array by 18 Address Input pins. When these address inputs are changed during /CE equals to “L” level, reading operation of data selected in the address after transition will start. |
| 7 to 10, 13 to 16,<br>29 to 32, 35 to 38 | I/O0 to I/O15 | Data Input/Output pins<br>These are 16 bits bidirectional pins for reading and writing. |
| 6 | /CE | Chip Enable Input pin<br>In case the /CE equals to “L” level and /ZZ equals to “H” level, device is activated and enables to start memory access.<br>In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FRAM memory array. |
| 17 | /WE | Write Enable Input pin<br>Writing operation starts at the falling edge of /WE.<br>Input data from I/O pins are latched at the rising edge of /WE and written to FRAM memory array. |
| 41 | /OE | Output Enable Input pin<br>When the /OE is “L” level, valid data are output to data bus.<br>When the /OE is “H” level, all I/O pins become high impedance (High-Z) state. |
| 28 | /ZZ | Sleep Mode Input pin<br>When the /ZZ becomes to “L” level, device transits to the Sleep Mode.<br>During reading and writing operation, /ZZ pin shall be hold “H” level. |
| 39, 40 | /LB, /UB | Lower/Upper byte Control Input pins<br>In case /LB or /UB equals to “L” level, it enables reading/writing operation of I/O0 to I/O7 or I/O8 to I/O15 respectively. In case /LB and /UB equal to “H” level, all I/O pins become High-Z state. |
| 11, 33 | VDD | Supply Voltage pins<br>Connect all two pins to the power supply. |
| 12, 34 | VSS | Ground pins<br>Connect all two pins to ground. |

Note: Please refer to the timing diagram for functional description of each pin.

## ■ BLOCK DIAGRAM



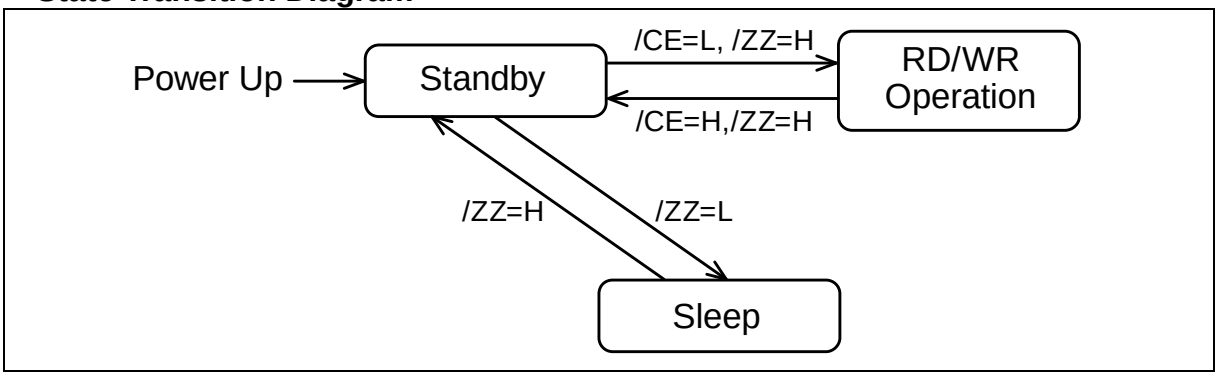

## ■ FUNCTIONAL TRUTH TABLE

| Operation Mode | /CE | /WE | /OE | A0 to A17 | /ZZ |
|---|---|---|---|---|---|
| Sleep | × | × | × | × | L |
| Standby | H | × | × | × | H |
| Read | ↓ | H | L | H or L | H |
| Address Access Read | L | H | L | ↑ or ↓ | H |
| Write(/CE Control)*1 | ↓ | L | × | H or L | H |
| Write(/WE Control)*1*2 | L | ↓ | × | H or L | H |
| Address Access Write*1*3 | L | ↓ | × | ↑ or ↓ | H |
| Pre-charge | ↑ | × | × | × | H |

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑

*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.
*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.
*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

## ■ State Transition Diagram




## ■ FUNCTIONAL TRUTH TABLE OF BYTE CONTROL

| Operation Mode | /WE | /OE | /LB | /UB | I/O0 to I/O7 | I/O8 to I/O15 |
|---|---|---|---|---|---|---|
| Read(Without Output) | H | H | × | × | Hi-Z | Hi-Z |
| | H | × | H | H | Hi-Z | Hi-Z |
| Read(I/O8 to I/O15) | H | L | H | L | Hi-Z | Output |
| Read(I/O0 to I/O7) | | | L | H | Output | Hi-Z |
| Read(I/O0 to I/O15) | | | L | L | Output | Output |
| Write(I/O8 to I/O15) | ↑ | × | H | L | × | Input |
| Write(I/O0 to I/O7) | | | L | H | Input | × |
| Write(I/O0 to I/O15) | | | L | L | Input | Input |

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑
Hi-Z= High Impedance

In case the byte reading or writing are not selected, /LB and /UB pins shall be connected to GND pin.
In writing, please don’t switch /LB and/or /UB during /CE=”L”.

## ■ ABABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Power Supply Voltage* | $V_{DD}$ | − 0.5 | + 4.0 | V |
| Input Pin Voltage* | $V_{IN}$ | − 0.5 | $V_{DD}$ + 0.5 ( ≤ 4.0) | V |
| Output Pin Voltage* | $V_{OUT}$ | − 0.5 | $V_{DD}$ + 0.5 ( ≤ 4.0) | V |
| Operation Ambient Temperature | $T_A$ | − 40 | + 85 | °C |
| Storage Temperature | Tstg | − 55 | + 125 | °C |

* : All voltages are referenced to VSS (ground 0 V).

**WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.**

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power Supply Voltage*1 | $V_{DD}$ | 1.8 | 3.3 | 3.6 | V |
| Operation Ambient Temperature*2 | $T_A$ | − 40 | — | + 85 | °C |

*1: All voltages are referenced to VSS (ground 0 V).

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

**WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.**

**Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.**

**No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.**

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input Leakage Current | $\|I_{LI}\|$ | $V_{IN}$ = 0V to $V_{DD}$ | — | — | 5 | µA |
| Output Leakage Current | $\|I_{LO}\|$ | $V_{OUT}$ = 0V to $V_{DD}$<br>/CE = $V_{IH}$ or /OE = $V_{IH}$ | — | — | 5 | µA |
| Operating Power Supply Current*1 | $I_{DD}$ | /CE = 0.2 V, $I_{out}$ = 0 mA | — | 15 | 20 | mA |
| Standby Current | $I_{SB}$ | /ZZ ≥ $V_{DD}$ − 0.2V<br>/CE, /WE, /OE ≥ $V_{DD}$ − 0.2V<br>/LB, /UB ≥ $V_{DD}$ − 0.2V<br>Others ≥ $V_{DD}$ − 0.2V or ≤ 0.2V | — | 30 | 150 | µA |
| Sleep Current | $I_{ZZ}$ | /ZZ = $V_{SS}$<br>/CE, /WE, /OE ≥ $V_{DD}$ − 0.2V<br>/LB, /UB ≥ $V_{DD}$ − 0.2V<br>Others ≥ $V_{DD}$ − 0.2V or ≤ 0.2V | — | 5 | 20 | µA |
| High Level Input Voltage | $V_{IH}$ | $V_{DD}$ = 1.8V to 3.6V | $V_{DD}$ × 0.8 | — | $V_{DD}$ + 0.3 | V |
| Low Level Input Voltage | $V_{IL}$ | $V_{DD}$ = 1.8V to 3.6V | − 0.3 | — | $V_{DD}$ × 0.17 | V |
| High Level Output Voltage | $V_{OH1}$ | $V_{DD}$ = 2.7V to 3.6V<br>$I_{OH}$ = − 1.0mA | $V_{DD}$ × 0.8 | — | — | V |
| | $V_{OH2}$ | $V_{DD}$ = 1.8V to 2.7V<br>$I_{OH}$ = − 100µA | $V_{DD}$ − 0.2 | — | — | |
| Low Level Output Voltage | $V_{OL1}$ | $V_{DD}$ = 2.7V to 3.6V<br>$I_{OL}$ = 2.0mA | — | — | 0.4 | V |
| | $V_{OL2}$ | $V_{DD}$ = 1.8V to 2.7V<br>$I_{OL}$ = 150µA | — | — | 0.2 | |

*1: During the measurement of $I_{DD}$, all Address and I/O were taken to only change once per active cycle.
Iout : output current

## 2. AC Characteristics

### ▪ AC Test Conditions

| | |
|---|---|
| Power Supply Voltage | : 1.8 V to 3.6 V |
| Operation Ambient Temperature | : − 40 °C to + 85 °C |
| Input Voltage Amplitude | : 0 V / $V_{DD}$ |
| Input Rising Time | : 3 ns |
| Input Falling Time | : 3 ns |
| Input Evaluation Level | : $V_{DD}$/2 |
| Output Evaluation Level | : $V_{DD}$/2 |
| Output Load Capacitance | : 30 pF |

### (1) Read Cycle

| Parameter | Symbol | Value ($V_{DD}$=1.8V to 2.7V) | | Value ($V_{DD}$=2.7V to 3.6V) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Read Cycle time | $t_{RC}$ | 185 | — | 150 | — | ns |
| /CE Access Time | $t_{CE}$ | — | 95 | — | 75 | ns |
| Address Access Time | $t_{AA}$ | — | 185 | — | 150 | ns |
| /CE Output Data Hold time | $t_{OH}$ | 0 | — | 0 | — | ns |
| Address Access Output Output Data Hold time | $t_{OAH}$ | 20 | — | 20 | — | ns |
| /CE Active Time | $t_{CA}$ | 95 | — | 75 | — | ns |
| Pre-charge Time | $t_{PC}$ | 90 | — | 75 | — | ns |
| /LB, /UB Access Time | $t_{BA}$ | — | 35 | — | 20 | ns |
| Address Setup Time | $t_{AS}$ | 0 | — | 0 | — | ns |
| Address Hold Time | $t_{AH}$ | 95 | — | 75 | — | ns |
| /CE↑ to Address Transition time*1 | $t_{CAH}$ | 0 | — | 0 | — | ns |
| /OE Access Time | $t_{OE}$ | — | 35 | — | 20 | ns |
| /CE Output Floating Time*1 | $t_{HZ}$ | — | 10 | — | 10 | ns |
| /OE Output Floating Time | $t_{OHZ}$ | — | 10 | — | 10 | ns |
| /LB, /UB Output Floating Time | $t_{BHZ}$ | — | 10 | — | 10 | ns |
| Address Transition Time*1 | $t_{AX}$ | — | 15 | — | 15 | ns |

*1: Same parameters with the Write cycle.

### (2) Write Cycle

| Parameter | Symbol | Value ($V_{DD}$=1.8V to 2.7V) | | Value ($V_{DD}$=2.7V to 3.6V) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 185 | — | 150 | — | ns |
| /CE Active Time | $t_{CA}$ | 95 | — | 75 | — | ns |
| /CE↓ to /WE↑ Time | $t_{CW}$ | 95 | — | 75 | — | ns |
| Pre-charge Time | $t_{PC}$ | 90 | — | 75 | — | ns |
| Write Pulse Width | $t_{WP}$ | 20 | — | 20 | — | ns |
| Address Setup Time | $t_{AS}$ | 0 | — | 0 | — | ns |
| Address Hold Time | $t_{AH}$ | 95 | — | 75 | — | ns |
| /WE↓ to /CE↑ Time | $t_{WLC}$ | 20 | — | 20 | — | ns |
| Address Transition to /WE↑ Time | $t_{AWH}$ | 185 | — | 150 | — | ns |
| /WE↑ to Address Transition Time | $t_{WHA}$ | 0 | — | 0 | — | ns |
| /LB, /UB Setup Time | $t_{BS}$ | 2 | — | 2 | — | ns |
| /LB, /UB Hold Time | $t_{BH}$ | 0 | — | 0 | — | ns |
| Data Setup Time | $t_{DS}$ | 10 | — | 10 | — | ns |
| Data Hold Time | $t_{DH}$ | 0 | — | 0 | — | ns |
| /WE Output Floating Time | $t_{WZ}$ | — | 10 | — | 10 | ns |
| /WE Output Access Time*1 | $t_{WX}$ | 10 | — | 10 | — | ns |
| Write Setup Time*1 | $t_{WS}$ | 0 | — | 0 | — | ns |
| Write Hold Time*1 | $t_{WH}$ | 0 | — | 0 | — | ns |

*1: Writing operation applies “Write Cycle Timing 1” or “Write Cycle Timing 2” by the relation of /CE and /WE timing. The values of $t_{WX}$, $t_{WS}$ and $t_{WH}$ are defined by these operations. The conditions of $t_{WS}$ and $t_{WH}$ are not checked at shipping test.

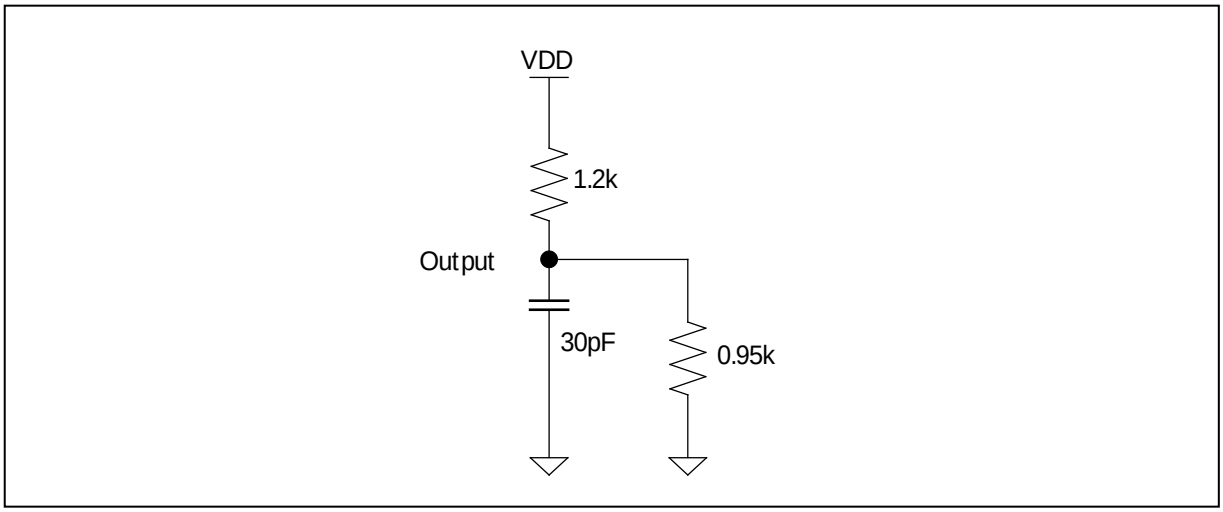
### (3) Power ON/OFF Sequence and Sleep Mode Cycle

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| /CE level hold time for Power ON | $t_{PU}$ | 450 | — | µs |
| /CE level hold time for Power OFF | $t_{PD}$ | 85 | — | ns |
| Power supply rising time | $t_{VR}$ | 50 | — | µs/V |
| Power supply falling time | $t_{VF}$ | 100 | — | µs/V |
| /ZZ active time | $t_{ZZL}$ | 1 | — | µs |
| Sleep mode enable time | $t_{ZZEN}$ | — | 0 | µs |
| /CE level hold time for Sleep mode release | $t_{ZZEX}$ | 450 | — | µs |

### 3. Pin Capacitance

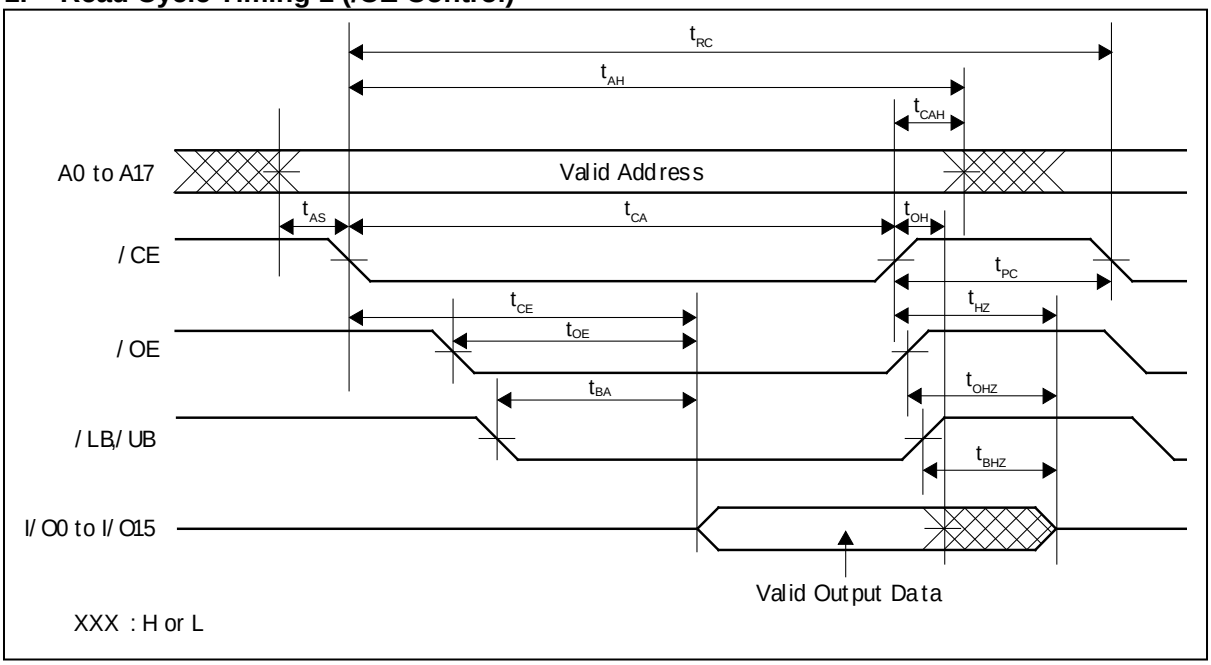
| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input Capacitance | $C_{IN}$ | $V_{DD}$ = 3.3 V, f = 1 MHz, $T_A$ = + 25 °C | — | — | 6 | pF |
| Input/Output Capacitance (I/O pin) | $C_{I/O}$ | | — | — | 8 | pF |
| /ZZ Pin Input Capacitance | $C_{ZZ}$ | | — | — | 8 | pF |

## ■ AC Test Load Circuit

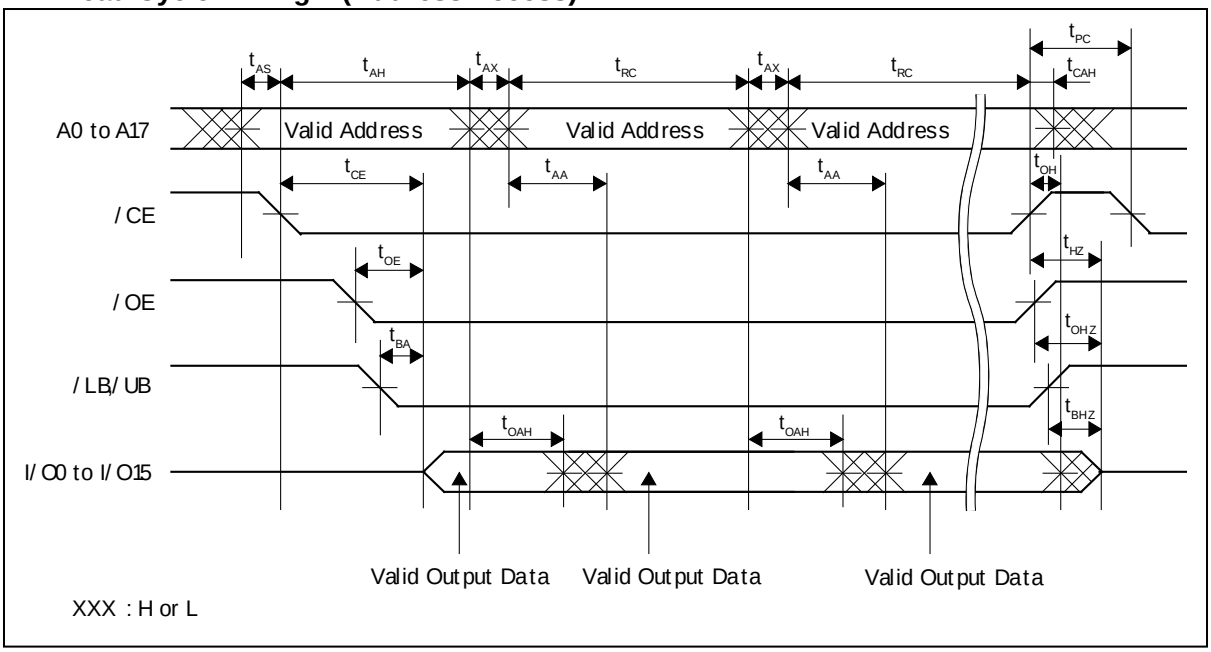


## ■ TIMING DIAGRAMS

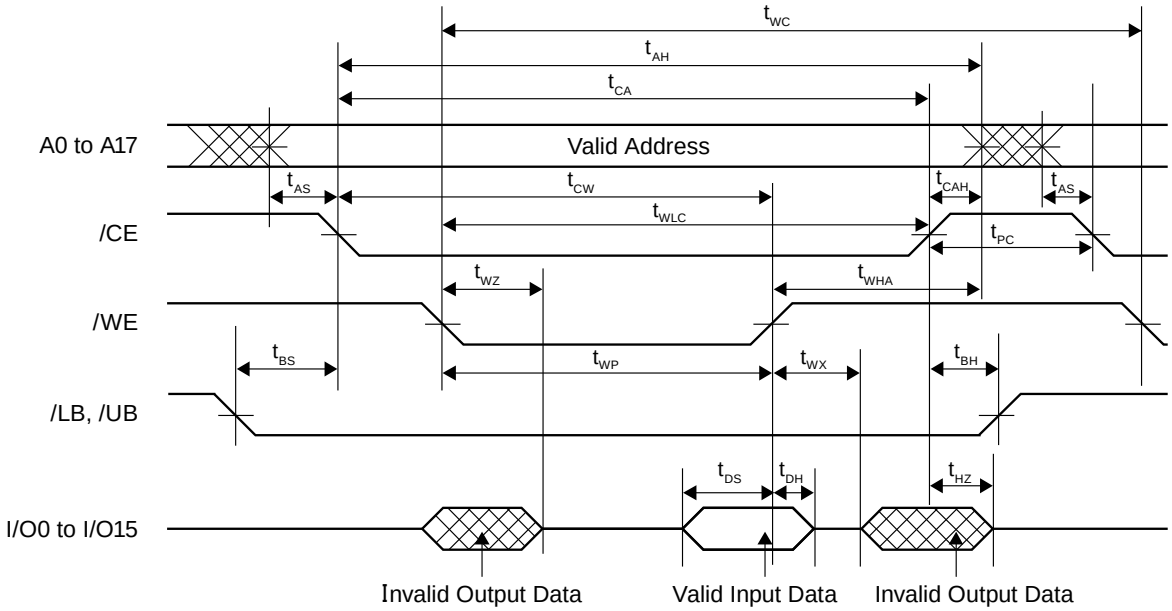
### 1. Read Cycle Timing 1 (/CE Control)




### 2. Read Cycle Timing 2 (Address Access)



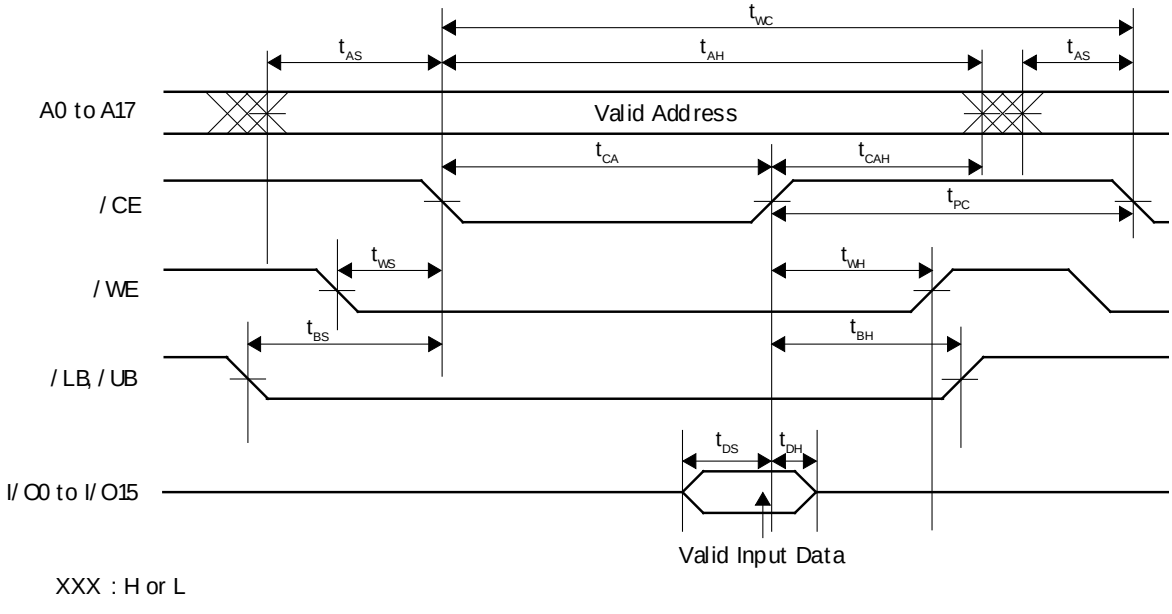
### 3. Write Cycle Timing 1 (/WE Control)




XXX : H or L

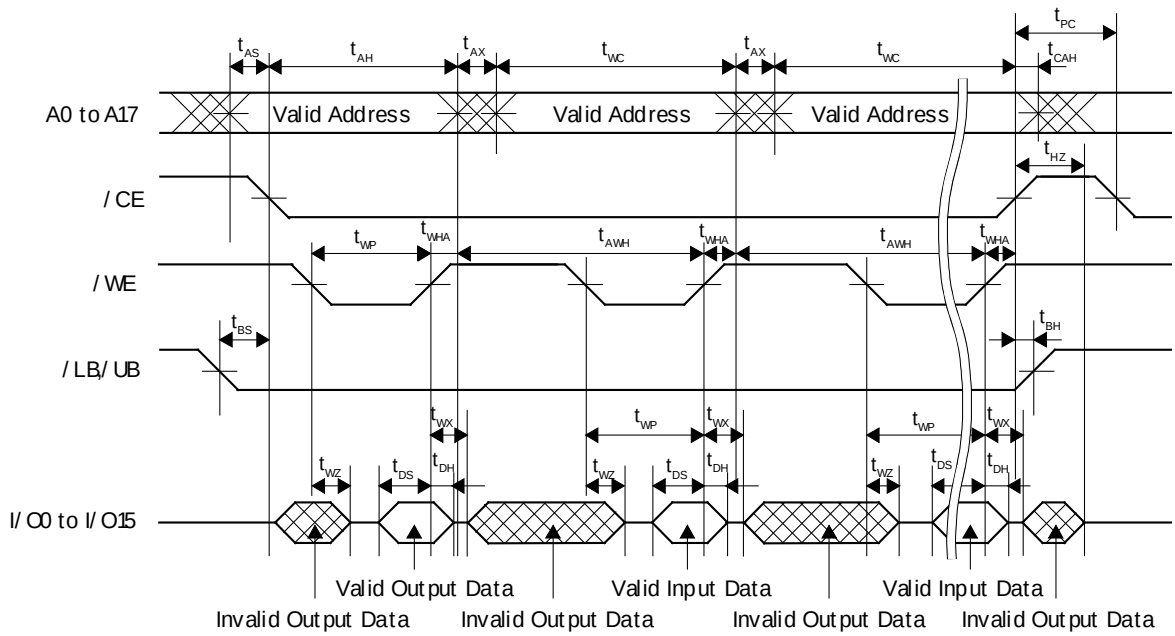
* : In case the /OE is “L” level, invalid data are output to data bus.
* : In case the /OE is “L” level, any bus conflict of input and output data shall not occur.

### 4. Write Cycle Timing 2 (/CE Control)




XXX : H or L

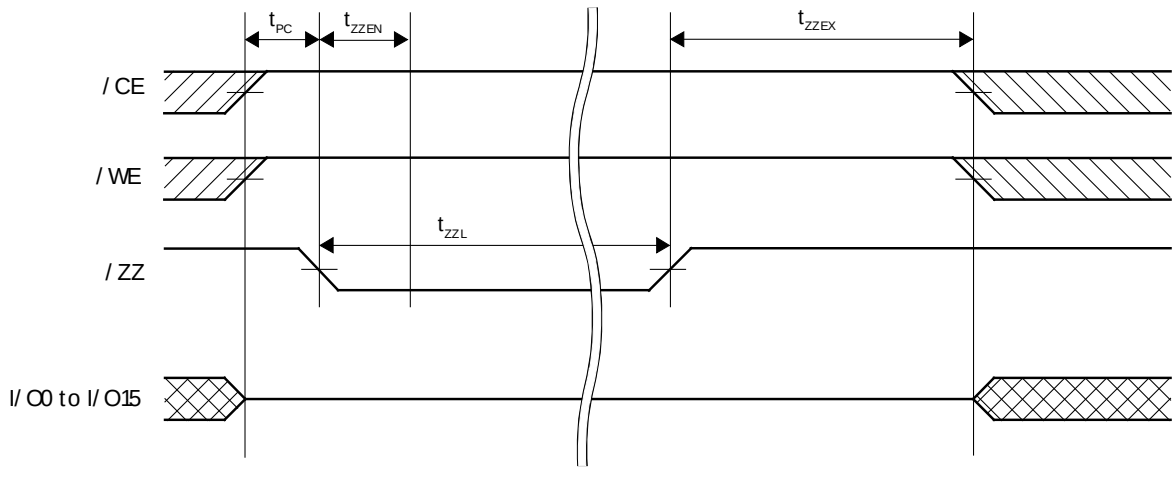
## 5. Write Cycle Timing 3 (Address Access and /WE Control)



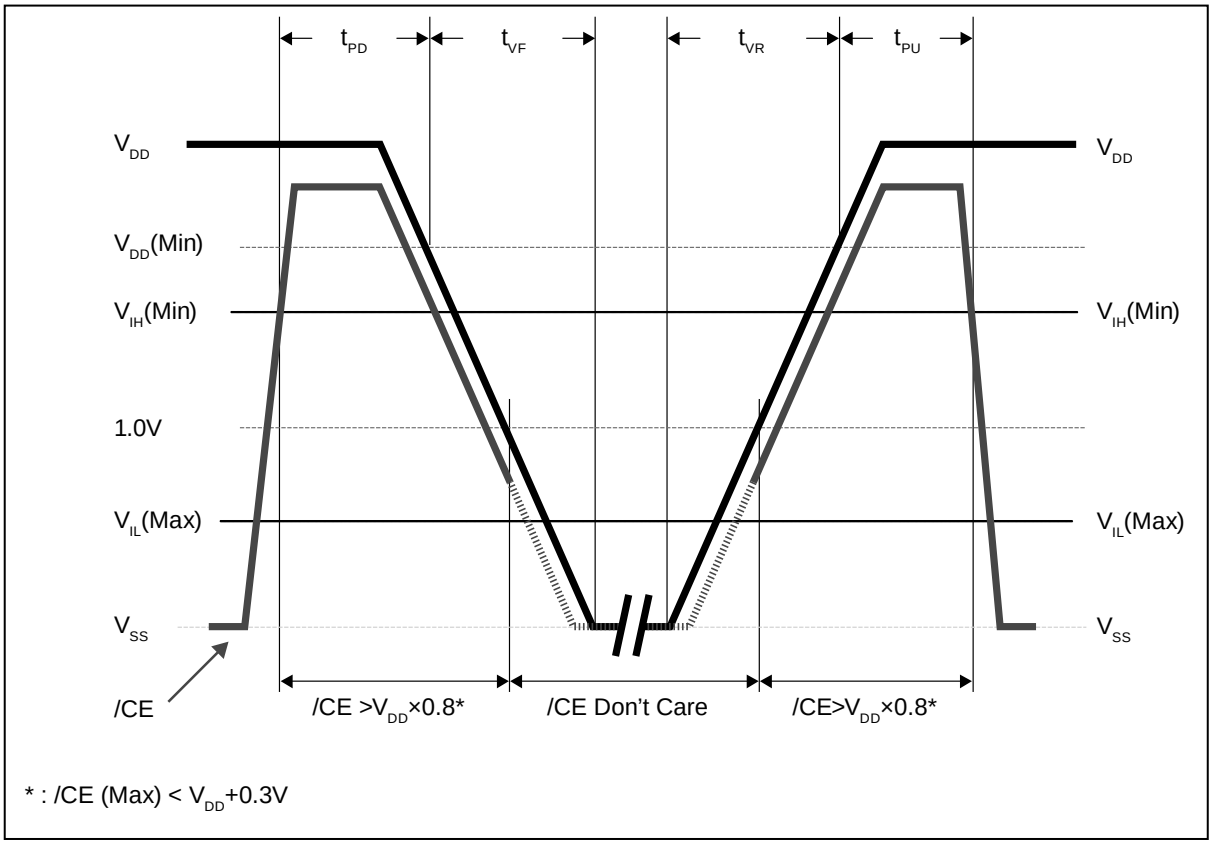

XXX : H or L

* : In case the / OE is "L" level, invalid data are output to data bus.
* : In case the / OE is "L" level, any bus conflict of input and output data shall not occur.

## 6. Sleep Mode Timing



## ■ POWER ON/OFF SEQUENCE




* : /CE (Max) < $V_{DD}$+0.3V

## ■ FRAM CHARACTERISTICS

| Item | Min | Max | Unit | Parameter |
|---|---|---|---|---|
| Read/Write Endurance*1 | $10^{13}$ | — | Times/16 bits | Operation Ambient Temperature $T_A$ = + 85 °C |
| Data Retention*2 | 10 | — | Years | Operation Ambient Temperature $T_A$ = + 85 °C |
| | 95 | — | | Operation Ambient Temperature $T_A$ = + 55 °C |
| | ≥ 200 | — | | Operation Ambient Temperature $T_A$ = + 35 °C |

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

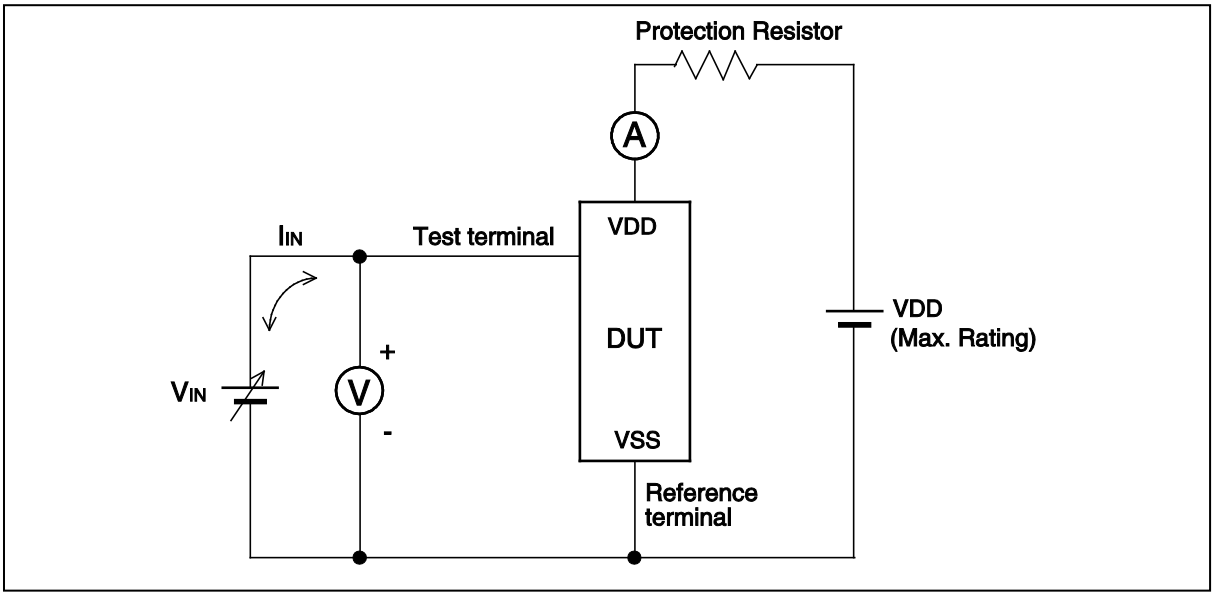
## ■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

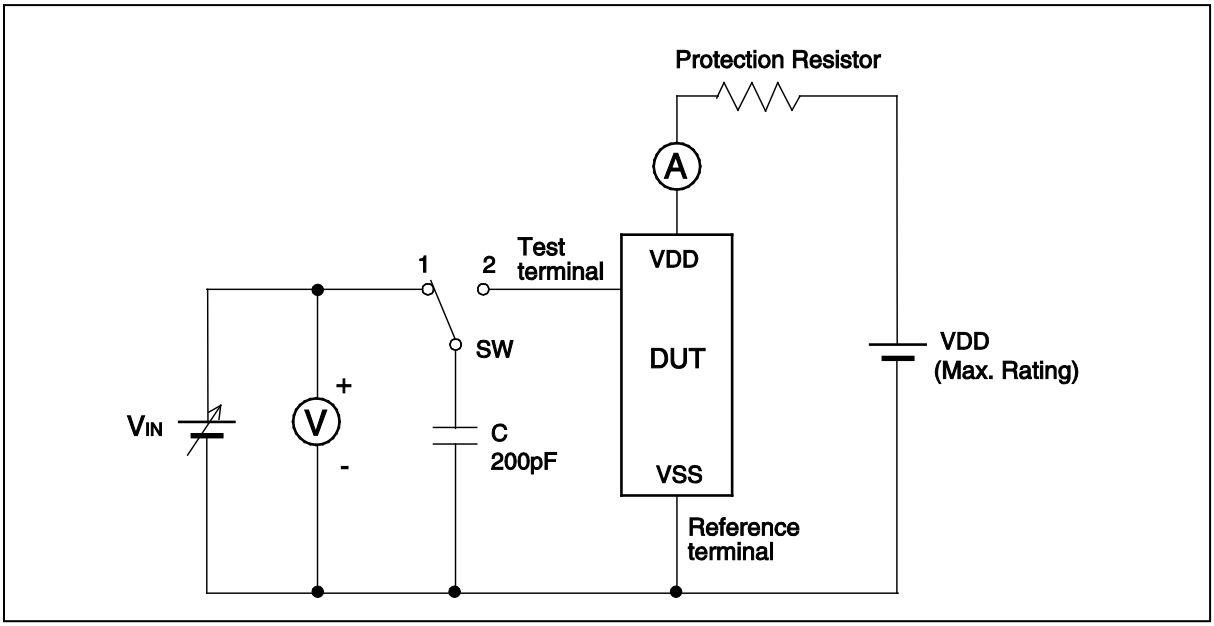
| Test | DUT | Value |
|---|---|---|
| ESD HBM (Human Body Model)<br>JESD22-A114 compliant | MB85R4M2TFN-G-JAE2 | ≥ \|2000 V\| |
| ESD MM (Machine Model)<br>JESD22-A115 compliant | | ≥ \|200 V\| |
| ESD CDM (Charged Device Model)<br>JESD22-C101 compliant | | — |
| Latch-Up (I-test)<br>JESD78 compliant | | — |
| Latch-Up ($V_{supply}$ overvoltage test)<br>JESD78 compliant | | — |
| Latch-Up (Current Method)<br>Proprietary method | | — |
| Latch-Up (C-V Method)<br>Proprietary method | | ≥ \|200 V\| |

**・Current method of Latch-Up Resistance Test**




Note: The voltage VIN is increased gradually and the current $I_{IN}$ of 300 mA at maximum shall flow.
Confirm the latch up does not occur under $I_{IN} = \pm 300$ mA.
In case the specific requirement is specified for I/O and $I_{IN}$ cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

・**C-V method of Latch-Up Resistance Test**




Note: Charge voltage alternately switching 1 and 2 approximately 2 sec intervals. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

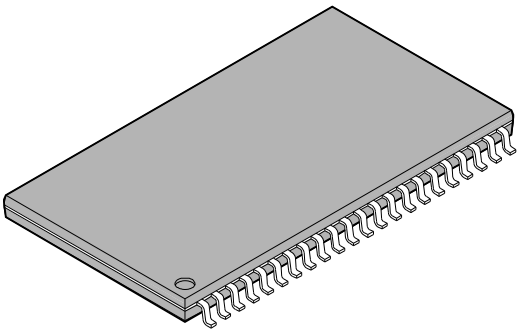
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

## ■ ORDERING INFORMATION

| Part Number | Package | Shipping form | Minimum shipping quantity |
|---|---|---|---|
| MB85R4M2TFN-G-JAE2 | 44-pin plastic TSOP (FPT-44P-M35) | Tray | —* |

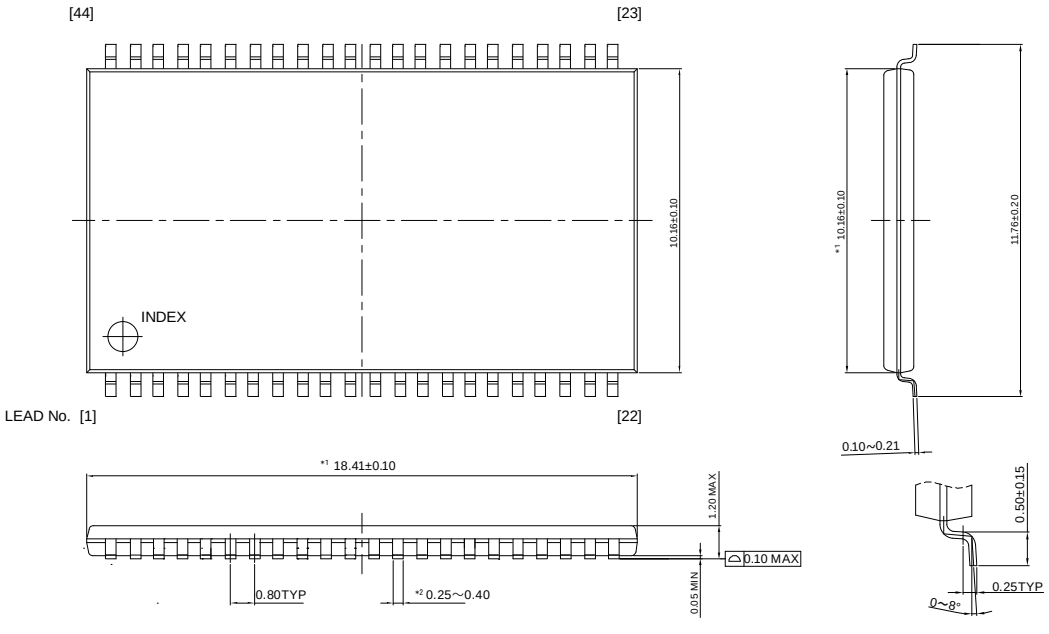
*: Please contact our sales office about minimum shipping quantity.

## ■ PACKAGE DIMENSIONS

| 44-pin plastic TSOP | | |
|---|---|---|
|  FPT-44P-M35 / MB85R4M2T | Lead pitch | 0.8mm |
| | Package width × package length | 10.16 × 18.41mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.2mm |
| | | |
| | | |

44-pin plastic TSOP
（FPT-44P-M35）

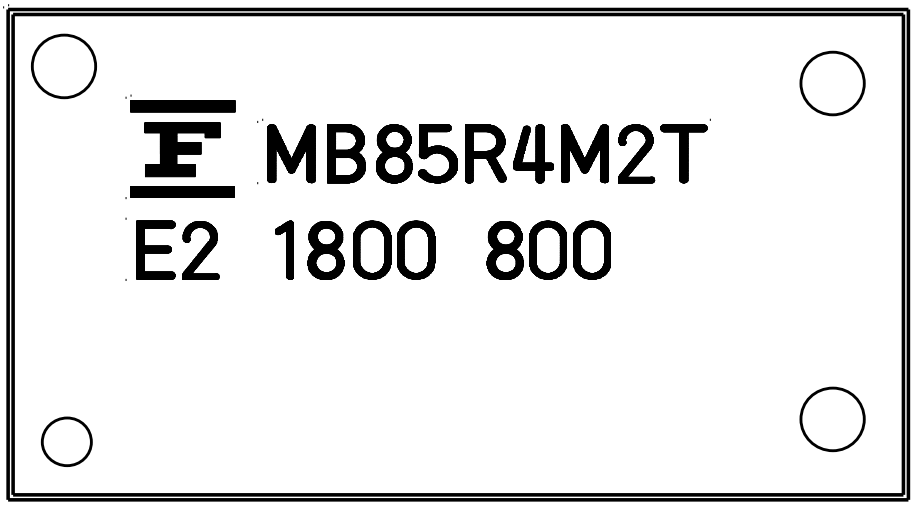
Note 1) *1: These dimensions do not include resin protrusion.
Note 2) *2: These dimensions do not include tie bar cutting remainder.
Pins width and pins thickness include plating thickness.




Dimensions in mm.

## ■ MARKING

[MB85R4M2TFN-G-JAE2]




[FPT-44P-M35]

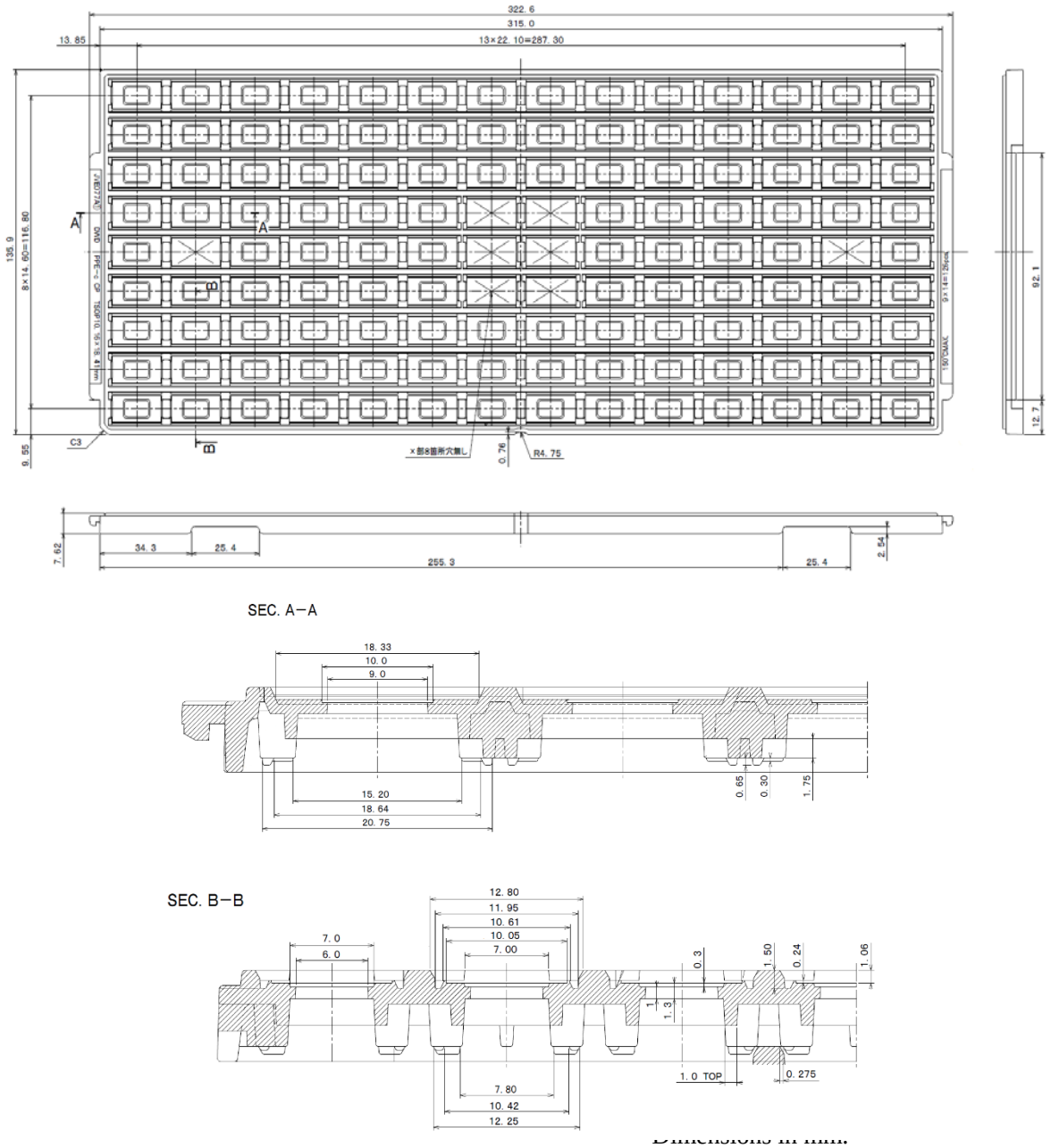
## ■ PACKING

1. Tray

1.1 Tray dimensions

| | PKG code | Maximum storage capacity | | |
|---|---|---|---|---|
| | | pcs/tray | pcs/inner box | pcs/outer box |
| | FPT-44P-M35 | 126 | 1260<br>(10trays) | 5040<br>(4 inner boxes, Max) |

FPT44

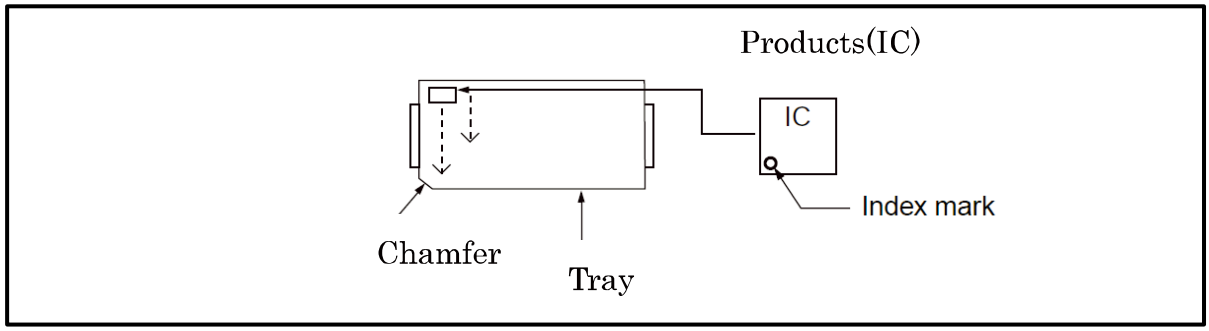



Dimensions in mm.

Material: Conductive-Polyphenyleneether(PPE)

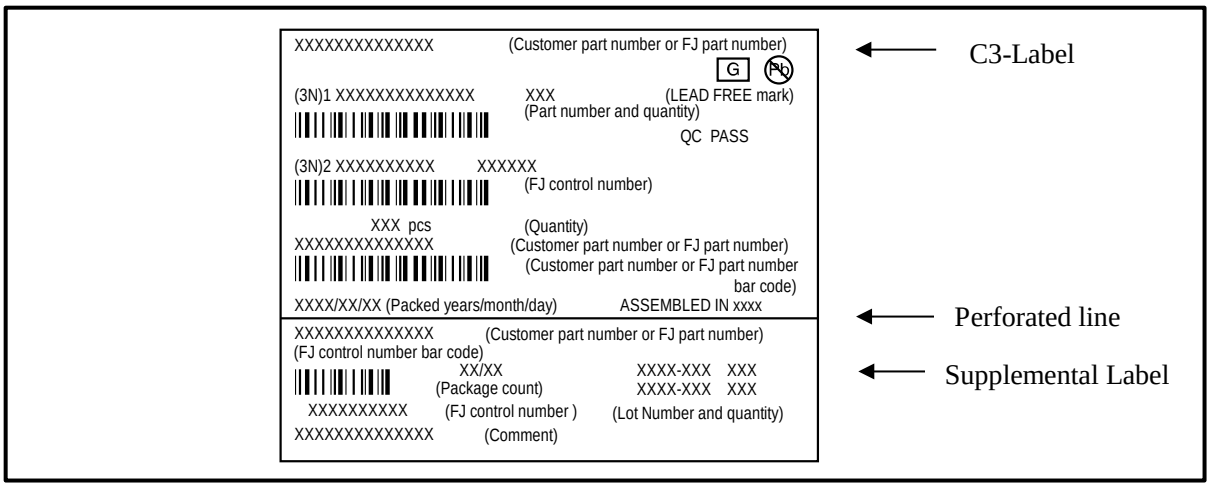
Heat resistance temperature: 150℃(max)

1.2 IC orientation



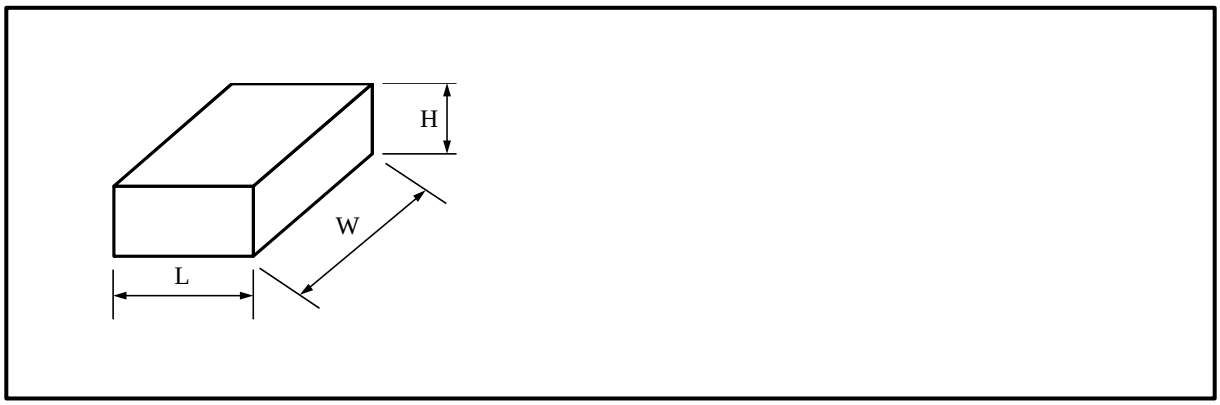

1.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



1.4 Dimensions for container

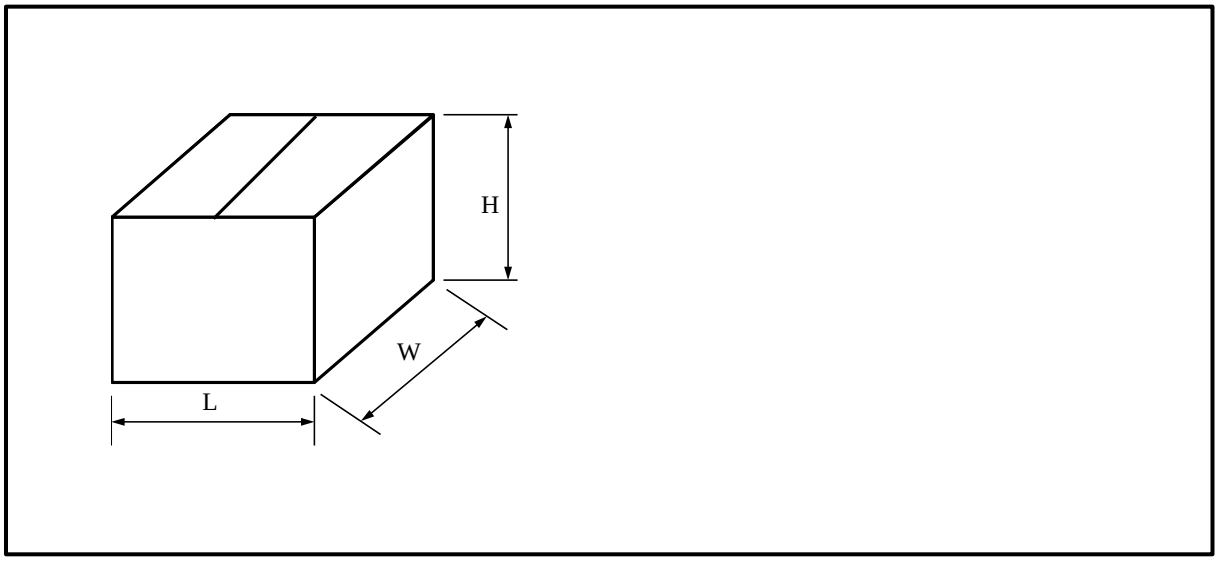
(1) Dimensions for inner box




| L | W | H |
|---|---|---|
| 162 | 360 | 90 |

(Dimensions in mm)

(2) Dimensions for outer box




| L | W | H |
|---|---|---|
| 410 | 375 | 225 |

(Dimensions in mm)

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Change Results |
|---|---|---|
| 1<br>2<br>17<br>18<br>19 | ■ **FEATURES**<br>■ **PIN ASSINGMENTS**<br>■ **ORDERING INFORMATION**<br>■ **PACKAGE DIMENSION**<br>■ **MARKING** | Package code is changed.<br>Part Number is changed.<br>Marking is changed. |
| 5 | ■ **FUNCTONAL TRUTH TABLE OF BYTE CONTROL** | Following comment is added.<br>In writing, please don't switch /LB and/or /UB during /CE="L". |
| 8 | ■ **ELECTRICAL CHARACTERISTICS**<br>**2. AC Characteristics** | tOH and tOAH are redefined.<br>tOH: /CE Output Data Hold time<br>tOAH: Address Access Output Output Data Hold time |
| 20 | ■ **PACKING** | Packing information is added. |

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