



AT28HC256

Military Grade 256-Kbit (32,768 x 8) High-Speed Paged Parallel EEPROM

Features

- Fast Read Access Time: 90 ns
- Automatic Page Write Operation:
 - Internally organized as 32,768 x 8 (256K)
 - Internal address and data latches for 64 bytes
 - Internal control timer
- Fast Write Cycle Time:
 - Page Write cycle time: 3 ms or 10 ms maximum
 - 1 to 64-byte Page Write operation
- Low-Power Dissipation:
 - 80 mA active current
 - 3 mA CMOS standby current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology:
 - Endurance: 10,000 or 100,000 cycles
 - Data retention: 10 years
- Single 5V \pm 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC[®] Approved Byte-Wide Pinout
- Full Military Temperature Range

Packages

- 32-Lead CERDIP, 32-Lead Flatpack, 32-Lead CLCC and 30-Pin PGA

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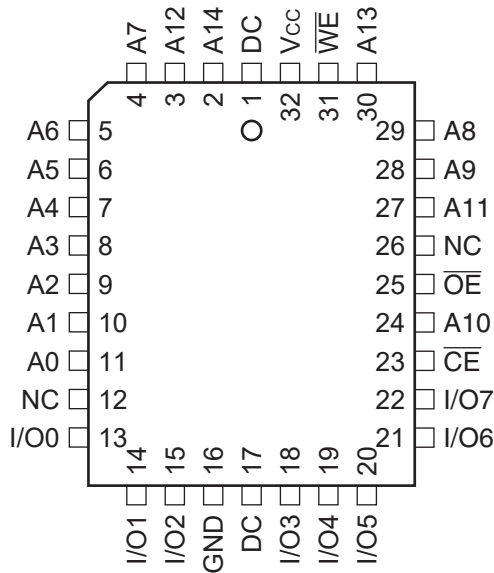
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1. Package Types (not to scale)

32-Pad CLCC⁽¹⁾

Top View



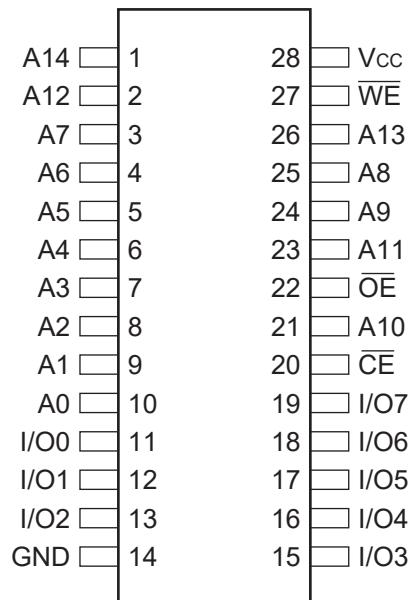
28-Lead PGA

Top View

| | | | | |
|------------|------------|----------------|-----------------------|------------|
| 4 A6 | 3 A7 | 1 A14 | 27 \overline{WE} | 26 A13 |
| 5 A5 | 2 A12 | 28 V_{cc} | 24 A9 | 25 A8 |
| 7 A3 | 6 A4 | | 22 \overline{OE} | 23 A11 |
| 9 A1 | 8 A2 | | 20 \overline{CE} | 21 A10 |
| 11 I/O0 | 10 A0 | 14 GND | 16 I/O4 | 19 I/O7 |
| 12 I/O1 | 13 I/O2 | 15 I/O3 | 17 I/O5 | 18 I/O6 |

28-Lead Cerdip/Flatpack

Top View



Note:

1. CLCC package pins 1 and 17 are "Don't Connect".

2. Pin Descriptions

The descriptions of the pins are listed in [Table 2-1](#).

Table 2-1. Pin Function Table

| Name | 32-Lead CERDIP | 32-Lead CLCC | 32-Lead FLATPACK | 30-Pin PGA | Function |
|-----------------|----------------|--------------|------------------|------------|---------------------|
| DC | — | 1 | — | — | Don't Connect |
| A14 | 1 | 2 | 1 | 1 | Address |
| A12 | 2 | 3 | 2 | 2 | Address |
| A7 | 3 | 4 | 3 | 3 | Address |
| A6 | 4 | 5 | 4 | 4 | Address |
| A5 | 5 | 6 | 5 | 5 | Address |
| A4 | 6 | 7 | 6 | 6 | Address |
| A3 | 7 | 8 | 7 | 7 | Address |
| A2 | 8 | 9 | 8 | 8 | Address |
| A1 | 9 | 10 | 9 | 9 | Address |
| A0 | 10 | 11 | 10 | 10 | Address |
| NC | — | 12 | — | — | No Connect |
| I/O0 | 11 | 13 | 11 | 11 | Data Input/Output |
| I/O1 | 12 | 14 | 12 | 12 | Data Input/Output |
| I/O2 | 13 | 15 | 13 | 13 | Data Input/Output |
| GND | 14 | 16 | 14 | 14 | Ground |
| DC | — | 17 | — | — | Don't Connect |
| I/O3 | 15 | 18 | 15 | 15 | Data Input/Output |
| I/O4 | 16 | 19 | 16 | 16 | Data Input/Output |
| I/O5 | 17 | 20 | 17 | 17 | Data Input/Output |
| I/O6 | 18 | 21 | 18 | 18 | Data Input/Output |
| I/O7 | 19 | 22 | 19 | 19 | Data Input/Output |
| \overline{CE} | 20 | 23 | 20 | 20 | Chip Enable |
| A10 | 21 | 24 | 21 | 21 | Address |
| \overline{OE} | 22 | 25 | 22 | 22 | Output Enable |
| NC | — | 26 | — | — | No Connect |
| A11 | 23 | 27 | 23 | 23 | Address |
| A9 | 24 | 28 | 24 | 24 | Address |
| A8 | 25 | 29 | 25 | 25 | Address |
| A13 | 26 | 30 | 26 | 26 | Address |
| \overline{WE} | 27 | 31 | 27 | 27 | Write Enable |
| V _{CC} | 28 | 32 | 28 | 28 | Device Power Supply |

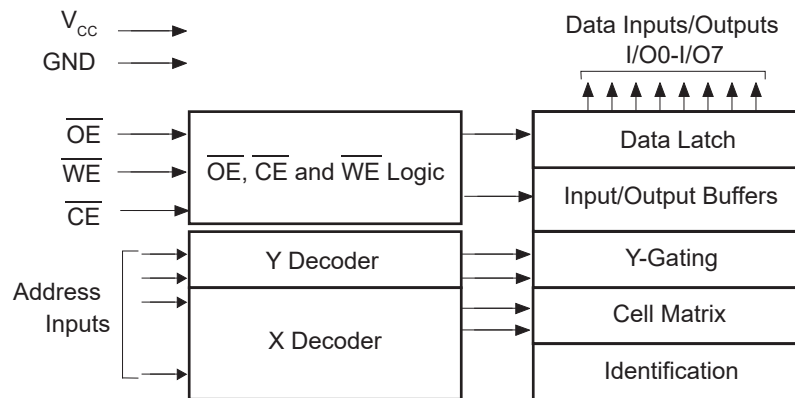
3. Description

The AT28HC256 is a high-performance Electrically Erasable and Programmable Read-Only Memory (EEPROM). Its 256-Kb memory is organized as 32,768 words by 8 bits. Manufactured with Microchip's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 5 mA.

The AT28HC256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The AT28HC256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

3.1 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

| | |
|---|--------------------------|
| Temperature under bias | -55°C to +125°C |
| Storage temperature | -65°C to +150°C |
| All input voltages (including NC pins) with respect to ground | -0.6V to +6.25V |
| All output voltages with respect to ground | -0.6V to $V_{CC} + 0.6V$ |
| Voltage on \overline{OE} and A9 with respect to ground | -0.6V to +13.5V |

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

| | | AT28HC256-90 | AT28HC256-12 |
|------------------------------|----------|-----------------|-----------------|
| Operating Temperature (Case) | Military | -55°C to +125°C | -55°C to +125°C |
| V_{CC} Power Supply | | 5V \pm 10% | 5V \pm 10% |

4.3 DC Characteristics

Table 4-2. DC Characteristics

| Parameter | Symbol | Minimum | Maximum | Units | Test Conditions |
|-------------------------------|-----------|---------|---------|---------|---|
| Input Load Current | I_{LI} | — | 10 | μA | $V_{IN} = 0V$ to $V_{CC} + 1V$ |
| Output Leakage Current | I_{LO} | — | 10 | μA | $V_{I/O} = 0V$ to V_{CC} |
| V_{CC} Standby Current TTL | I_{SB1} | — | 3 | mA | $\overline{CE} = 2.0V$ to $V_{CC} + 1V$ |
| V_{CC} Standby Current CMOS | I_{SB2} | — | 300 | μA | $\overline{CE} = V_{CC} - 0.3V$ to V_{CC} |
| V_{CC} Active Current | I_{CC} | — | 80 | mA | $f = 5$ MHz; $I_{OUT} = 0$ mA |
| Input Low Voltage | V_{IL} | — | 0.8 | V | |
| Input High Voltage | V_{IH} | 2.0 | — | V | |
| Output Low Voltage | V_{OL} | — | 0.45 | V | $I_{OL} = 6.0$ mA |
| Output High Voltage | V_{OH1} | 2.4 | — | V | $I_{OH} = -4$ mA |

4.4 Pin Capacitance

Table 4-3. Pin Capacitance^(1,2)

| Symbol | Typical | Maximum | Units | Conditions |
|-----------|---------|---------|-------|----------------|
| C_{IN} | 4 | 6 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0V$ |

Note:

1. This parameter is characterized but is not 100% tested in production.
2. $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$

5. Normalized I_{CC} Graphics

Figure 5-1. Normalized Supply Current vs. Temperature

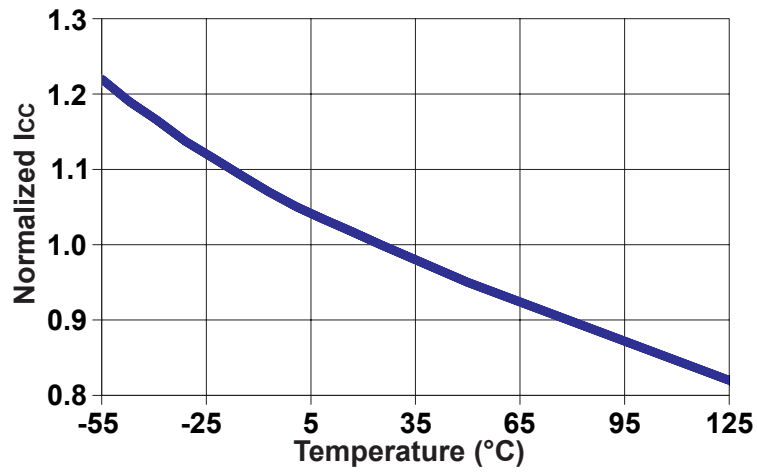


Figure 5-2. Normalized Supply Current vs. Address Frequency

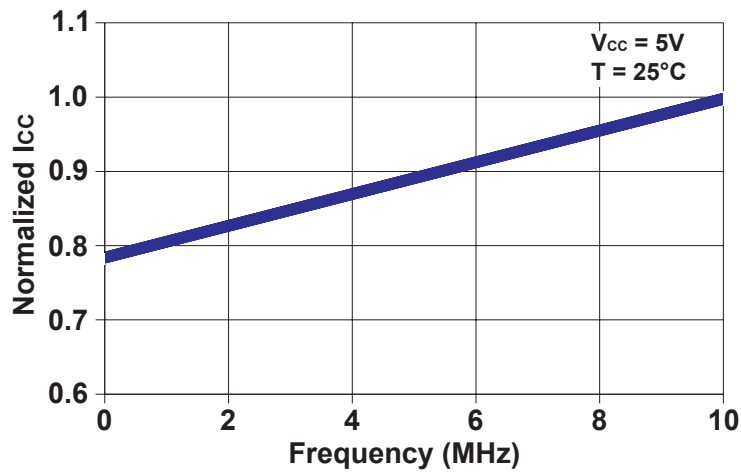
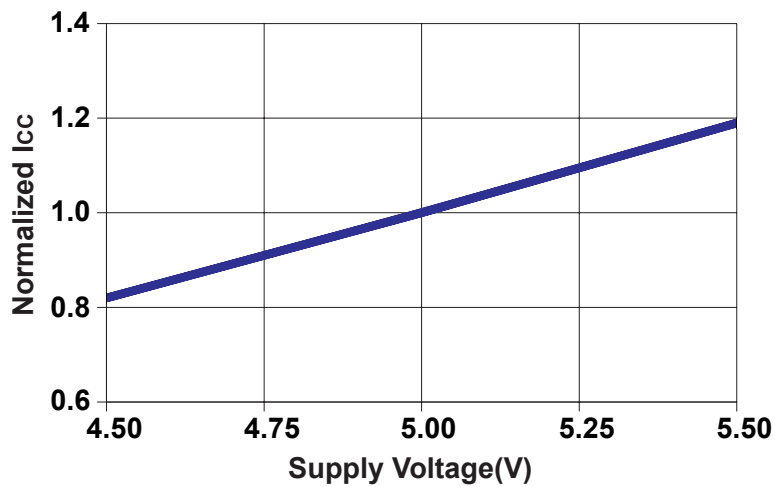


Figure 5-3. Normalized Supply Current vs. Supply Voltage



6. Device Operation

READ: The AT28HC256 is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high initiates a write cycle. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Once a byte write is started, it will automatically time itself to completion. Once a programming operation is initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 μ s (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28HC256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6-A14 inputs. For each \overline{WE} high-to-low transition during the page write operation, A6-A14 must be the same. The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28HC256 features \overline{DATA} Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. \overline{DATA} Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to \overline{DATA} Polling, the AT28HC256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Microchip incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256 in the following ways:

- V_{CC} sense – if V_{CC} is below 3.8V (typical), the write function is inhibited
- V_{CC} power-on delay – once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write
- write inhibit – holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits write cycles
- noise filter – pulses of less than 15 ns (typical) on the \overline{WE} or \overline{CE} inputs will not initiate a write cycle

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28HC256. When enabled, the software data protection (SDP) will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC256 is shipped with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} , the entire AT28HC256 will be protected against inadvertent write operations. It should be noted that, once protected, the host may still perform a byte or page write to the AT28HC256. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28HC256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC} , read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to $12V \pm 0.5V$ and using address locations 7FC0H to 7FFFH, the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. See Software Chip Erase application note for details.

6.1 Operating Modes

Table 6-1. Operating Modes

| Mode | \overline{CE} | \overline{OE} | WE | I/O |
|-----------------------|-----------------|----------------------|----------|-----------|
| Read | V_{IL} | V_{IL} | V_{IH} | D_{OUT} |
| Write ⁽¹⁾ | V_{IL} | V_{IH} | V_{IL} | D_{IN} |
| Standby/Write Inhibit | V_{IH} | X ⁽²⁾ | X | High-Z |
| Write Inhibit | X | X | V_{IH} | |
| Write Inhibit | X | V_{IL} | X | |
| Output Disable | X | V_{IH} | X | High-Z |
| Chip Erase | V_{IL} | V_H ⁽³⁾ | V_{IL} | High-Z |

Note:

1. Refer to AC Programming Waveforms.
2. X can be V_{IL} or V_H .
3. $V_H = 12.0V \pm 0.5V$

6.2 AC Read Characteristics

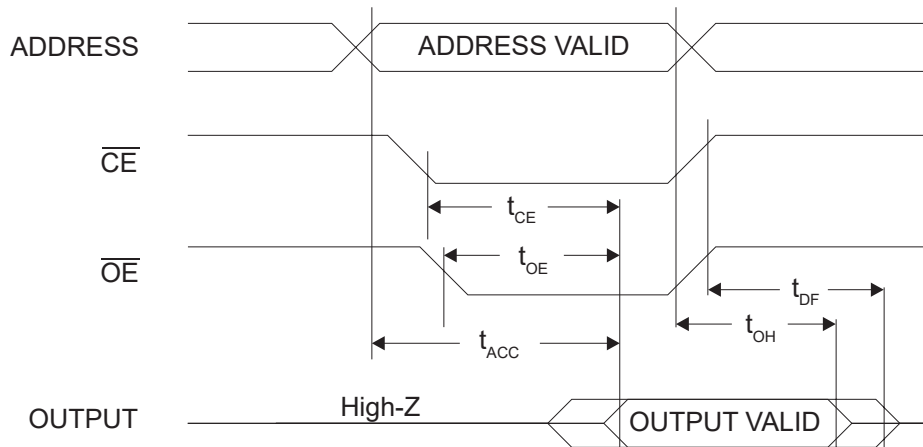
Table 6-2. AC Read Characteristics

| Parameter | Symbol | AT28HC256-90 | | AT28HC256-12 | | Units |
|--|---------------------------|--------------|------|--------------|------|-------|
| | | Min. | Max. | Min. | Max. | |
| Address to Output Delay | t_{ACC} | — | 90 | — | 120 | ns |
| \overline{CE} to Output Delay | t_{CE} ⁽¹⁾ | — | 90 | — | 120 | ns |
| \overline{OE} to Output Delay | t_{OE} ⁽²⁾ | 0 | 40 | 0 | 50 | ns |
| \overline{CE} or \overline{OE} to Output Float | t_{DF} ^(3,4) | 0 | 40 | 0 | 50 | ns |
| Output Hold from \overline{OE} or \overline{CE} , whichever occurred first | t_{OH} | 0 | — | 0 | — | ns |

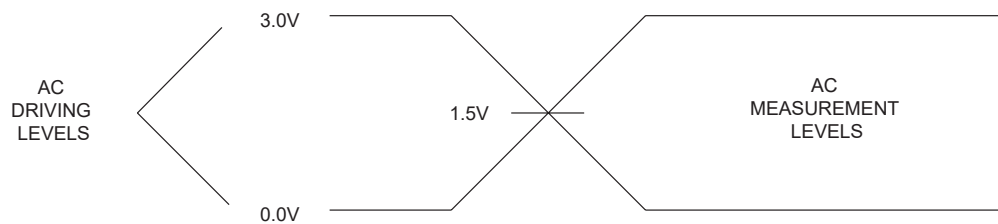
Note:

1. \overline{CE} may be delayed up to $t_{ACC}-t_{CE}$ after the address transition without impact on t_{ACC} .
2. \overline{OE} may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC}-t_{OE}$ after an address change without impact in t_{ACC} .
3. t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first ($C_L = 5\text{ pF}$).
4. This parameter is characterized and is not 100% tested.

6.3 AC Read Waveforms

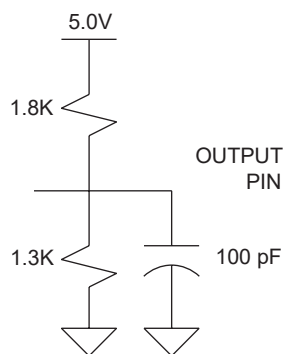


6.4 Input Test Waveforms and Measurement Level



Note: $t_R, t_F < 5$ ns.

6.5 Output Test Load



6.6 AC Write Characteristics

Table 6-3. AC Write Characteristics

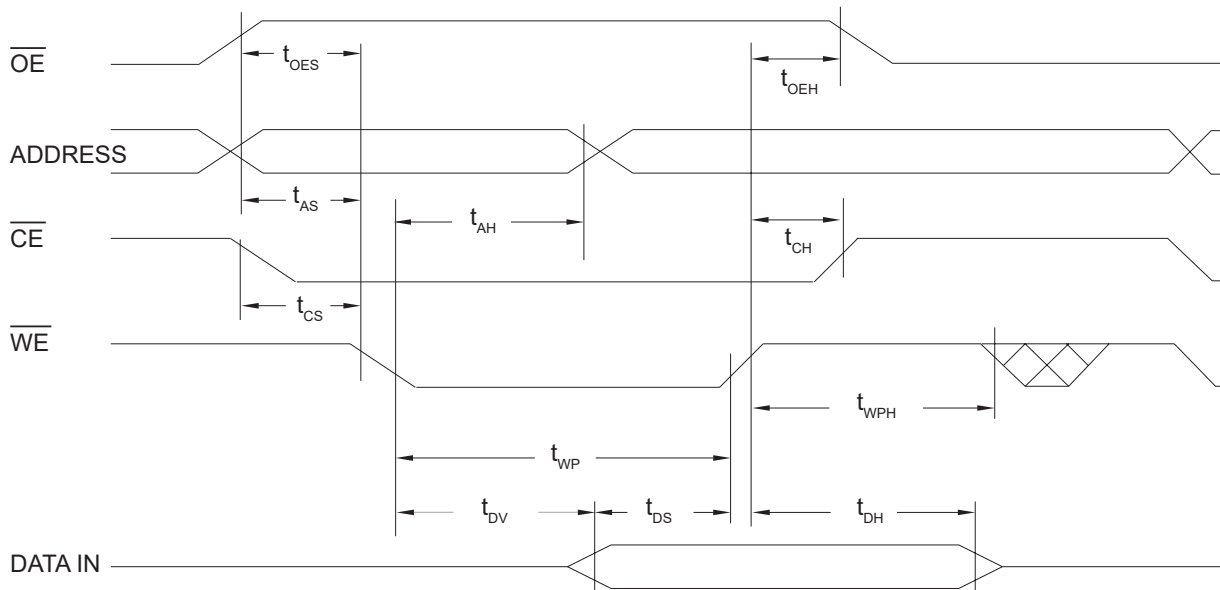
| Parameter | Symbol | Minimum | Maximum | Units |
|--|-------------------|-------------------|---------|---------|
| Address, \overline{OE} Setup Time | t_{AS}, t_{OES} | 0 | — | ns |
| Address Hold Time | t_{AH} | 50 | — | ns |
| Chip Select Setup Time | t_{CS} | 0 | — | ns |
| Chip Select Hold Time | t_{CH} | 0 | — | ns |
| Write Pulse Width (\overline{WE} or \overline{CE}) | t_{WP} | 100 | — | ns |
| Data Setup Time | t_{DS} | 50 | — | ns |
| Data, \overline{OE} Hold Time | t_{DH}, t_{OEH} | 0 | — | μ s |
| Time to Data Valid | t_{DV} | NR ⁽¹⁾ | — | |

Note:

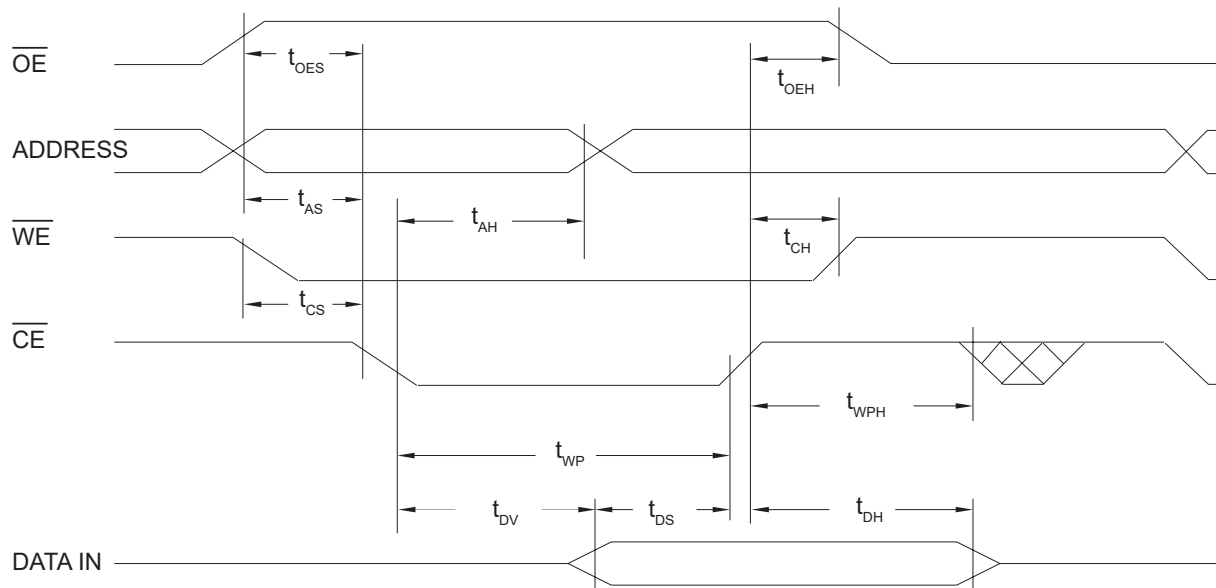
1. NR = No Restriction

6.7 AC Write Waveforms

6.7.1 \overline{WE} Controlled



6.7.2 $\overline{\text{CE}}$ Controlled

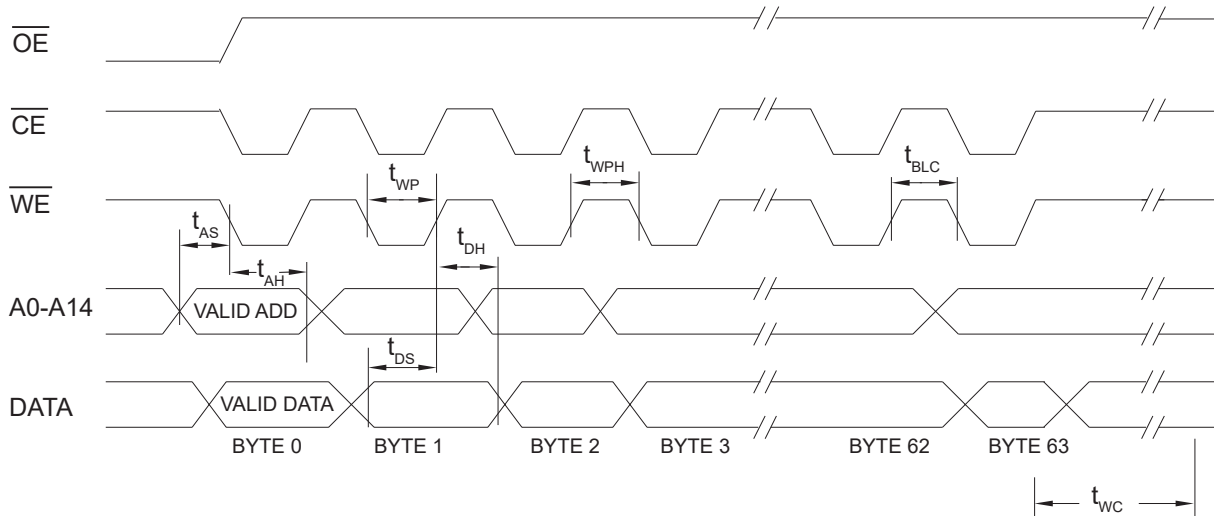


6.8 Page Mode Characteristics

Table 6-4. Page Mode Characteristics

| Parameter | Symbol | Minimum | Maximum | Units |
|------------------------|------------------|---------|---------|---------------|
| Write Cycle Time | t_{WC} | — | 10 | ms |
| | | — | 3 | ms |
| Address Setup Time | t_{AS} | 0 | — | ms |
| Address Hold Time | t_{AH} | 50 | — | ns |
| Data Setup Time | t_{DS} | 50 | — | ns |
| Data Hold Time | t_{DH} | 0 | — | ns |
| Write Pulse Width | t_{WP} | 100 | — | ns |
| Byte Load Cycle Time | t_{BLC} | — | 150 | μs |
| Write Pulse Width High | t_{WPH} | 50 | — | ns |

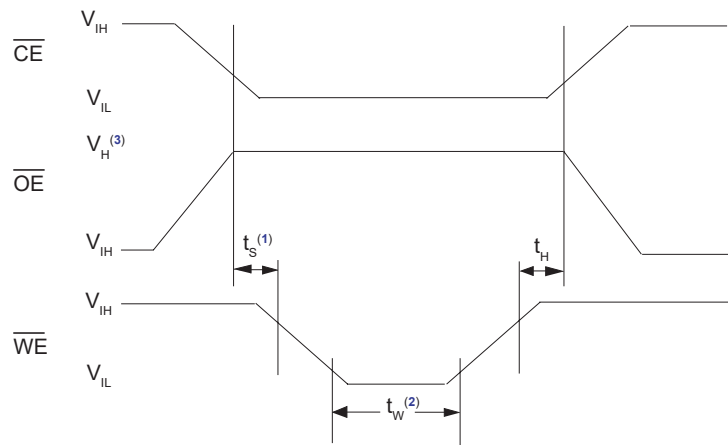
6.9 Page Mode Write Waveforms^(1,2)



Note:

1. A6 through A14 must specify the page address during each high-to-low transition of \overline{WE} (or \overline{CE}).
2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

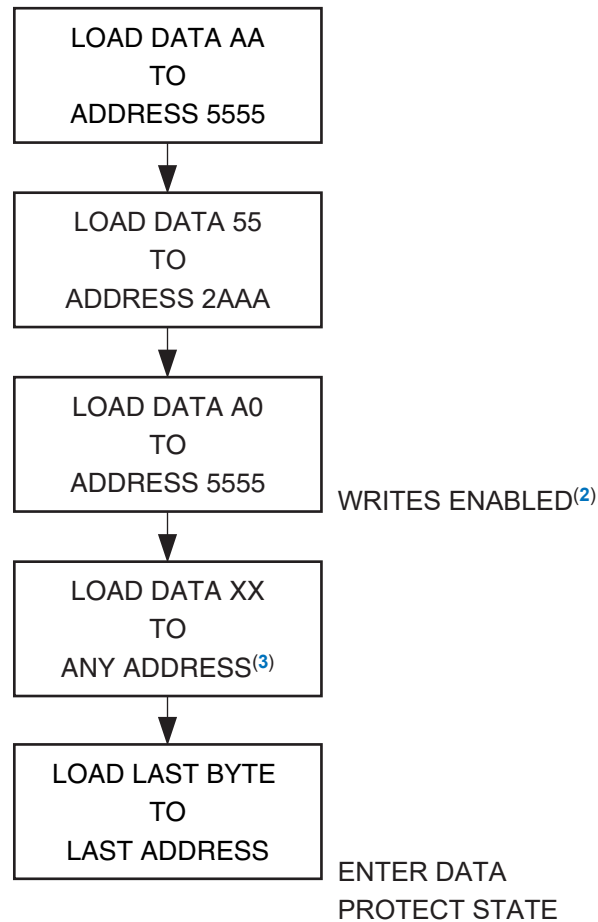
6.10 Chip Erase Waveforms



Note:

1. $t_S = t_H = 5 \mu\text{sec}$ (minimum)
2. $t_W = 10 \text{ msec}$ (minimum)
3. $V_H = 12.0\text{V} \pm 0.5\text{V}$

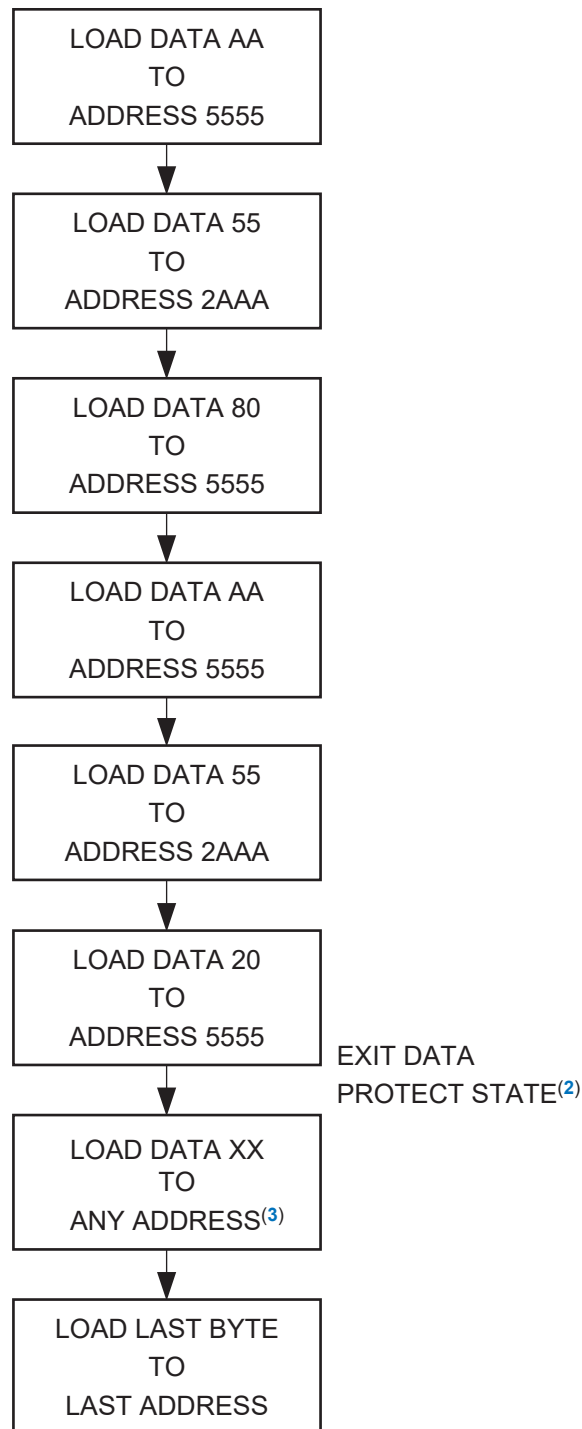
6.11 Software Data Protection Enable Algorithm⁽¹⁾



Note:

1. Data format: I/O7-I/O0 (Hex); Address format: A14-A0 (Hex).
2. Write-Protect state will be activated at end of write even if no other data is loaded.
3. 1 to 64 bytes of data are loaded.

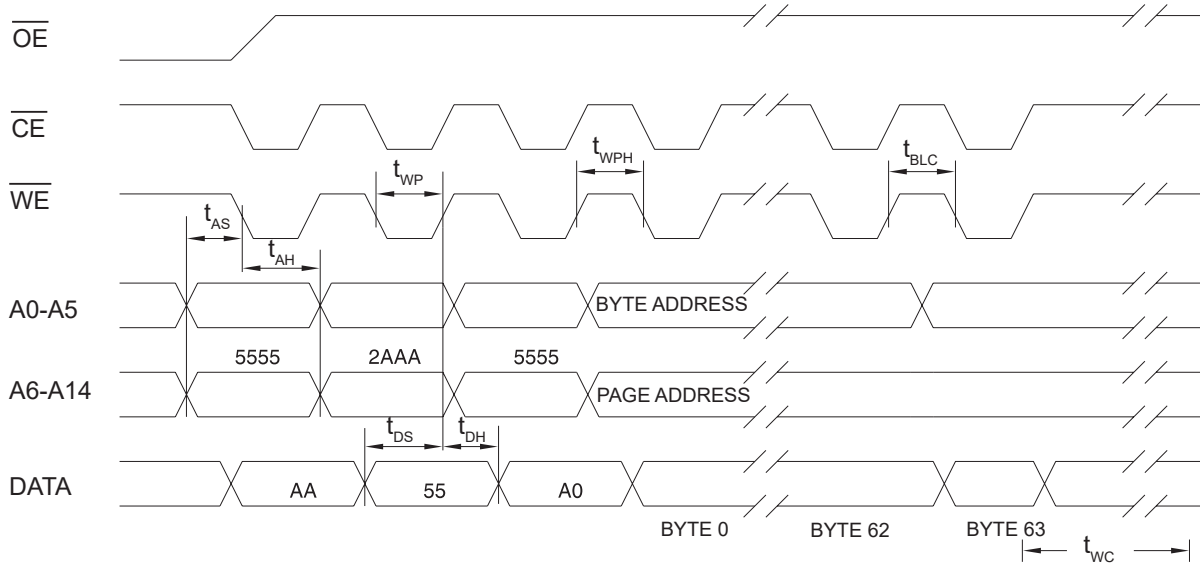
6.12 Software Data Protection Disable Algorithm⁽¹⁾



Note:

1. Data format: I/O7-I/O0 (Hex); Address format: A14-A0 (Hex).
2. Write-Protect state will be deactivated at end of write period even if no other data is loaded.
3. 1 to 64 bytes of data are loaded.

6.13 Software Protected Program Cycle Waveform^(1,2)



Note:

1. A6-A14 must specify the same page address during each high-to-low transition of \overline{WE} (or \overline{CE}) after the software code has been entered.
2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

6.14 Data Polling Characteristics⁽¹⁾

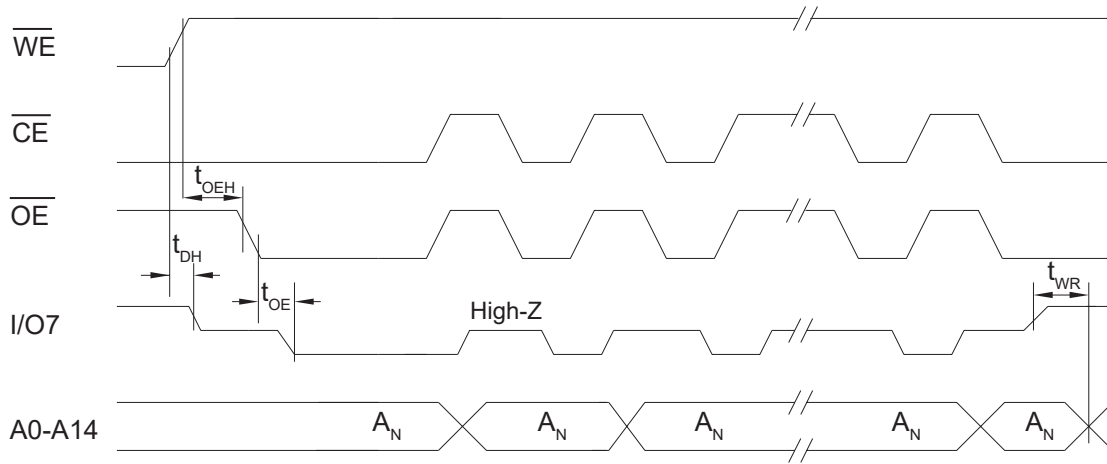
Table 6-5. Data Polling Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--|------------|---------|---------|---------|-------|
| Data Hold Time | t_{DH} | 0 | — | — | ns |
| \overline{OE} Hold Time | $t_{OE H}$ | 0 | — | — | ns |
| \overline{OE} to Output Delay ⁽²⁾ | t_{OE} | — | — | — | ns |
| Write Recovery Time | t_{WR} | 0 | — | — | ns |

Note:

1. These parameters are characterized and not 100% tested.
2. See [AC Read Characteristics](#).

6.15 Data Polling Waveforms



6.16 Toggle Bit Characteristics⁽¹⁾

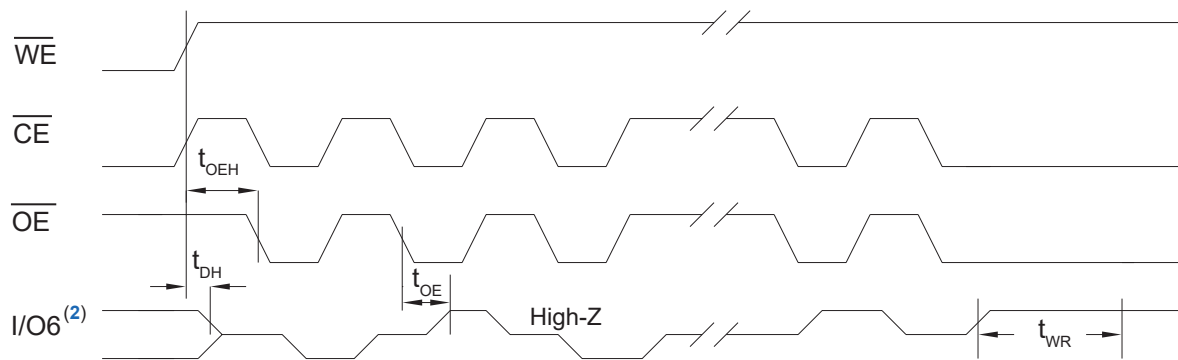
Table 6-6. Toggle Bit Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--|------------|---------|---------|---------|-------|
| Data Hold Time | t_{DH} | 10 | — | — | ns |
| \overline{OE} Hold Time | t_{OEH} | 10 | — | — | ns |
| \overline{OE} to Output Delay ⁽²⁾ | t_{OE} | — | — | — | ns |
| \overline{OE} High Pulse ⁽²⁾ | t_{OEHP} | 150 | — | — | ns |
| Write Recovery Time | t_{WR} | 0 | — | — | ns |

Note:

1. These parameters are characterized and not 100% tested.
2. See [AC Read Characteristics](#).

6.17 Toggle Bit Waveforms

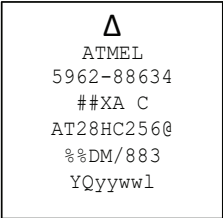
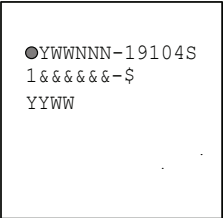
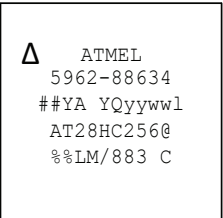
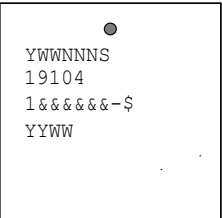
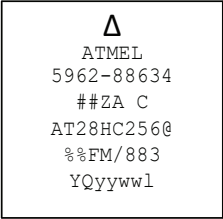
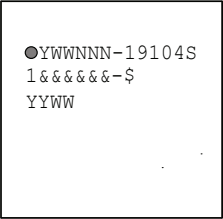
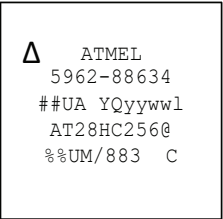
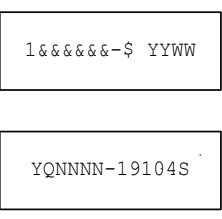


Note:

1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

7. Packaging Information

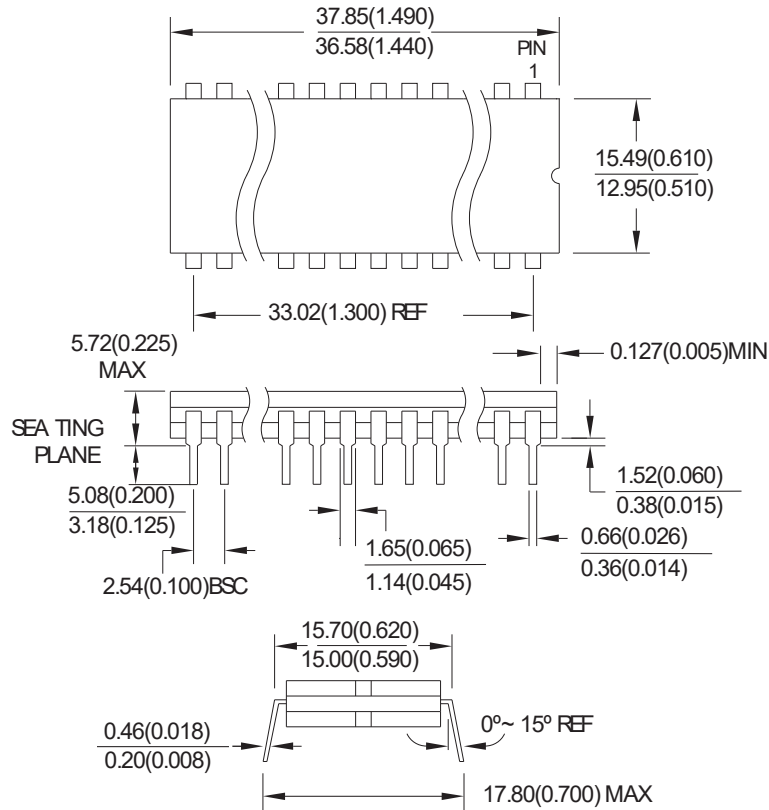
7.1 Package Marking Information

| AT28HC256: Package Marking Information (SMD devices) | | | |
|---|--|--|---|
| 28-pin CERDIP | | 32-pad CLCC | |
| Topside | Backside | Topside | Backside |
|  <p style="text-align: center;"> Δ ATMEL 5962-88634 ##XA C AT28HC256@ %%DM/883 YQyyw1 </p> |  <p style="text-align: center;"> ●YWWNNN-19104S 1&&&&&- YYWW </p> |  <p style="text-align: center;"> Δ ATMEL 5962-88634 ##YA YQyyw1 AT28HC256@ %%LM/883 C </p> |  <p style="text-align: center;"> ● YWWNNNS 19104 1&&&&&- YYWW </p> |
| 28-lead FLATPACK | | 30-pin PGA | |
| Topside | Backside | Topside | Edges |
|  <p style="text-align: center;"> Δ ATMEL 5962-88634 ##ZA C AT28HC256@ %%FM/883 YQyyw1 </p> |  <p style="text-align: center;"> ●YWWNNN-19104S 1&&&&&- YYWW </p> |  <p style="text-align: center;"> Δ ATMEL 5962-88634 ##UA YQyyw1 AT28HC256@ %%UM/883 C </p> |  <p style="text-align: center;"> 1&&&&&- YYWW YQNNNN-19104S </p> |
| ## = SMD Device | %% = Access Time | @ = Write Endurance Rating | \$ = Assembly Location |
| 03: 90ns, 10ms TWC 01: 120ns, 10ms TWC 04: 90ns, 3ms TWC 02: 120ns, 3ms TWC | 90: 90 ns 12: 120 ns | Blank: Standard (10K at 10ms) E: Extended (100K at 10ms) F: Fast Write (10k at 3ms) | F: Philippines N: Thailand |
| Country of Assembly | | Lot Trace Code | Seal Year and Work Week |
| &&&&&: Country of Assembly | | YWWNNN: Lot Trace Code | YYWW: Seal Year and Work Week |
| Year, Quarter, Seal Year, Seal Week and Group D Coverage (Military Date Code) | | | |
| YQyyw1: Year, Quarter, Seal Year, Seal Week and Group D Coverage (Military Date Code) | | | |

AT28HC256

Packaging Information

Dimensions in Millimeters and (Inches).
 Controlling dimension: Inches.
 MIL-STD 1835 D-10 Config A (Glass Sealed)



10/23/03

| TITLE | DRAWING NO. | REV. |
|--|-------------|------|
| 28D6, 28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip) | 28D6 | B |

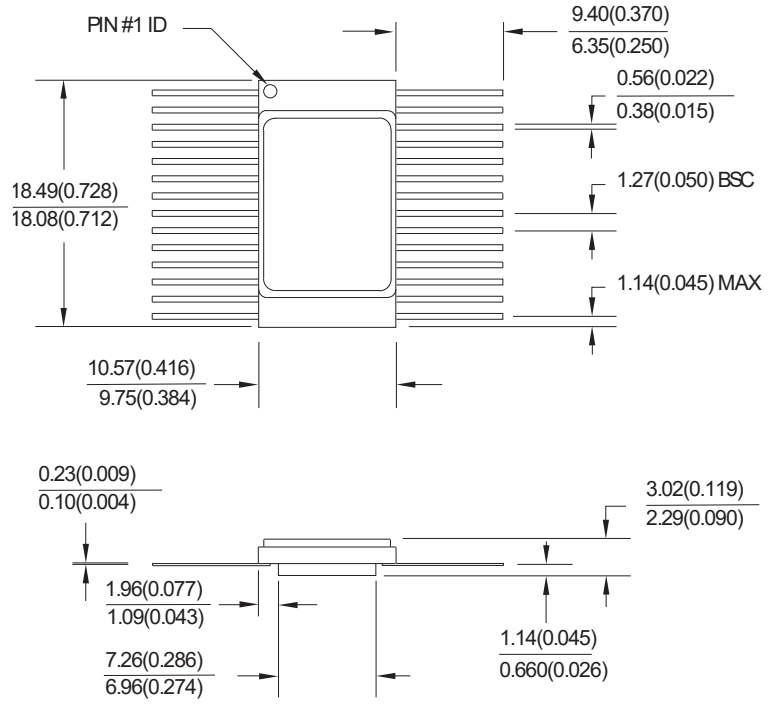
Note:

For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

AT28HC256

Packaging Information

Dimensions in Millimeters and (Inches).
 Controlling dimension: Inches.
 MIL-STD 1835 F-12 Config B



10/21/03

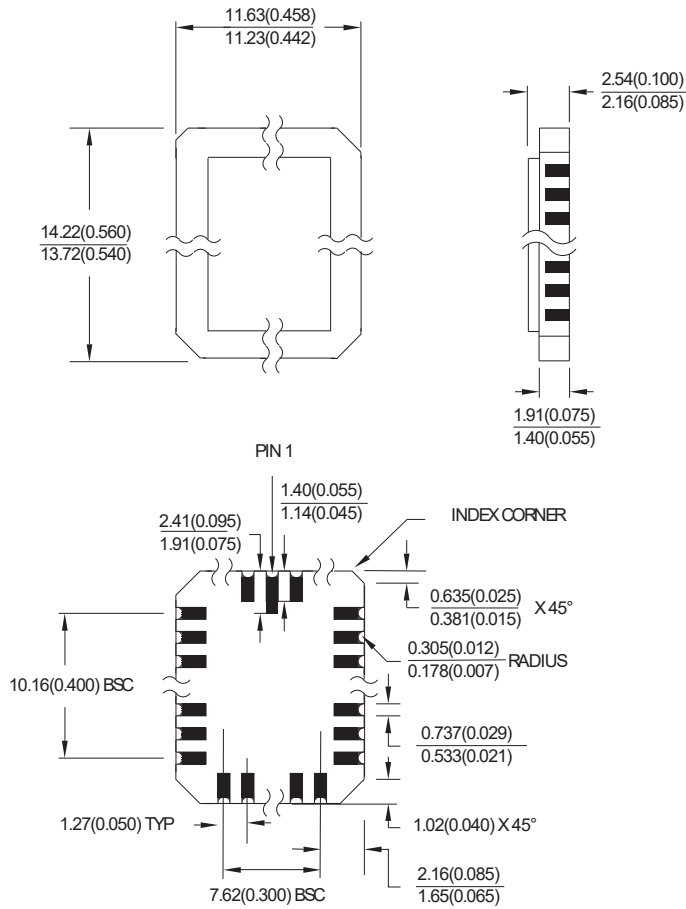
| | | | |
|--|---|---------------------------|------------------|
| | TITLE 28F, 28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (FlatPack) | DRAWING NO. 28F | REV. B |
|--|---|---------------------------|------------------|

Note:
 For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

AT28HC256

Packaging Information

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 C-12



10/21/03

| TITLE | DRAWING NO. | REV. |
|---|-------------|------|
| 32L, 32-pad, Non-windowed, Ceramic Lid, Leadless Chip Carrier (LCC) | 32L | B |

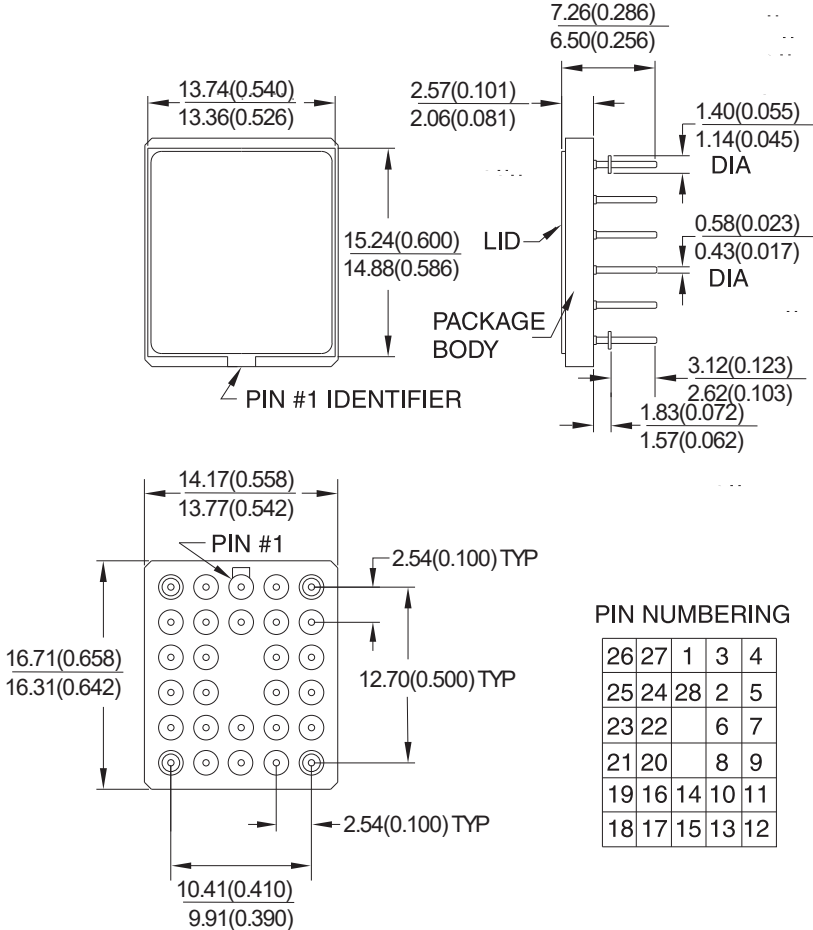
Note:

For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

AT28HC256

Packaging Information

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.



PIN NUMBERING

| | | | | |
|----|----|----|----|----|
| 26 | 27 | 1 | 3 | 4 |
| 25 | 24 | 28 | 2 | 5 |
| 23 | 22 | | 6 | 7 |
| 21 | 20 | | 8 | 9 |
| 19 | 16 | 14 | 10 | 11 |
| 18 | 17 | 15 | 13 | 12 |

10/21/03

| | | | |
|--|---|---------------------------|------------------|
| | TITLE 28U, 28-pin, Ceramic Pin Grid Array (PGA) | DRAWING NO. 28U | REV. B |
|--|---|---------------------------|------------------|

Note:
For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

8. Revision History

Revision A (April 2020)

Updated to the Microchip template. Microchip DS20006352 replaces Atmel document 0006. Added updated Part Markings to include new trace code format.

Atmel Document 0006 Revision M (December 2009)

Updated AC Characteristics and ordering information.

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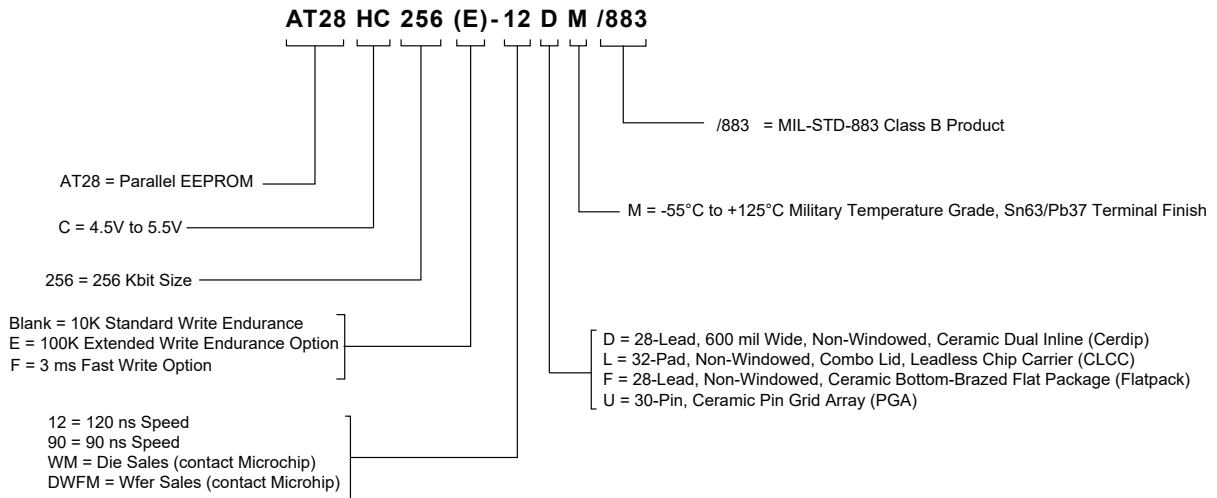
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

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Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples

Table 12-1. AT28HC256 Ordering Information

| Ordering Code | Standard Military Drawing Number (SMD#) | Package Number | t _{ACC} (ns) | Operating Range |
|--------------------|---|----------------|-----------------------|---|
| AT28HC256-90DM/883 | 5962-88634 03 XA | 28D6 | 90 | Military/883C Class B, Fully Compliant (-55°C to 125°C) |
| AT28HC256-90FM/883 | 5962-88634 03 ZA | 28F | | |
| AT28HC256-90LM/883 | 5962-88634 03 YA | 32L | | |
| AT28HC256-90UM/883 | 5962-88634 03 UA | 28U | | |
| AT28HC256-12DM/883 | 5962-88634 01 XA | 28D6 | 120 | |
| AT28HC256-12FM/883 | 5962-88634 01 ZA | 28F | | |
| AT28HC256-12LM/883 | 5962-88634 01 YA | 32L | | |
| AT28HC256-12UM/883 | 5962-88634 01 UA | 28U | | |

Table 12-2. AT28HC256E Ordering Information (Not Dual Marked Packages)

| Ordering Code | Standard Military Drawing Number (SMD#) | Package Number | t _{ACC} (ns) | Operating Range |
|---------------------|---|----------------|-----------------------|---|
| AT28HC256E-90DM/883 | N/A | 28D6 | 90 | Military/883C Class B, Fully Compliant (-55°C to 125°C) |
| AT28HC256E-90FM/883 | N/A | 28F | | |
| AT28HC256E-90LM/883 | N/A | 32L | | |
| AT28HC256E-90UM/883 | N/A | 28U | | |
| AT28HC256E-12DM/883 | N/A | 28D6 | 120 | |
| AT28HC256E-12FM/883 | N/A | 28F | | |
| AT28HC256E-12LM/883 | N/A | 32L | | |
| AT28HC256E-12UM/883 | N/A | 28U | | |

Table 12-3. AT28HC256F Ordering Information

| Ordering Code | Standard Military Drawing Number (SMD#) | Package Number | t _{ACC} (ns) | Operating Range |
|---------------------|---|----------------|-----------------------|---|
| AT28HC256F-90DM/883 | 5962-88634 04 XA | 28D6 | 90 | Military/883C Class B, Fully Compliant (-55°C to 125°C) |
| AT28HC256F-90FM/883 | 5962-88634 04 ZA | 28F | | |
| AT28HC256F-90LM/883 | 5962-88634 04 YA | 32L | | |
| AT28HC256F-90UM/883 | 5962-88634 04 UA | 28U | | |
| AT28HC256F-12DM/883 | 5962-88634 02 XA | 28D6 | 120 | |
| AT28HC256F-12FM/883 | 5962-88634 02 ZA | 28F | | |
| AT28HC256F-12LM/883 | 5962-88634 02 YA | 32L | | |
| AT28HC256F-12UM/883 | 5962-88634 02 UA | 28U | | |

Package Types

| | |
|------|--|
| 28D6 | 28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline (Cerdip) |
| 28F | 28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack) |
| 32L | 32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC) |
| 28U | 28-Pin, Ceramic Pin Grid Array (PGA) |
| WM | Diced Die Military |
| DWFM | Die in Wafer Form Military |

Options

| | |
|-------|---|
| Blank | Standard Device: Endurance = 10K Write Cycles; Write Time 10 ms |
| E | High Endurance Option: Endurance = 100K Write Cycles |
| F | Fast Write Option: Write Time = 3 ms |

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