MAX20084

Automotive Dual-Antenna Power Supply with I²C Serial Interface

General Description

The MAX20084 is a dual-antenna power supply with I²C interface for diagnostics and control. The dual 270mA antenna supplies are linear regulators whose output voltage is set individually through I²C. Additionally, internal registers are used to set current limit, open-load threshold, and other parameters.

An internal 8-bit ADC allows the channel current to be measured. The AOUT analog output can also be used with an external ADC to measure the output current on either channel.

The MAX20084 is available in two variants: the MAX20084ATEA/VY+ with both channels turned off by default after power-up, and the MAX20084ATEB/VY+ with channel 1 turned on by default after power-up.

The MAX20084 is available in a 4mm x 4mm, optional side-wettable TQFN package and operates over the -40 to +125°C temperature range.

Applications

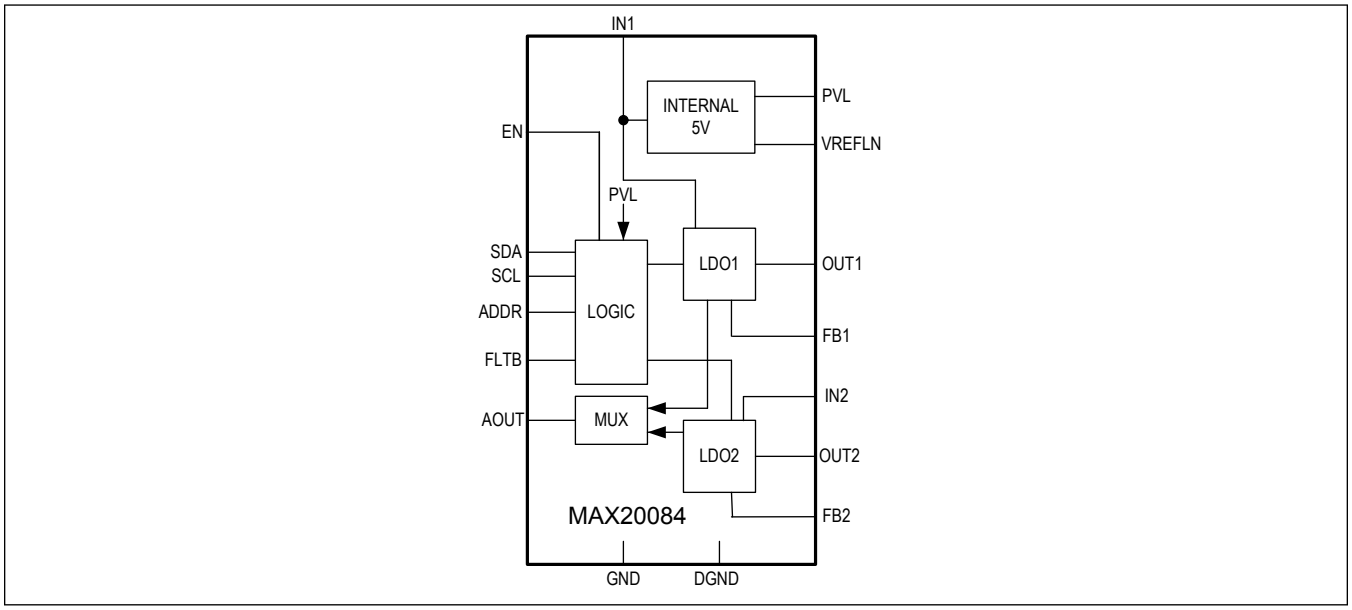
- Remote LNA Phantom Power
- Automotive Camera and Sensor Power
- Automotive Microphone Power

Benefits and Features

- Wide Input Voltage Range: 4.5V to 28V (40V Load Dump Tolerant)
- High Integration
  - Complete 2-Channel Solution with Linear Regulators and Diagnostics
  - I²C Control for Minimum Parts Count
- Complete and Flexible Control
  - Regulator Output Voltage
  - Regulator Current Limit
  - Regulator Overcurrent Level
  - Individual Disable/Enable
- Detailed Diagnostics
  - Output Current
  - Short-to-Ground/Battery
  - Overtemperature Warning
  - Thermal Shutdown
- Compact, 4mm x 4mm, 16 TQFN, Optional Side-Wettable Package

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



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Absolute Maximum Ratings

IN1, EN to GND ..... -0.3V to +40V
IN1 to IN2 ..... -0.3V to +0.3V
OUT1, OUT2, FB1, FB2 to GND ..... -0.3V to +26V
DGND to GND ..... -0.3V to +0.3V
AOUT, VREFLN, ADDR to GND ..... -0.3V to V_{PVL} + 0.3V
PVL, FLTB, SDA, SCL to GND ..... -0.3V to +6V

Continuous Power Dissipation Multilayer Board (T_A = +70°C) ..... +2W
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SW-TQFN

Package Code	T1644Y-4C
Outline Number	21-100204
Land Pattern Number	90-0070
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	59.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	40°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W

TQFN

Package Code	T1644-4C
Outline Number	21-0139
Land Pattern Number	90-0070
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	59.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	40°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN1} = V_{IN2} = 12V, T_A = T_J = -40°C to +125°C, EN = high, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT						
Input Voltage Range	V_{IN}		4.5		28	V
		Outputs disabled, maximum 1s			40	
IN1 Undervoltage Lockout Rising	V_{UVLOR}			4.15	4.45	V
IN1 Undervoltage Lockout Falling	V_{UVLOF}			3.7	4	V
Quiescent Supply Current	I_Q	LDOs enabled, no load, V_{OUT} = 8V		3.1	4.1	mA
		LDOs disabled		1.2	1.8	
Standby Supply Current	I_{SD}	EN = 0		0.1	1	µA
PVL REGULATOR						
PVL Output Voltage				5		V
PVL Undervoltage Lockout, Rising			4.05		4.35	V
PVL Undervoltage Lockout, Falling			3.9		4.2	V
OUT1/2 REGULATORS						
OUT_ Voltage	$V_{OUT\_}$	8.5V setting, 1mA < $I_{OUT\_}$ < 250mA	8.287	8.5	8.713	V
		8.5V setting, $I_{OUT\_}$ = 100mA	8.33	8.5	8.67	
OUT1 On-Resistance		I_{OUT1} = 100mA, V_{OUT1} = 5V		1.7	4	Ω
OUT2 On-Resistance		I_{OUT2} = 100mA, V_{OUT2} = 5V		2.8	6.6	Ω
OUT_ Voltage Range		Linear regulator mode	3.3		12	V
Power-Supply Rejection Ratio		V_{RIPPLE} = $1V_{P-P}$, f = 100Hz, $I_{OUT\_}$ = 10mA, $V_{OUT\_}$ = 8.5V (Note 2)		73		dB
Output Voltage Noise		10Hz to 100kHz, 100mA load current, $V_{OUT\_}$ = 8.5V, C_{OUT} = 10µF (Note 2)		85		$µV_{RMS}$
CURRENT SENSE						
OUT_ Current to AOUT Ratio		20mA < $I_{OUT\_}$ < 250mA	9	10	11	mV/mA
		6mA < $I_{OUT\_}$ < 20mA	7	10	13	
ADC Resolution				8		Bits
ADC Current Measurement 1-LSB Step Size		Read through I²C, 50mA < $I_{OUT\_}$ < 250mA	0.9	1	1.1	mA/bit
ADC Current Measurement 1-LSB Step Size, Low-Current Range		Read through I²C, 6mA < $I_{OUT\_}$ < 50mA	0.18	0.2	0.22	mA/bit
		Read through I²C, 3mA < $I_{OUT\_}$ < 6mA	0.17	0.2	0.23	
DIAGNOSTICS						
ILIM Current Limit	I_{LIM}	ILIM[4:0] = 00010	95	100	105	mA
IOC Threshold	I_{OC}	IOC[4:0] = 01110	95	100	105	mA

Electrical Characteristics (continued)

(V_{IN1} = V_{IN2} = 12V, T_A = T_J = -40°C to +125°C, EN = high, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IWARN Threshold	I_{WARN}	IWARN[3:0] = 0110	75	80	85	mA
IOL Threshold	I_{OL}	IOL[2:0] = 110	8.5	10	11.5	mA
IN1 Overvoltage Lockout Rising Threshold	V_{OVLOR}	IN1 rising	19.5	20.5	21	V
IN1 Overvoltage Lockout Falling Threshold	V_{OVLOF}		18.2			V
Short-to-Battery Threshold in Off State		$V_{OUT1/2}$ - $V_{IN1/2}$, rising, checked during turn-on sequence	10	20	37.5	mV
Reverse-Current Detection Level, Switch Mode		OUT_ enabled, $V_{OUT1/2}$ - $V_{IN1/2}$, rising	0.2	0.3	0.46	V
Reverse-Current Detection Level, Regulator Mode		OUT_ enabled, $V_{OUT1/2}$ - $V_{IN1/2}$, rising	10	20	37.5	mV
Reverse-Current Shutdown Delay				9	20	µs
Reverse Current Blanking Time	$t_{BLANKREV}$	After enable		16		ms
Short-Circuit Current Blanking Time	t_{BLANK}	TBLANK_SET[1:0] = 10		100		ms
OUT_ Short to Ground Detection Falling Threshold		OUT_ falling	0.55	0.7	1.05	V
OUT_ Short to Ground Detection Rising Threshold		OUT_ rising	0.9	1	1.3	V
OVERTEMPERATURE PROTECTION						
Thermal Shutdown Temperature		(Note 2)		165		°C
Thermal Shutdown Hysteresis		(Note 2)		15		°C
Thermal Warning Temperature	T_{WARN}	TWARN_SET[1:0] = 11 (Note 2)		125		°C
INPUT/OUTPUT PINS						
EN, SCL, SDA Input Voltage Low					0.8	V
EN, SCL, SDA Input Voltage High			2			V
SCL, SDA Input Leakage Current			-1		+1	µA
EN Input Pulldown Resistor	R_{ENPD}		250	500		kΩ

Electrical Characteristics (continued)

(V_{IN1} = V_{IN2} = 12V, T_A = T_J = -40°C to +125°C, EN = high, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB_ Internal Pulldown Resistor	R_{FBPD}			100		kΩ
FLTB, SDA Low Output Voltage		I_{SINK} = 5mA			0.4	V
I²C INTERFACE						
Clock Frequency	f_{SCL}				400	kHz
Setup Time (Repeated) START	$t_{SU:STA}$		260			ns
Hold Time (Repeated) START	$t_{HD:STA}$		260			ns
SCL Low Time	t_{LOW}		350			ns
SCL High Time	t_{HIGH}		260			ns
Data Setup Time	$t_{SU:DAT}$		50			ns
Data Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU:STO}$		260			ns
Spike Suppression				50		ns

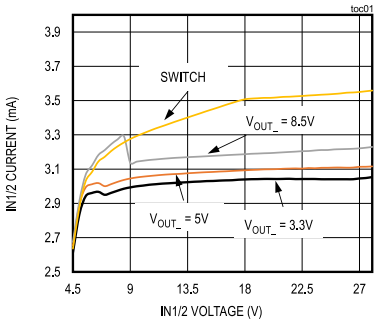
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 2: Guaranteed by design, not production tested.

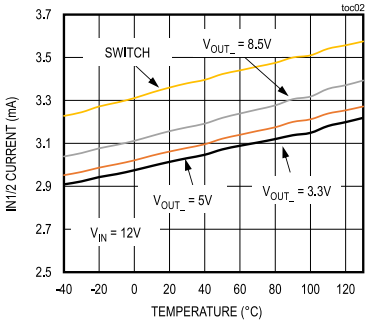
Typical Operating Characteristics

(V_{IN1} = V_{IN2} = +12V, T_A= +25°C, unless otherwise noted.)

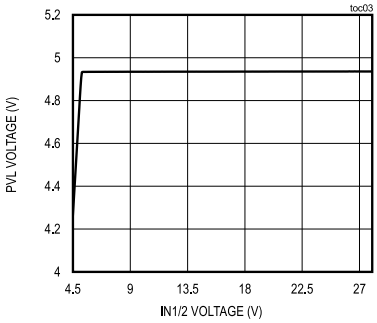
QUIESCENT SUPPLY CURRENT



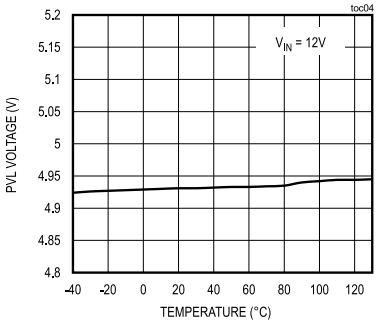
QUIESCENT SUPPLY CURRENT



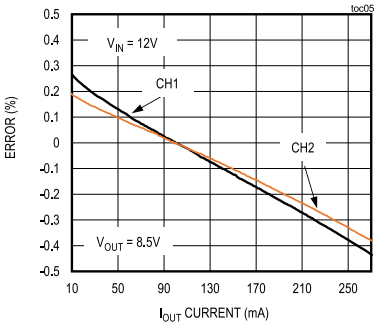
PVL REGULATOR VOLTAGE



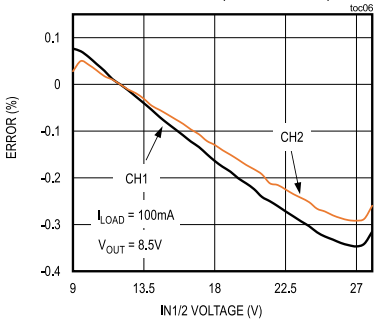
PVL REGULATOR VOLTAGE



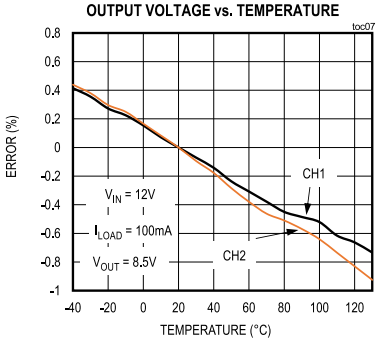
LOAD REGULATION



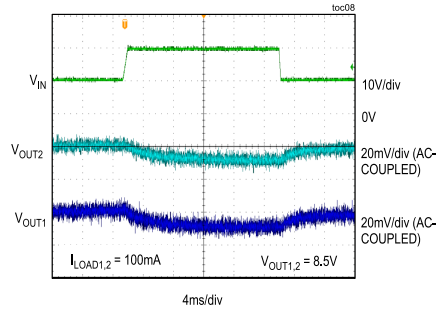
LINE REGULATION (OVP DISABLED)



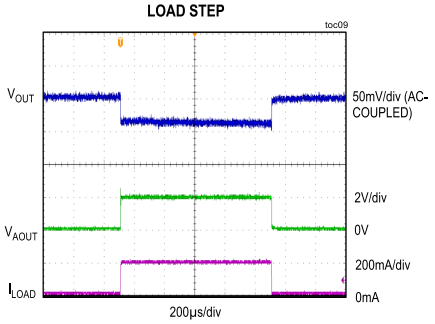
OUTPUT VOLTAGE vs. TEMPERATURE



LDO REGULATOR LINE STEP



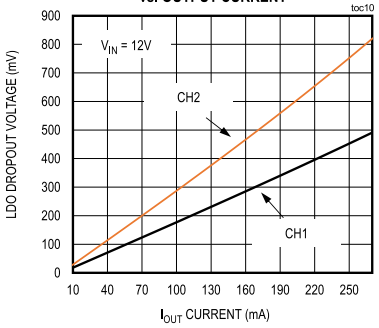
LDO REGULATOR LOAD STEP



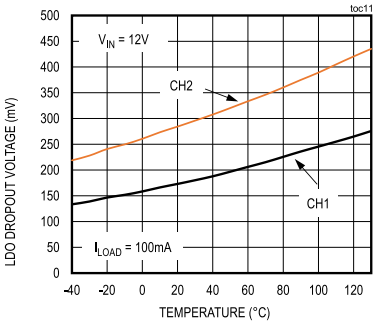
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = +12V, T_A= +25°C, unless otherwise noted.)

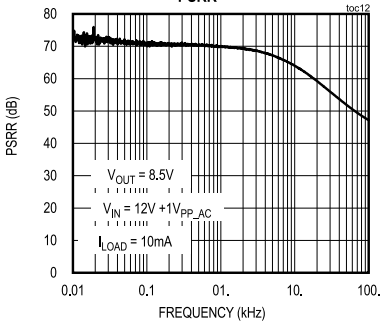
LDO DROPOUT VOLTAGE vs. OUTPUT CURRENT



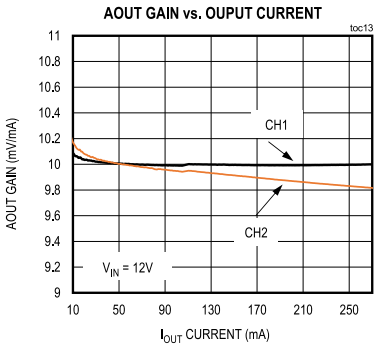
LDO DROPOUT VOLTAGE vs. TEMPERATURE



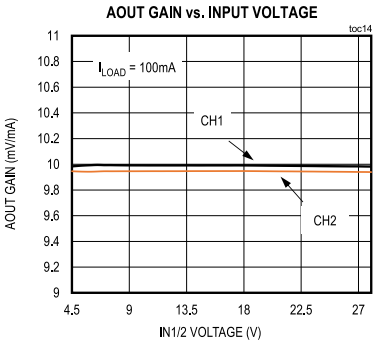
PSRR



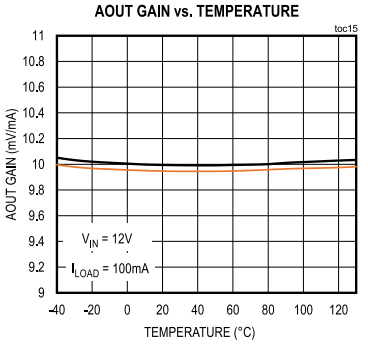
AOUT GAIN vs. OUPUT CURRENT



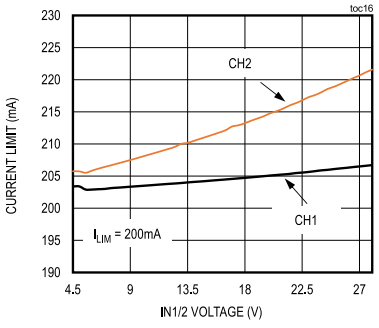
AOUT GAIN vs. INPUT VOLTAGE



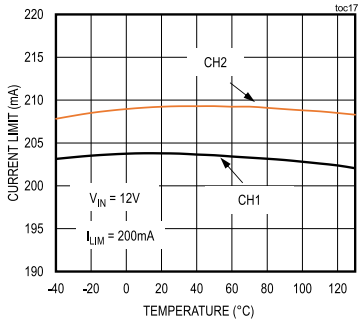
AOUT GAIN vs. TEMPERATURE



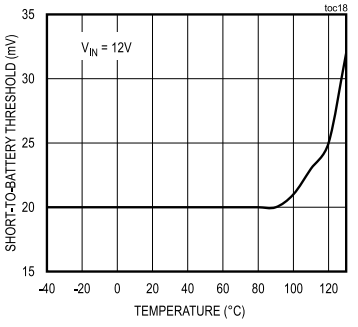
CURRENT LIMIT vs. INPUT VOLTAGE



CURRENT LIMIT vs. TEMPERATURE



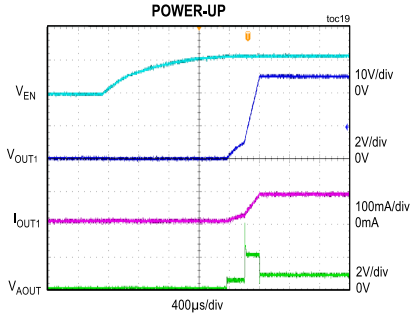
S2B THRESHOLD vs. TEMPERATURE



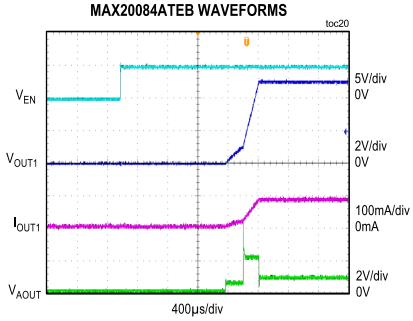
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = +12V, T_A= +25°C, unless otherwise noted.)

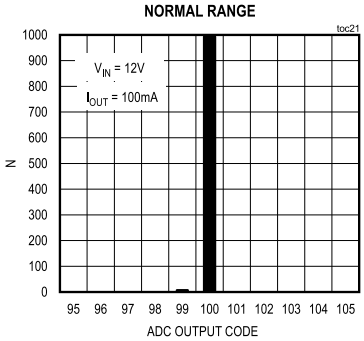
MAX20084ATEB WAVEFORMS
POWER-UP



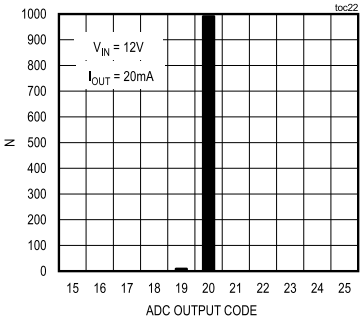
MAX20084ATEB WAVEFORMS



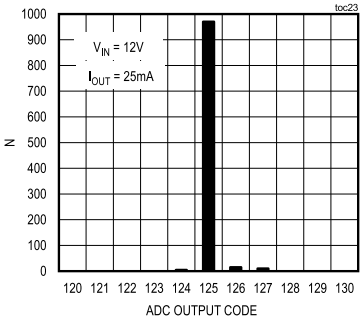
ADC NOISE HISTOGRAM
NORMAL RANGE



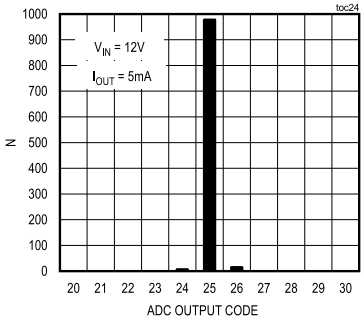
ADC NOISE HISTOGRAM
NORMAL RANGE



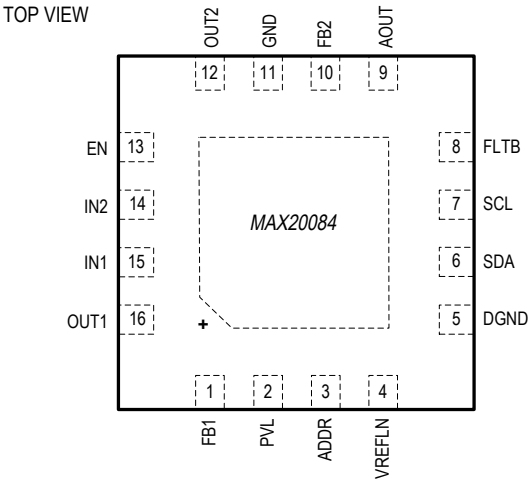
ADC NOISE HISTOGRAM
LOW RANGE



ADC NOISE HISTOGRAM
LOW RANGE



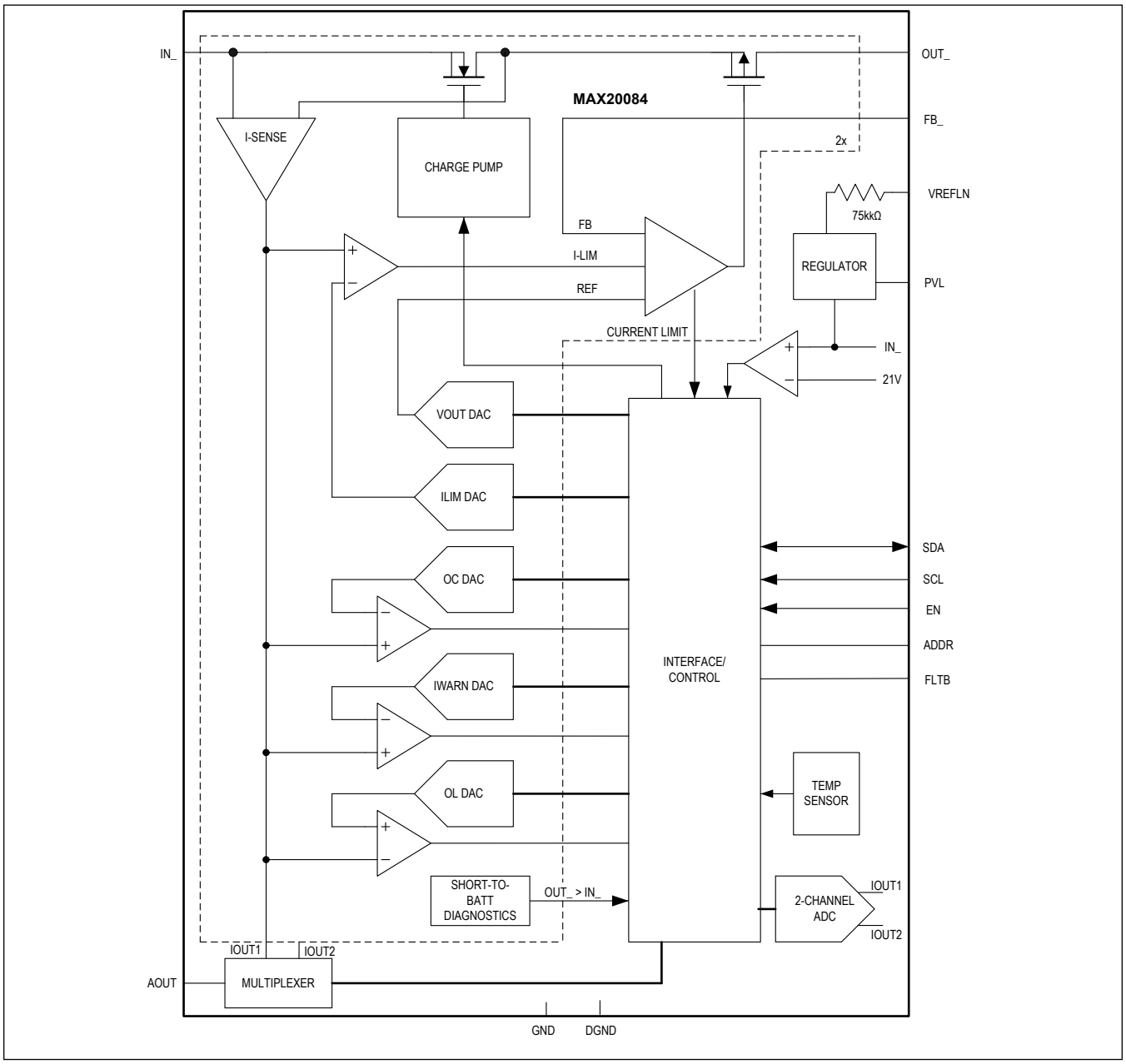
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	FB1	Feedback Connection for the OUT1 Output. Connect FB1 to OUT1.
2	PVL	5V Regulator Output. Bypass PVL to GND with a minimum of 1µF ceramic capacitor as close as possible to the device.
3	ADDR	I2C Address Setting. Connect to PVL or GND or connect a 51kΩ or 91kΩ resistor from ADDR to GND to set one of the four address options. See Table 1.
4	VREFLN	Internal Reference. Bypass VREFLN to GND with a 100nF ceramic capacitor.
5	DGND	Digital Ground. Connect DGND directly to the exposed pad of the package.
6	SDA	I2C Data I/O. Connect a pullup resistor from SDA to the logic supply.
7	SCL	I2C Clock Input. Connect a pullup resistor from SCL to the logic supply.
8	FLTB	Open-Drain, Active-Low Fault Output. FLTB asserts low when any diagnostic bit is asserted if it is not masked. Connect a pullup resistor from FLTB to the logic supply.
9	AOUT	Analog Output. AOUT outputs a voltage that represents the load current of the selected output OUT1 or OUT2. An internal multiplexer controlled through I2C sets the selected channel for AOUT. If AOUT is used, place a 100kΩ resistor and a 220pF capacitor from the pin to GND.
10	FB2	Feedback Connection for the OUT2 Output. Connect FB2 to OUT2.
11	GND	Ground. GND is the current return path connection for the low-noise analog signals. Connect GND to the exposed pad of the package.
12	OUT2	Regulator Output 2. Connect a capacitor with a minimum value of 10µF from OUT2 to PGND, placing it as close as possible to the IC. A protection diode can also be used to protect OUT2 from negative voltage transients.
13	EN	Main Enable Input for the MAX20084. When EN is goes high, the internal PVL regulator is enabled and the I2C interface becomes active. In the case of the MAX20084ATEB, LDO1 is also enabled with the default configuration when EN is goes high. EN has an internal pulldown resistor.
14	IN2	Supply Input. Connect IN2 and IN1 together directly at the IC.
15	IN1	Main Supply Input. Connect a 4.5V to 18V supply to IN1. Bypass IN1 to GND with a combination of ceramic capacitor of value 4.7µF and optionally an electrolytic capacitor. See the *Short-to-Battery and Reverse-Current Protection* section. Connect IN1 and IN2 together directly at the IC.
16	OUT1	Regulator Output 1. Connect a capacitor with a minimum value of 10µF from OUT1 to GND, placing it as close as possible to the IC. A protection diode can also be used to protect OUT1 from negative voltage transients.
—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the IC ground connection. EP must be connected to ground.

Functional Diagram



Detailed Description

The MAX20084 is a dual high-voltage, I2C-controlled, current-sensing LDO/switch designed to operate with an input voltage range from 4.5V to 28V (40V load dump tolerant). The device provides phantom power over coax cable to remote radio frequency low-noise amplifiers (LNAs) in automotive systems with a maximum current of 270mA per channel. The device also provides a regulated output voltage adjustable between 3.3V and 12V, or the device can be configured as a switch.

The device monitors the load current using an internal analog-to-digital converter (ADC), and in addition the AOUT pin, provides an output voltage proportional to the sensed load current on the selected channel. An accurate programmable current limit protects the input supply against both overcurrent and short-circuit conditions. The device features an open-drain fault indicator output, over- temperature warning, and shutdown.

The device also features short-to-battery protection to latch off the internal LDO/switch during a short-to-battery event. During a thermal overload, the device reduces power dissipation by entering thermal shutdown. It includes a high-voltage-capable enable input to place the complete device in a low-power shutdown mode.

After enabling the MAX20084ATEA/VY+ both channels are off by default and can be turned on through I2C. After enabling the MAX20084ATEB/VY+, channel 1 immediately turns on as a 5V-output LDO with default settings, while the MAX20084ATEB/VY+ channel 2 is off by default and can be enabled successively through I2C.

Short Circuit and Overcurrent

The current limit of each channel is programmed by writing to the ILIM1 and ILIM2 registers. When the current in a channel reaches the set current limit, the output current of the LDO/switch is limited while the output remains on until the blanking time elapses. If the channel current is above the overcurrent setting in the OC_OL register at the end of the blanking time the channel is disabled and an overcurrent (OC_) fault is declared. If the OC_ fault is not masked the FLTB pin goes low to indicate a fault to the local microcontroller.

If the output voltage of a channel goes below 0.65V, the current limit is automatically reduced to 50mA. This lower current-limit level is also applied during startup while the output voltage is less than 1V. The configured current limit is reestablished when the output voltage is above 1V. To properly execute the startup sequence, maximum output capacitance must be limited depending on the selected current limit and blanking time:

$$C_{OUT} < t_{BLANK} \times I_{LIM}$$

The blanking time is also programmable. Use the 200ms option only for low-current applications to avoid excessive power dissipation in the case of overcurrent.

After an overcurrent event, it is necessary to wait some time before reenabling the output to avoid overheating of the device (and thermal shutdown). Calculate the minimum delay using the following equation:

$$t_{RETRY} > t_{BLANK} \times I_{LIM} \times V_{IN}/P_{MAX}$$

where t_{RETRY} is the minimum time between retries, t_{BLANK} is the programmed blanking time, I_{LIM} is the current limit set through I2C and P_{MAX} is 2W at 70°C.

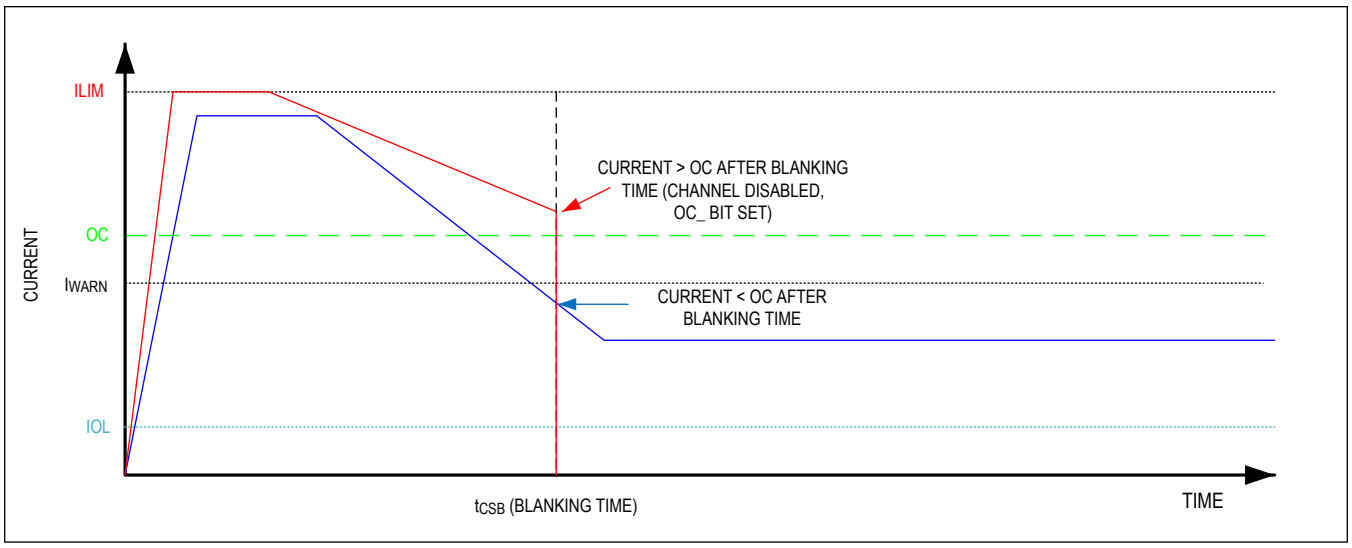


Figure 1. Load Current Template

Short-to-Battery and Reverse-Current Detection

Due to a system fault either or both of the OUT_ pins can be shorted to the battery. Each channel detects this failure by comparing the voltage at OUT_ and IN_ before the channel turns on. Every time the LDO/switch is enabled by setting an EN_ bit high (SETUP1 register) and when exiting thermal shutdown, the short-to-battery detection test is performed. At this point, if the device detects the short-to-battery fault, the LDO/switch stays off and the SB_ bit is set. The fault is latched, and the startup resumes when the short-to-battery fault has been removed and the appropriate EN_ bit toggled.

During normal operation if a short-to-battery fault results in a reverse voltage being detected across the channel for more than 9µs (typ), the LDO/switch is latched off and the IREV_ bit is set. To remove the latched condition after a reverse-current fault, the fault condition must first be removed and the appropriate EN_ bit toggled.

Series inductance combined with the output capacitor can produce ringing during large load transients when enabling the LDO/switch, which results in an output voltage that temporarily exceeds the input voltage. Blanking is implemented during startup. The reverse current blanking time ($t_{BLANKREV}$) is 16ms (typ).

When the device is operated with an input voltage close to the output voltage, as in switch mode operation or LDO mode in dropout, care must be taken to avoid a false reverse-current detection in the presence of a short circuit-to-ground fault. If both channels are enabled and one channel is shorted to ground after startup, the current drawn from the input capacitor can result in a temporary dip in the input voltage and trigger the reverse-current detection fault. To avoid this false trigger event, use an electrolytic capacitor of at least 100µF on IN_.

Thermal Warning/Shutdown

An internal temperature sensor protects the device from overheating. The device can issue a thermal warning at a programmable temperature of +95°C, +105°C, +115°C, or +125°C. Set the warning temperature by writing to the TWARN[1:0] bits in the SETUP2 register. In case the temperature continues to increase, the device turns off if the junction temperature exceeds +165°C (typ). It turns on again when the device temperature drops by approximately 15°C (typ).

Input Undervoltage and Overvoltage Lockout

The device includes undervoltage lockout circuitry (UVLO) to prevent erroneous switch operation as the input voltage rises or during brownout conditions. As the input voltage rises during startup, the voltage must exceed V_{UVLOR} before the device begins operation. If the input voltage drops below V_{UVLOF} during operation, the device is disabled.

The device also features an overvoltage lockout (OVLO) threshold of +21V (typ). When V_{IN} is greater than V_{OVLO}, the

device immediately turns off the channel. An overvoltage shutdown is indicated in the DIAG2 register by the OV bit.

Disable the overvoltage protection feature by setting the DISOV bit in register SETUP1, but note that power dissipation at high input voltages can cause thermal shutdown.

I2C Interface

The I2C interface consists of a serial-data line (SDA) and serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX20084 and the master at rates up to 400kHz. The MAX20084 is a slave device that transfers and receives data. The master (typically a microcontroller) initiates data transfer on the bus and generates the SCL signal to permit that transfer.

Slave Address

A bus master initiates communication with a slave device by issuing a START (S) condition followed by a slave address. When idle, the device waits for a START condition followed by its slave address. When the device recognizes a slave address, it is ready to accept or send data. The device offers four slave addresses, depending on the state of the ADDR pin. See Table 1 for the slave address options.

Table 1. I2C Addresses

ADDR PIN CONNECTION	I2C 7-BIT ADDRESS
GND	0x3A
51kΩ resistor to GND	0x3C
91kΩ resistor to GND	0x3B
PVL	0x3D

The least significant bit (LSB) of the address byte (R/W) determines whether the master is writing to or reading from the device (R/W = 0 selects a write operation, R/W = 1 selects a read operation). After receiving the address, the device (slave) issues an acknowledge by pulling SDA low for one clock cycle.

I2C Write Operation

A write operation (Figure 2) begins with the bus master issuing a START (S) condition followed by seven address bits and a write bit (R/W = 0). If the address byte is successfully received, the device (slave) issues an acknowledge (A). The master then writes to the slave and the sequence is terminated by a STOP (P) condition for a single write ope

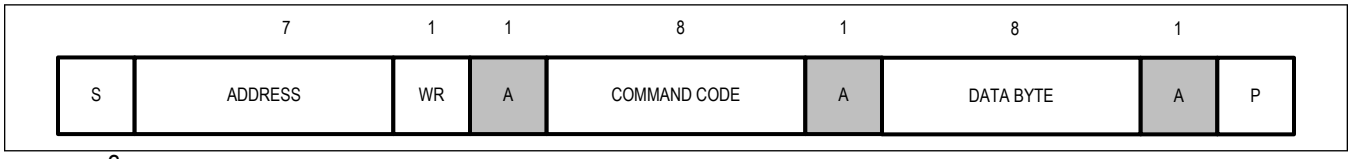


Figure 2. I2C Write

I2C Read Operation

In an I2C read operation (Figure 3), the bus master issues a write command first by initiating a START (S) condition followed by seven address bits, a write bit (R/W = 0) and the 8-bit register address. The master then issues a repeated START (Sr) condition, followed by seven address bits, a read bit (R/W = 1). If the address byte is successfully received, the device (slave) issues an acknowledge (A). The master then reads from the slave. For continuous read, the master issues an acknowledge bit (AM) after each received byte. The master terminates the read operation by sending a not acknowledge (N) bit. The device then releases the data line.

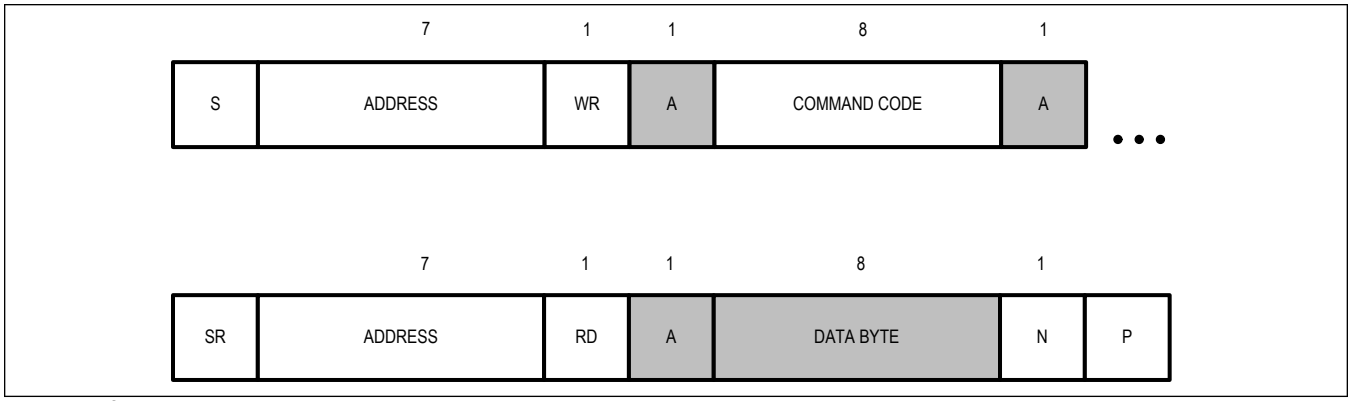


Figure 3. I2C Read

Register Map

ADDRESS	NAME	MSB							LSB
I2C									
0x00	DEV_ID[7:0]	DEVICE_ID[4:0]					REVISION_ID[2:0]		
0x01	ILIM1_REG[7:0]	–	–	–	ILIM1[4:0]				
0x02	ILIM2_REG[7:0]	–	–	–	ILIM2[4:0]				
0x03	OC_OL1[7:0]	IOC1[4:0]					IOL1[2:0]		
0x04	OC_OL2[7:0]	IOC2[4:0]					IOL2[2:0]		
0x05	IWARN[7:0]	IW1[3:0]				IW2[3:0]			
0x06	VOUT1_REG[7:0]	–	VOUT1[6:0]						
0x07	VOUT2_REG[7:0]	–	VOUT2[6:0]						
0x08	SETUP1[7:0]	–	–	DISOV	EN1	EN2	DISREV1	DISREV2	AOUT-MUX
0x09	SETUP2[7:0]	–	–	–	–	TWARN_SET[1:0]		TBLANK_SET[1:0]	
0x0A	IOUT1_REG[7:0]	IOUT1[7:0]							
0x0B	IOUTL1_REG[7:0]	IOUTL1[7:0]							
0x0C	IOUT2_REG[7:0]	IOUT2[7:0]							
0x0D	IOUT2L_REG[7:0]	IOUTL2[7:0]							
0x0E	DIAG1[7:0]	OC1	OC2	OL1	OL2	SB1	SB2	TWARN	TSHUT-DOWN
0x0F	DIAG2[7:0]	ILIM1_ STAT	ILIM2_ STAT	WARN1	WARN2	IREV1	IREV2	OV	POR
0x10	MASK[7:0]	–	MASKREV	MASKOC	MASKOL	MASKSB	MASKT-WARN	MASKI-WARN	MASKOV

Register Details

DEV_ID (0x00)

Device-specific information

BIT	7	6	5	4	3	2	1	0
Field	DEVICE_ID[4:0]					REVISION_ID[2:0]		
Reset	0b10100					0b010		

BIT	7	6	5	4	3	2	1	0
Access Type	Read Only					Read Only		

BITFIELD	BITS	DESCRIPTION
DEVICE_ID	7:3	Unique device type identifier
REVISION_ID	2:0	Device revision code

ILIM1_REG (0x01)

Current-limit setting, channel 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ILIM1[4:0]				
Reset	–	–	–	0b01100				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE	
			ILIM1[4:0]	**CURRENT LIMIT (mA)**
			00000	50
			00001	70
			00010	100
			00011	110
			00100	120
			00101	130
			00110	140
			00111	150
			01000	160
			01001	170
			01010	180
			01011	190
			01100	200*
			01101	210
			01110	220
			01111	230
ILIM1	4:0	Current-limit setting, OUT1	10000	240
			10001	250
			10010	260
			10011	270
			10100	280
			10101	290
			10110	300

ILIM2_REG (0x02)

Current-limit setting, channel 2

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ILIM2[4:0]				

BIT	7	6	5	4	3	2	1	0
Reset	–	–	–	0b01100				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE	
			ILIM2[4:0]	CURRENT LIMIT (mA)
			00000	50
			00001	70
			00010	100
			00011	110
			00100	120
			00101	130
			00110	140
			00111	150
			01000	160
			01001	170
			01010	180
			01011	190
			01100	200*
			01101	210
			01110	220
			01111	230
ILIM2	4:0	Current-limit setting, OUT2	10000	240
			10001	250
			10010	260
			10011	270
			10100	280
			10101	290
			10110	300

OC_OL1 (0x03)

Overcurrent and open-load settings, channel 1

BIT	7	6	5	4	3	2	1	0
Field	IOC1[4:0]					IOL1[2:0]		
Reset	0b01110					0b110		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE	
			IOC1[4:0]	OVERCURRENT LEVEL (mA)
			00000	10
			00001	15
			00010	20
			00011	25
			00100	30
			00101	35
			00110	40
			00111	45
			01000	50
			01001	55
			01010	60
			01011	70
			01100	80
			01101	90
			01110	100*
			01111	110
			10000	120
			10001	130
IOC1	7:3	Overcurrent settings, channel 1	10010	140
			10011	150
			10100	160
			10101	180
			10110	200
			10111	220
			11000	250
			11001	270

BITFIELD	BITS	DESCRIPTION	DECODE	
			IOL1[2:0]	OPEN-LOAD CURRENT (mA)
			000	2
			001	2
			010	3
			011	4
			100	6
IOL1	2:0	Open-load settings, channel 1	101	8
			110	10*
			111	15

OC_OL2 (0x04)

Overcurrent and open-load settings, channel 2

BIT	7	6	5	4	3	2	1	0
Field	IOC2[4:0]					IOL2[2:0]		
Reset	0b01110					0b110		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE	
IOC2	7:3	Overcurrent settings, channel 2	**IOC2[4:0]**	**OVERCURRENT LEVEL (mA)**
			00000	10
			00001	15
			00010	20
			00011	25
			00100	30
			00101	35
			00110	40
			00111	45
			01000	50
			01001	55
			01010	60
			01011	70
			01100	80
			01101	90
			01110	100*
			01111	110
			10000	120
			10001	130
			10010	140

BITFIELD	BITS	DESCRIPTION	DECODE	
IOC2	7:3	Overcurrent settings, channel 2	10011	150
			10100	160
			10101	180
			10110	200
			10111	220
			11000	250
			11001	270
IOL2	2:0	Open-load settings, channel 2	**IOL2[2:0]**	**OPEN-LOAD CURRENT (mA)**
			000	2
			001	2
			010	3
			011	4
			100	6
			101	8
			110	10*
			111	15

IWARN (0x05)

Current warning level for channel 1/2

BIT	7	6	5	4	3	2	1	0
Field	IW1[3:0]				IW2[3:0]			
Reset	0b0110				0b0110			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE	
IW1	7:4	Current warning level for OUT1	**IW1[3:0]**	**CURRENT WARNING LEVEL (mA)**
			0000	15
			0001	30
			0010	40
			0011	50
			0100	60
			0101	70
			0110	80*
			0111	100
			1000	120
			1001	140
			1010	160
			1011	180
			1100	200
			1101	220
			1110	250
IW2	3:0	Current warning level for OUT2	**IW2[3:0]**	**CURRENT WARNING LEVEL (mA)**
			0000	15
			0001	30
			0010	40
			0011	50
			0100	60
			0101	70
			0110	80*
			0111	100
			1000	120
			1001	140
			1010	160
			1011	180
			1100	200
			1101	220
			1110	250

VOUT1_REG (0x06)

Output voltage setting, channel 1

BIT	7	6	5	4	3	2	1	0
Field	–	VOUT1[6:0]						
Reset	–	0b0000101						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE	
			VOUT1[6:0]	OUTPUT VOLTAGE (V)
			0000000	Switch mode
			0000001	3.3
			0000010	3.4
			0000011	3.5
			0000100	3.6
			0000101	5*
			0000110	5.1
			0000111	5.2
			0001000	5.3
			0001001	5.4
			0001010	5.5
			0001011	5.6
			0001100	5.7
			0001101	5.8
			0001110	5.9
			0001111	6
			0010000	6.1
			0010001	6.2
			0010010	6.3
			0010011	6.4
			0010100	6.5
			0010101	6.6
			0010110	6.7
VOUT1	6:0	OUT1 voltage setting	0010111	6.8
			0011000	6.9
			0011001	7
			0011010	7.1
			0011011	7.2
			0011100	7.3
			0011101	7.4
			0011110	7.5
			0011111	7.6
			0100000	7.7

BITFIELD	BITS	DESCRIPTION	DECODE	
			VOUT1[6:0]	OUTPUT VOLTAGE (V)
			0100001	7.8
			0100010	7.9
			0100011	8
			0100100	8.1
			0100101	8.2
			0100110	8.3
			0100111	8.4
			0101000	8.5
			0101001	8.6
			0101010	8.7
			0101011	8.8
			0101100	8.9
			0101101	9
			0101110	9.1
			0101111	9.2
			0110000	9.3
			0110001	9.4
			0110010	9.5
			0110011	9.6
			0110100	9.7
			0110101	9.8
			0110110	9.9
			0110111	10
VOUT1	6:0	OUT1 voltage setting	0111000	10.1
			0111001	10.2
			0111010	10.3
			0111011	10.4
			0111100	10.5
			0111101	10.6
			0111110	10.7
			0111111	10.8
			1000000	10.9

BITFIELD	BITS	DESCRIPTION	DECODE	
			VOUT1[6:0]	OUTPUT VOLTAGE (V)
			1000001	11
			1000010	11.1
			1000011	11.2
			1000100	11.3
VOUT1	6:0	OUT1 voltage setting	1000101	11.4
			1000110	11.5

BITFIELD	BITS	DESCRIPTION	DECODE	
			1000111	11.6
			1001000	11.7
			1001001	11.8
			1001010	11.9
			1001011	12

VOUT2_REG (0x07)

Output voltage setting, channel 2

BIT	7	6	5	4	3	2	1	0
Field	–	VOUT2[6:0]						
Reset	–	0b0000101						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE	
			VOUT2[6:0]	OUTPUT VOLTAGE (V)
			0000000	Switch mode
			0000001	3.3
			0000010	3.4
			0000011	3.5
			0000100	3.6
			0000101	5*
			0000110	5.1
			0000111	5.2
			0001000	5.3
			0001001	5.4
			0001010	5.5
			0001011	5.6
			0001100	5.7
			0001101	5.8
			0001110	5.9
			0001111	6
VOUT2	6:0	OUT2 voltage setting	0010000	6.1
			0010001	6.2
			0010010	6.3
			0010011	6.4
			0010100	6.5
			0010101	6.6
			0010110	6.7
			0010111	6.8
			0011000	6.9
			0011001	7.0
			0011010	7.1

BITFIELD	BITS	DESCRIPTION	DECODE	
			0011011	7.2
			0011100	7.3
			0011101	7.4
			0011110	7.5
			0011111	7.6
			0100000	7.7

BITFIELD	BITS	DESCRIPTION	DECODE	
			VOUT2[6:0]	OUTPUT VOLTAGE (V)
			0100001	7.8
			0100010	7.9
			0100011	8
			0100100	8.1
			0100101	8.2
			0100110	8.3
			0100111	8.4
			0101000	8.5
			0101001	8.6
			0101010	8.7
			0101011	8.8
			0101100	8.9
			0101101	9
			0101110	9.1
			0101111	9.2
			0110000	9.3
			0110001	9.4
			0110010	9.5
			0110011	9.6
			0110100	9.7
			0110101	9.8
			0110110	9.9
			0110111	10
VOUT2	6:0	OUT2 voltage setting	0111000	10.1
			0111001	10.2
			0111010	10.3
			0111011	10.4
			0111100	10.5
			0111101	10.6
			0111110	10.7
			0111111	10.8
			1000000	10.9

BITFIELD	BITS	DESCRIPTION	DECODE	
			VOUT2[6:0]	OUTPUT VOLTAGE (V)
			1000001	11
			1000010	11.1
			1000011	11.2
			1000100	11.3
			1000101	11.4
			1000110	11.5
			1000111	11.6
			1001000	11.7
			1001001	11.8
			1001010	11.9
VOUT2	6:0	OUT2 voltage setting	1001011	12

SETUP1 (0x08)

Output enable, disable reverse-current detection, disable overvoltage shutdown, AOUT select

BIT	7	6	5	4	3	2	1	0
Field	–	–	DISOV	EN1	EN2	DISREV1	DISREV2	AOUTMUX
Reset	–	–	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DISOV	5	If set to 1 disables the overvoltage shutdown (i.e., the switchoff of the channels)	
EN1	4	Output 1 enable	When 1 channel 1 is enabled. Default value 0. After startup, before writing the EN1 bit to 1, the VOUT1 register must have been written to.
EN2	3	Output 2 enable	When 1 channel 2 is enabled. Default value 0. After startup, before writing the EN2 bit to 1, the VOUT2 register must have been written to.
DISREV1	2	Disable reverse-current detection for channel 1.	When 1 short-to-battery protection is disabled on channel 1. Default value 0.
DISREV2	1	Disable reverse-current detection for channel 2.	When 1 short-to-battery protection is disabled on channel 2. Default value 0.
AOUTMUX	0	AOUT select	When 1 the voltage on AOUT reflects the current in channel 2. Default value 0 (channel 1 current).

SETUP2 (0x09)

Set warning temperature, blanking time

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	TWARN_SET[1:0]		TBLANK_SET[1:0]	
Reset	–	–	–	–	0b00		0b10	
Access Type	–	–	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE	
TWARN_SET	3:2	Set warning temperature	**TWARN_SET [1:0]**	**MINIMUM BLANKING TIME SETTING (ms)**
			00	95*
			01	105
			10	115
			11	125
TBLANK_SET	1:0	Set blanking time	**TBLANK [1:0]**	**MINIMUM BLANKING TIME SETTING (ms)**
			00	25
			01	50
			10	100*
			11	200

IOUT1_REG (0x0A)

ADC current readback, channel 1.

BIT	7	6	5	4	3	2	1	0
Field	IOUT1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE	
IOUT1	7:0	OUT1 current readback	**IOUT1 [7:0]**	**CURRENT (mA)**
			0x00	0
			0x01	1
			0x02	2
			0x03	3
			0x04	4
			0x05	5
			0x06	6
			...	...
			0xF9	249
			0xFA	250
			0xFB	251
			0xFC	252
			0xFD	253
			0xFE	254
			0xFF	255

IOUTL1_REG (0x0B)

ADC current readback, low-current range, channel 1

BIT	7	6	5	4	3	2	1	0
Field	IOUTL1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE	
			IOUTL1 [7:0]	CURRENT (mA)
			0x00	0
			0x01	0.2
			0x02	0.4
			0x03	0.6
			0x04	0.8
			0x05	1
			0x06	1.2
			0xF9	49.8
			0xFA	50
IOUTL1	7:0	OUT1 current readback, low-current range	0xFB	50.2
			0xFC	50.4
			0xFD	50.6
			0xFE	50.8
			0xFF	51 or greater

IOUT2_REG (0x0C)

ADC current readback, channel 2

BIT	7	6	5	4	3	2	1	0
Field	IOUT2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE	
			IOUT2 [7:0]	CURRENT (mA)
			0x00	0
			0x01	1
			0x02	2
			0x03	3
			0x04	4
			0x05	5
			0x06	6
			0xF9	249
			0xFA	250
IOUT2	7:0	OUT2 current readback	0xFB	251
			0xFC	252
			0xFD	253
			0xFE	254
			0xFF	255

IOUT2L_REG (0x0D)

ADC current readback, low-current range, channel 2

BIT	7	6	5	4	3	2	1	0
Field	IOUTL2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE	
			IOUTL2 [7:0]	CURRENT (mA)
			0x00	0
			0x01	0.2
			0x02	0.4
			0x03	0.6
			0x04	0.8
			0x05	1
			0x06	1.2
			...	...
			0xF9	49.8
			0xFA	50
IOUTL2	7:0	OUT2 current readback, low-current range	0xFB	50.2
			0xFC	50.4
			0xFD	50.6
			0xFE	50.8
			0xFF	51 or greater

DIAG1 (0x0E)

OUT1/2 diagnostics

BIT	7	6	5	4	3	2	1	0
Field	OC1	OC2	OL1	OL2	SB1	SB2	TWARN	TSHUT-DOWN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION
OC1	7	When 1, an overcurrent fault has been detected on channel 1.
OC2	6	When 1, an overcurrent fault has been detected on channel 2.
OL1	5	When 1, an open-circuit fault has been detected on channel 1.
OL2	4	When 1, an open-circuit fault has been detected on channel 2.
SB1	3	When 1, a short-to-battery fault has been detected on channel 1.
SB2	2	When 1, a short-to-battery fault has been detected on channel 2.
TWARN	1	When 1, the junction temperature has exceeded the warning threshold.
TSHUTDOWN	0	When 1, the junction temperature has exceeded the shutdown threshold.

DIAG2 (0x0F)

Current warning, OV status, power-on-reset

BIT	7	6	5	4	3	2	1	0
Field	ILIM1_STAT	ILIM2_STAT	WARN1	WARN2	IREV1	IREV2	OV	POR
Reset	0b0	0b0	0b0	0b0	0x0		0b0	0b1
Access Type	Read Only	Read Only	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION
ILIM1_STAT	7	Current limit status bit for channel 1
ILIM2_STAT	6	Current limit status bit for channel 2
WARN1	5	Current warning channel 1. When 1, the current on channel 1 has exceeded the warning threshold.
WARN2	4	Current warning channel 2. When 1, the current on channel 2 has exceeded the warning threshold.
IREV1	3	When set, this bit indicates that a reverse-current event occurred on channel 1.
IREV2	2	When set, this bit indicates that a reverse-current event occurred on channel 2.
OV	1	OV status. When 1, the input voltage has exceeded the over-voltage threshold.
POR	0	Power-on-reset. When 1, this is the first read from this register after a power- on-reset of the device. Power-on value 1. This bit is reset to 0 on the first read from this register.

MASK (0x10)

Mask register for FLTB pin

BIT	7	6	5	4	3	2	1	0
Field	–	MASKREV	MASKOC	MASKOL	MASKSB	MASKT- WARN	MASKI- WARN	MASKOV
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
MASKREV	6	Reverse current mask
MASKOC	5	When 1, overcurrent faults do not cause FLT to assert low. Default value 0.
MASKOL	4	When 1, open-load faults do not cause FLT to assert low. Default value 0.
MASKSB	3	When 1, short-to-battery fault does not cause FLT to assert low. Default value 0.
MASKTWARN	2	When 1, a temperature warning does not cause FLT to assert low. Default value 0.
MASKIWARN	1	When 1, overcurrent warning faults do not cause FLT to assert low. Default value 0.
MASKOV	0	When 1, an overvoltage does not cause FLT to assert low. Default value 0.

Applications Information

Input Capacitor

Connect a > 4.7µF low-ESR ceramic capacitor from IN to GND to limit the input-voltage drop during momentary output short-circuit conditions and to protect the device against transients due to inductance on the input. Larger capacitor values reduce the voltage undershoot and overshoot in case of reverse current.

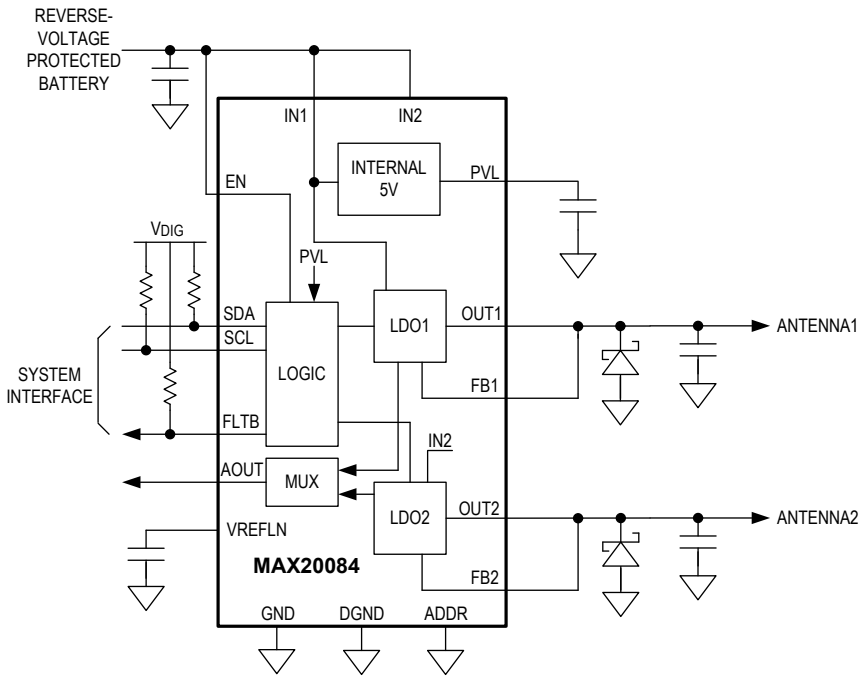
Output Capacitor

Connect a minimum of parallel 10µF and 0.1µF low-ESR ceramic capacitors between OUT1/OUT2 and GND for regulator stability. These capacitors should be placed as close as possible to the device. Utilize capacitors with an X7R dielectric to ensure stability over the operating temperature range of the device.

In an analogous fashion to the input capacitor, an output capacitor protects the device against transients due to any series inductance in the output. The negative voltage on OUT1/OUT2 pins should be limited to -0.3V DC or -0.6V for transients up to 1.5ms. A Schottky diode is required as a clamp if transients are expected to go below ground.

Typical Application Circuits

2-Channel Application



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DEFAULT LDOS STATE AT POWER-UP
MAX20084ATEA/VY+	-40°C to +125°C	16 SW-TQFN	LDO1 off, LDO2 off
MAX20084ATEB/VY+	-40°C to +125°C	16 SW-TQFN	LDO1 on, LDO2 off
MAX20084ATEA/V+**	-40°C to +125°C	16 TQFN	LDO1 off, LDO2 off

+Denotes a lead(Pb)-free/RoHS-compliant package.

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	6/18	Updated TOCs 15, 19, 20	6, 7
2	8/18	Updated Electrical Characteristics table and register tables	3, 14–30
3	11/19	Updated General Description, Benefits and Features, Package Information, Electrical Characteristics table, and Ordering Information	1, 2, 4, 32
4	9/20	Updated Applications Information related to negative voltage on OUT1/OUT2. Updated Typical Application Circuit.	33, 34